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Abstract:

Silicon photonics has generated a growing interest with impressive results on active devices like optical modulators and photodetectors in the last few years. In the framework of the European project HELIOS, several research groups and industrial partners work on the main building blocks to make high-speed optical links based on either silicon-based materials or III-V components bonded on silicon. Here, we present an overview of the main achievements on PN and PIPIN optical modulators based on carrier depletion and on germanium and III-V photodetectors integrated with silicon waveguides.

Keywords: microphotonics, waveguide, silicon-on-insulator, optical modulator, carrier depletion, germanium, InGaAs, photodetector, integrated optics

I. Introduction

Silicon-based photonics has generated an increasing interest in recent years, mainly for optical telecommunications or optical interconnects in microelectronic circuits [1] with some promising solutions for biophotonics. The rationale of silicon photonics is the reduction of photonic system cost and the increase of the number of functionalities on the same integrated chip by combining photonic components with electronic circuits.

A photonic electronic integrated circuit needs to address the different routes of convergence of photonics and electronics on large-scale wafers. Several integration technology options are presented in figure 1. Each integration scheme has some advantages and drawbacks and can be considered in the future according to the applications [2].

Three integration schemes can be considered:

• The first option is to integrate the photonic layer at the top of the CMOS circuit. Two possibilities can be considered: either the photonic layer is inserted at the top of the metallization levels using back-end fabrication (i.e. low temperature

Silicon Photonics V, edited by Joel A. Kubby, Graham T. Reed, Proc. of SPIE Vol. 7606, 76060S © 2010 SPIE · CCC code: 0277-786X/10/\$18 · doi: 10.1117/12.843798 process) or the photonic layer is bounded at the top of the CMOS circuit using wafer bonding technology.

- The second option combines the fabrication of transistors and of the photonic devices at the front–end fabrication level.
- The last option considers the back-side integration either using back-end or wafer bonding processes.



Fig 1 : Integration schemes of the photonic and the electronics layers

In the framework of the European project HELIOS (pHotonics ELectronics functional Integration on CMOS - <u>www.helios-project.eu</u>), European companies, public laboratories and research centres are combining their efforts to develop high efficiency building blocks and to explore the different possibilities to integrate photonics and electronics.

The final demonstrators developed in this project are:

- 40 Gb/s modulator
- 10x10 Gb/s transceivers
- mixed analog and digital transceiver module for multifunction antennas
- photonic QAM-10Gb/s wireless transmission system

In all integration schemes, reliable building blocks to guide [3,4], distribute [5,6], modulate [7-10], emit [11-14] and detect [15-23] light have to be studied.

In this paper, we only present the recent results on optical modulators based on carrier depletion and photodetectors integrated in SOI waveguides.

II. Optical modulators

Several physical effects can be used to obtain light modulation in silicon. However, to date, the more efficient effect to achieve high speed optical modulator is to use carrier depletion in PN or PIN diodes.

Two optical modulators are studied and presented in figure 2



Figure 2: Optical modulator studied in the framework of the Helios project (a) 400-nm thick PIPIN diode and (b) 220-nm thick PN diode.

The first modulator is based on a 400nm thick PIPIN diode (figure 2a). The considered silicon rib waveguide height and width are 400 nm and 660 nm, resepctively, while the etching depth is 100 nm. Such a geometry leads to a single mode propagation of the guided mode at 1.55 μ m wavelength. A p-doped slit is inserted in the intrinsic region of the lateral pin diode and acts as a source of holes. High p and n- doped regions are placed apart from the rib region to define the pin diode. As a large part of the waveguide is not doped and the metallic contacts are deposited on both sides of the waveguide, low propagation loss is obtained whilst keeping a high modulation efficiency. Such a design is favorable for high speed operation as the capacitance and the access resistances are reduced in comparison with the usually considered vertical structures.

The principle is the following: at equilibrium, holes are confined in the doped slit inside the rib waveguide. A good overlap between the carrier density variation zone (doped slit) and the guided mode occurs. Under a reverse bias, holes are swept out which leads to an effective index variation. This index variation creates a phase shift of the guided mode. The phase shifter is inserted in both arms of a 4-mm long asymetric Mach-Zehnder interferometer and electrodes are used to bias one arm.

The measured insertion loss is about 5 dB and DC extinction ratio is around 14 dB from 0 to a reverse bias of 10 V. A bandwidth of 15GHz has been obtained which is compatible with 10 Gbit/s operation.

The second modulator is based on a 220nm thick lateral PN diode (figure 2b). The principle is similar to the previous phase shifter. The concentrations of the n and p type regions are tuned such that the majority of the depletion occurs in the waveguide with applied voltage. Furthermore, the doping level is chosen to reduce the optical loss and ensure efficient phase variation. The main advantage of this structure is that no critical alignment of the implant windows is required. The pn junction position corresponds with waveguide edge as a result of a self aligned process. The phase shifter is inserted in both arms of an asymetric Mach-Zehnder however only one arm is biased to induce intensity modulation.

A static extinction ratio larger than 25dB has been demonstrated with a 3V reverse bias applied to a 3.5mm phase shifter. Furthermore, the first measurement of the electro-optic bandwidth has demonstrated a cut-off frequency of 8GHz which is also compatible with 10 Gbit/s operation.

Both optical modulators present promising behaviour for the next generations of 10Gbit/s photonic circuits.

III. Photodetectors on silicon

The choice of the absorbent material at telecom wavelength is directly linked to the integration scheme we consider (figure 1). Indeed, two kinds of active material can be used to detect light on silicon: germanium which is directly compatible with CMOS technology and III–V compound semiconductors which can be heterogeneously integrated on silicon.

If all photonic devices are processed at low temperature (back-end approach), InGaAs semiconductor will be used while in other options, either III-V or germanium can be considered.

In the framework of the European project HELIOS, compact and efficient InAlAs–InGaAs metal–semiconductor–metal photodetectors and germanium photodetectors integrated on silicon-on-insulator (SOI) waveguides are studied and optimized to achieve data transmission up to 40 Gbit/s.

1. InGaAs photodetector on silicon

The first approach is based on the integration of InGaAs photodetectors by means of die-towafer bonding using benzocyclobutene (DVS-BCB) as a bonding agent. The photodetector design we propose is shown in Figure 3a.



Figure 3: (a) Three dimensional- and (b) cross-section view of waveguide integrated MSM detector.

An InAlAs/InGaAs metal-semiconductor-metal (MSM) detector is integrated on top of an SOI waveguide using a very thin (< 300nm) DVS-BCB bonding layer. The SOI waveguides are 220nm high and deeply etched. Light from the SOI waveguide is evanescently coupled into the detector. In this design, the optical absorption path length is independent of the carrier transit-length and thus, offers the possibility for efficient, high bandwidth operation.

Figure 3b shows the cross-section of the MSM-detector on top of the SOI waveguide. The material structure of the thin film MSM detector consists of a 40nm InAlAs Schottky barrier enhancement layer, 20nm InAlAs/InGaAs superlattice layer to decrease carrier trapping by the bandgap discontinuity between $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$ and a 145nm $In_{0.53}Ga_{0.47}As$ absorption layer. Two Schottky electrodes are deposited on top, with the same spacing as the SOI waveguide width.

The MSM-detector is designed in such a way that there is phase matching between the detector waveguide mode and the mode in the SOI waveguide. This allows very efficient evanescent coupling and moreover a strong absorption for a short length.

Such a photodiode exhibits a dark current as low as 3nA and a responsivity as high as 1 A/W under 5V bias. Furthermore, the expected bandwidth is larger than 30GHz which is compatible for 40Gbit/s data transmission.

2. Germanium on silicon photodetector

Monolithic integration of a photodetector in a SOI waveguide requires an active material compatible with the IV/IV semiconductor technology. Silicon-Germanium (SiGe) compounds are natural candidates to realize the photodetection. Indeed, silicon is transparent at the considered telecom wavelengths (from $1.3 \,\mu m$ to $1.6 \,\mu m$). Addition of Ge in silicon is thus needed to increase absorption efficiency and consequently to generate photocurrent. Optical absorption is directly linked to the mean content of Ge in the structure: bulk Ge is thus the more appropriate candidate for high-speed and efficient detection.



Figure 4: Electric field amplitudes from 3D-FDTD simulations at the wavelengths 1.55µm and 1.31 µm for butt coupling configuration

Ge is selectively grown at the end of the waveguide in a silicon recess in order to address butt coupling integration. Such configuration allows a very short absorption length: 95 % of the light intensity is absorbed over about 4 μ m at 1.31 μ m and less than 7 μ m at 1.55 μ m (figure 4).

The photodetector considered here is a vertical pin diode defined as a N-doped silicon layer acting as bottom contact, a 300nm thick undoped i-Ge layer and a P-doped Ge layer for the top contact (figure 5).



Figure 5: Schematic and SEM views of Ge vertical pin diode inserted in silicon-on-insulator waveguide.

The dark current and the responsivity are 18nA under -1V bias and 1 A/W under -4V bias respectively.

The device RF bandwidth/eye diagram responses have been characterized and results are given in Fig. 6 and Fig. 7, respectively.

The -3dB bandwidth are 12GHz, 28GHz and 42GHz under 0V, -2V and -4V biases, respectively. Under -4V bias, an open eye diagram at 40 Gb/s has been obtained (figure 6).



Figure 6 Normalized optical response of the Ge pin vertical photodetector as a function of frequency for different biases.



Figure 7: Open eye diagram at 40 Gbit/s.

Table 1 presents a non-exhaustive state of the art of photodetectors in/on silicon using either III-V materials bonded on Si or germanium on silicon.

	Ge-on-Si photodetectors				III-V-on-Si photodetectors			
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	MIT	UPS-IEF & LETI	INTEL	UPS-IEF & LETI	PICMOS	IMEC	INTEL	LETI
Year	2007	2007	2007	2008	2006	2007	2007	2007
structure	PIN	MSM	PIN	PIN	PIN	MSM	PIN	PIN
Dark current at -1V	~1 µA	~100 µA	~170 nA	~20 nA	~1 nA	~1 nA	~50 nA	~10 nA
Responsivity	~1.08 A/W	> 1 A/W	~0.9 A/W	~1 A/W	~0.45 A/W	~1 A/W	~0.31 A/W	~0.01 A/W
Bandwidth	7.2 GHz	25 GHz	31 GHz	42 GHz	33 GHz	-	0.5 GHz	-

Table 1: Non-exhaustive state of the art of germanium and III-V photodetectors on silicon [15-23].

It shows that both III-V bonded on Si and Ge directely integrated on Si show competitive performances with low dark currents, high responsivity and large bandwidths figures. They are both valid solutions for photodetection for data transmission up to 40 Gb/s.

IV. Conclusion

In conclusion, we report recent results of optical modulators and photodetectors on silicon developed in the framework of the European project HELIOS. To date, optical modulator behaviors allow achieving 10 Gbit/s data transmission and InAlAs–InGaAs metal–semiconductor–metal photodetectors and germanium photodetectors exhibit performances of operation up to 40 Gbit/s.

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