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Monolithic coupling strategy between high- and mid-index multi-micron waveguides for O-band applications

Ilias Skandalos[a], Thalía Domínguez Bucio[a], Lorenzo Mastronardi[a], Yaonan Hou[a], Teerapat Rutirawut[a], and Frederic Gardes[a]

[a]Optoelectronics Research Centre, University of Southampton, University Road, Southampton, United Kingdom

ABSTRACT

In this work, a coupling strategy between mid-index SiNx and high-index active waveguides on the same silicon chip is proposed. To that aim, a sophisticated proof-of-concept integration between N-rich SiN and SOI micro-metric waveguides is demonstrated achieving a <0.5 dB coupling for both TE/TM polarisations. The optical tunability of SiNx allows the mitigation of the mid-high refractive index discrepancy by interposing a SiO_2/Si-rich SiN double-layer anti-reflective coating, attaining back-reflections close to −20 dB. On that basis, it is shown numerically that a sub-dB interconnection between multiple-quantum well/dot stratified stacks and a silicon nitride passive waveguide is achievable, while keeping the introduced back-reflection level below −30 dB.

Keywords: SiN_x, Monolithic, Integration, Actives, Passives, Silicon

1. INTRODUCTION

Today's datacom applications require fast and low-power silicon photonic interconnects,[1] setting a high-standard performance condition for the related passive and active components to meet.[2] Low-loss and compact SOI waveguides have been established as the passive workhorse in silicon photonics,[3] nevertheless the formation of efficient active devices on silicon requires a multi-material integration.[4,5] That performance can be met by active components comprised of quantum well/dot active regions, however their monolithic integration on silicon requires thick buffers/claddings forming multi-micron waveguides, which lead to a size-mismatch challenge for the passive-to-active interconnection.[6]

Silicon nitride (SiNx) is gaining ground as a CMOS fab material of low-losses and high fabrication tolerances, important for (de-)multiplexing applications.[7] Its low-temperature (350 °C) growth capability[8] provides a back-end-of-line integration to active devices, by building defect-free layers of the same order of size, setting the ground for a SiNx-based passive circuitry and/or a pathway to SOI waveguides.

In this work, a coupling strategy between mid-index SiNx and high-index active waveguides on the same silicon chip is proposed, toward silicon-substrate fully integrated active components. To that aim, a proof-of-principle SOI-N-rich SiN butt-coupling scheme of <0.5 dB coupling loss and close to −20 dB back-reflection for the fundamental TE/TM polarisations is demonstrated. Based on the demonstrated results, the SiN-integration of quantum well/quantum dot (QW/QD) stratified stacks is numerically investigated.

2. PROOF-OF-CONCEPT SOI-SIN BUTT-COUPLING

The proof-of-principle micro-metric scheme originally demonstrated in,[9] utilises 1.25 μm thick SOI and N-rich SiN (low-loss in the O-band) rib waveguides. The devices are fabricated on an 8-inch SOI wafer with a 2 μm bottom oxide. The N-rich SiN is grown through PECVD and planarised via CMP. Both SOI and N-rich SiN waveguides are formed by 248 nm DUV lithography and ICP etching (0.85 μm), while they are capped by SiO_2 cladding. Toward optimal photonic coupling a double-layer anti-reflective coating pair of SiO_2/Si-rich SiN is used for the refractive index difference mitigation. The interface is protected during fabrication by wide un-etched

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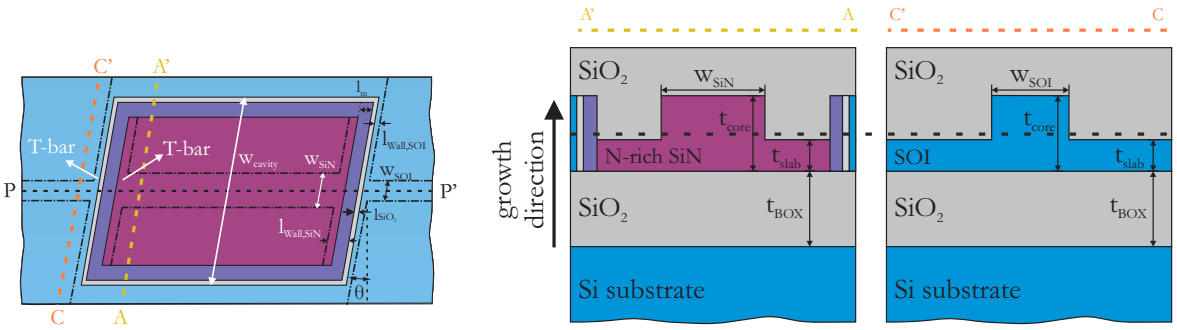
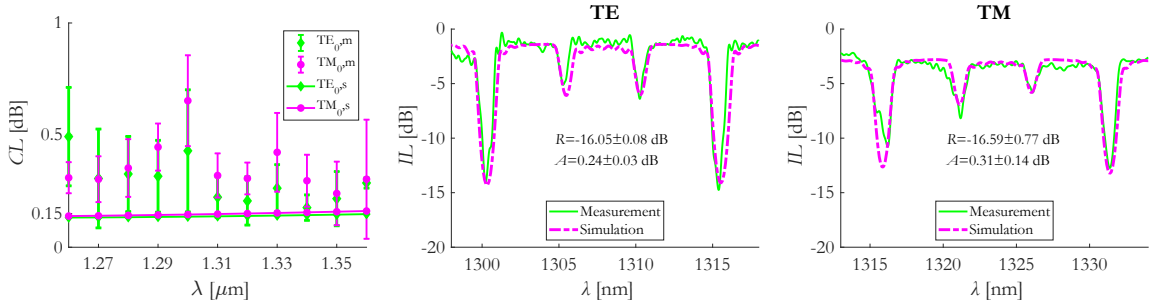


(a) (b)

Figure 1: SOI-to-SiN butt-coupling interconnection concept. In **(a)** the top view of the interconnection is depicted, with the N-rich SiN facets connected to SOI waveguides. The PP' dashed line reveals the lateral view of the structure, while cross-sections of the waveguides are depicted in **(b)**.

areas near the interface (T-bars). The top view and the related cross-sections of the involved waveguides are illustrated in figure 1.

Multiple cut-back structures of flat interfaces were fabricated toward the coupling loss and the back-reflection levels evaluation. Several chips at the centre of the wafer were characterised to include any statistical variation. The coupling loss data along with the statistical error are depicted in figure 2(a) for the entire O-band, revealing values <0.5 dB for both TE/TM polarisations at the majority of the wavelengths. The back-reflection induced at the interface is calculated through the fit the measured spectral response of a structure with 14 interfaces and the corresponsing simulated transmissivity model. The fit is done in the entire O-band and a restricted range of wavelengths is given in figures 2(b) and 2(c) revealing a <-16 dB back-reflection, however more recent fabrication runs showed improvement down to -19.56 dB.

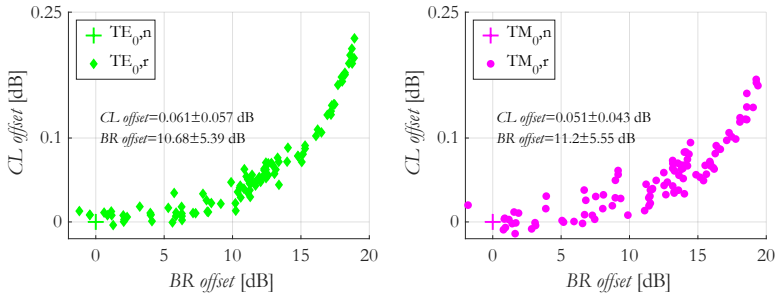


(a) (b) (c)

Figure 2: O-band cut-back coupling loss (a) and back-reflection (b), (c) data. The back-reflection is provided in a restricted range of wavelengths for illustration purposes.

The original numerical assessment of the interface quality showed <0.15 dB coupling loss and <-30 dB back-reflection levels. The discrepancy is explained through geometric/material fabrication variations as illustrated in figure 3. In particular, figure 3 presents the offset of the two metrics when the involved layers are geometric- and material-based varied. A variation of ± 20 nm from the nominal value is assumed for the geometric variables and a change of ± 0.02 is accounted for the refractive indices of the materials. Both TE and TM polarisations are studied. The wavelength is set at 1310 nm. The mean value and the standard deviation of the two metrics added to the simulated values align with the characterised results.

Further author information:
Ilias Skandalos: E-mail: I.Skandalos@soton.ac.uk

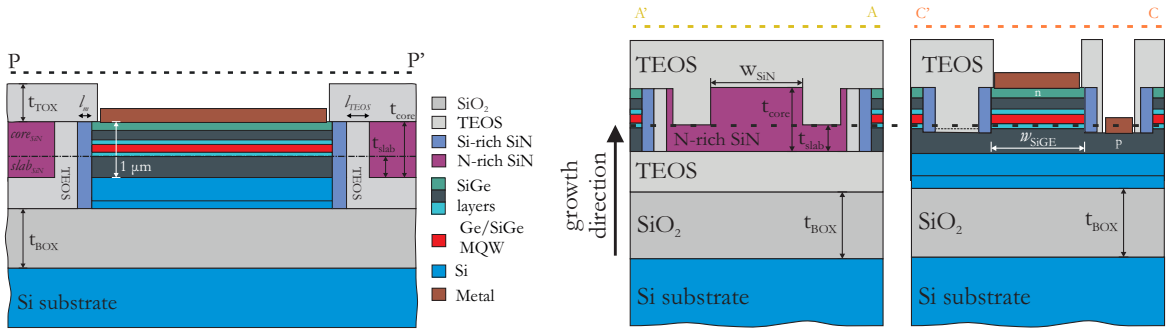


(a) (b)

Figure 3: Scatter diagrams for the simulated offset of the coupling loss and the back-reflection metrics, when uniform random numbers in a restricted range are set to the varying geometrical and material parameters that define the quality of the transition. The indices n and r refer to the nominal and the random cases, respectively.

3. SIN-INTEGRATED QW/QD STRATIFIED MEDIUMS

Based on the results of section 2 the integration of a SiGe multiple QW (MQW) and a III/V dot-in-well (DWELL) stack is investigated. A MQW-to-SiN example is given in figure 4, where the MQW stack and the SiN waveguide are 1 μm thick. The SiN section is a rib waveguide with a 0.4 μm slab.



(a) (b)

Figure 4: SiN-to-MQW butt-coupling interconnection concept. The PP' dashed line in (a) reveals the side view of the structure depicted in **(a)**. The MQW stack stands in the middle and its facets are connected to the N-rich SiN waveguides. The cross-sections of the waveguides are depicted in (b).

Following the same simulation strategy as for the SOI-to-SiN scheme, a <0.3 dB coupling loss and <−50 dB back-reflection active-to-passive transition is disclosed. In that way, the high-coupling loss issue is relaxed, mainly apparent due to QW pinching when the selective epitaxial growth method in pre-etched SOI wafers is used. In a similar manner, a 3.7 μm thick DWELL stack is examined in terms of the coupling efficiency with an N-rich SiN waveguide. The statistics-assisted simulations show a guaranteed <−40 dB back-reflection and a close to 1.2 dB coupling loss capability. The enhanced DWELL-to-SiN interconnection efficiency takes advantage of the coupling strategy flexibility, avoiding active-to-passive positioning misalignment when the stack is grown in pre-etched SOI substrates.

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