An Extended Boost Three-Phase Transformerless PV Inverter for Common-Mode Leakage Current Reduction

Georgios I. Orfanoudakis, *Member, IEEE*, Eftichios Koutroulis, *Senior Member, IEEE*, Suleiman M. Sharkh, *Senior Member, IEEE*, and Michael A. Yuratich

***Abstract*—A known issue with transformerless photovoltaic (PV) inverters is the generation of common-mode (CM) ground leakage currents. Single-phase transformerless topologies have been proposed that can achieve CM current suppression, but the relevant concepts do not perform equally well when applied to three-phase topologies. Existing three-phase transformerless topologies also have increased component count and losses, while their modified modulation strategies typically reduce output voltage quality and DC-bus voltage utilization. This paper presents a new three-phase PV inverter topology which achieves CM current suppression by incorporating a modification, the addition of a diode, in the boost converter that precedes the three-phase inverter stage. The boost converter switching is coordinated with that of the inverter, which operates based on an adapted modulation strategy that practically eliminates the CM current when the PV array voltage is lower than a certain threshold. For higher PV array voltages, conventional modulation strategies can be applied, which are also shown to reduce the generated CM current by up to 90%. All the above strategies retain a high output voltage/current quality, while the added diode losses have a minor impact of approximately 0.3% on the converter efficiency. The effectiveness of the topology with respect to CM current suppression is demonstrated through simulations in MATLAB/Simulink and experimental results from a comprehensive laboratory setup.**

***Index Terms*—Transformerless, PV inverter, Boost converter, Ground leakage current, Common-mode current.**

I. Introduction

THE common mode (CM) voltage of a three-phase inverter is defined as the average of the output terminal voltages (v_a, v_b, v_c) with respect to a reference point in the inverter circuit, such as the negative DC-bus terminal:

$$v_{CM} = \frac{v_a + v_b + v_c}{3} \quad (1)$$

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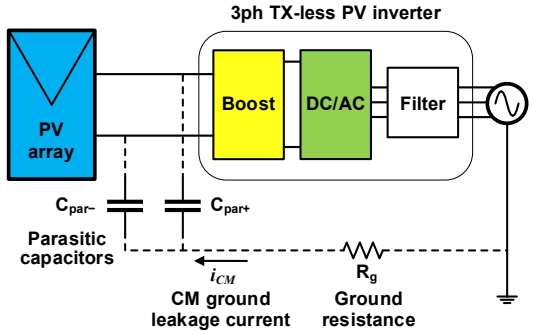

Fig. 1. Ground leakage current circulation path.

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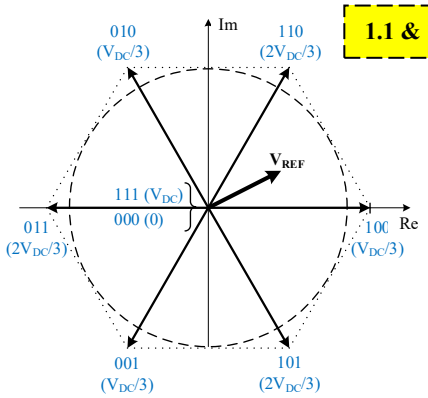

Fig. 2. Two-level inverter states and corresponding values of CM voltage w.r.t. the negative DC-bus terminal (in brackets).

In the absence of a transformer, fast variation of the photovoltaic (PV) inverter CM voltage gives rise to CM currents, due to the existence of parasitic capacitances between the solar cells of the PV array and the ground. CM currents flow through the grounded electric grid neutral as illustrated in Fig. 1 and cause deterioration of the PV cells and safety hazards [1, 2].

In order to reduce these currents, different approaches have been adopted in the literature. First, three-phase inverter modulation techniques that reduce the number and/or magnitude of CM voltage changes have been devised. Examples of such techniques can be found in [1 – 3]. However, these techniques on their own cannot eliminate the variation of the CM voltage, as the PV inverter inevitably has to apply different vectors, shown in Fig. 2, to generate the requested output voltage. Moreover, the proposed modulation techniques operate with low DC-bus voltage utilization and

heavily deteriorate the quality of the inverter output voltage and current. As a second step towards the enhancement of CM current suppression, modifications to the basic two-level [6 – 12] or multilevel [12 – 18] inverter topologies have been proposed. These are normally inspired from single-phase transformerless PV inverter topologies [13], which are designed to keep the CM voltage generated by the inverter approximately constant or isolate the PV array from the grid during certain inverter states. The single-phase transformerless PV inverter concepts, however, do not perform equally well when applied to three-phase inverters. This is because the latter utilize a higher number of states and generate more levels of CM voltage than their single-phase counterparts [14]. As a result, most proposed three-phase transformerless topologies do not achieve CM current elimination, while also incorporating several additional power semiconductors and achieving lower efficiencies than the two-level topology.

In addition to CM current suppression, a highly desirable feature for PV inverters is their capability of PV array voltage step-up. This enables operation with lower DC input voltage levels, thus extending energy harvesting over wider solar irradiance and temperature ranges. With regards to single-phase PV inverters, several topologies with step-up capability have been proposed in the literature, operating based on a number of different concepts regarding the waveform of their DC-link voltage [19]. Again, only a few of these concepts are applicable to three-phase inverters. For example, a three-phase inverter cannot operate according to the concept of having a rectified sinewave form of DC-link voltage which is then "unfolded" towards the grid. Besides, proposed current-source or Z-source three-phase topologies [20 – 25] require complex modulation strategies to suppress CM currents, which typically result in higher grid current distortion than voltage-source inverters. Finally, switched-capacitor converters are not suited for the power levels of three-phase PV inverters [26]. Consequently, PV voltage step-up for three-phase inverters is normally achieved by the addition of an input boost stage.

This paper proposes a three-phase PV inverter topology which achieves CM current suppression by applying a modification to the preceding boost converter and coordinating its operation with the inverter switching. The modification entails the addition of a diode, which is shown to only slightly increase the overall conversion losses. By means of a suitable modulation strategy, the proposed topology achieves complete CM current suppression when the PV array voltage is low (in the range or 100 – 150 V for a 400 V grid). For higher PV array voltage levels, the topology offers very significant CM current reduction, up to 90%, without compromising DC-bus voltage utilization or output voltage/current quality.

The paper is structured as follows: Section II presents the proposed topology and describes the method and mechanism for achieving CM current suppression. Section III presents an inverter modulation strategy for achieving CM current elimination when operating with low PV array voltages, discusses its boundaries and provides an alternative for higher PV voltages. Section IV presents simulation results in MATLAB/Simulink to illustrate the operation and performance of the proposed topology, and Section V includes experimental results from a laboratory setup. A discussion of the results and comparison with other topologies follows in Section VI, while Section VII concludes the paper.

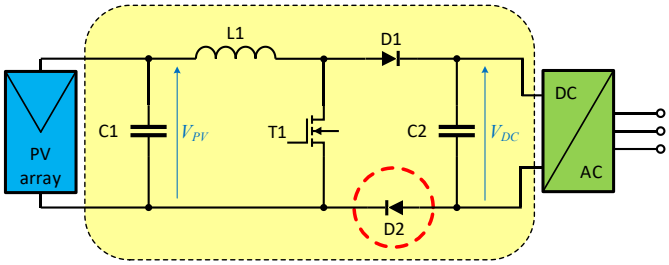

Fig. 3. Proposed extended boost converter-based three-phase transformerless PV inverter topology.

II. Proposed Topology and CM Current Suppression

The proposed topology is shown in Fig. 3 [27]. The inverter (DC/AC) block represents a conventional two-level inverter, while L1, T1 D1 and C2 form a conventional boost converter. The additional diode, D2, is inserted in the negative rail, between C2 and T1.

In contrast to other transformerless PV inverters, CM current suppression in the proposed topology is not based on an attempt to prevent or reduce the variation of the CM voltage; the inverter is allowed to utilise all the states in Fig. 2,

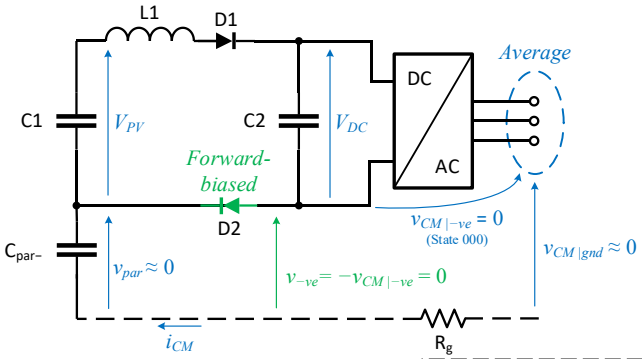

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Fig. 4. Voltage-to-ground equivalent circuits for: (a) inverter state 000 and T1 OFF, (b) other inverter states and T1 ON.

1.1 & 1.2: New figure.

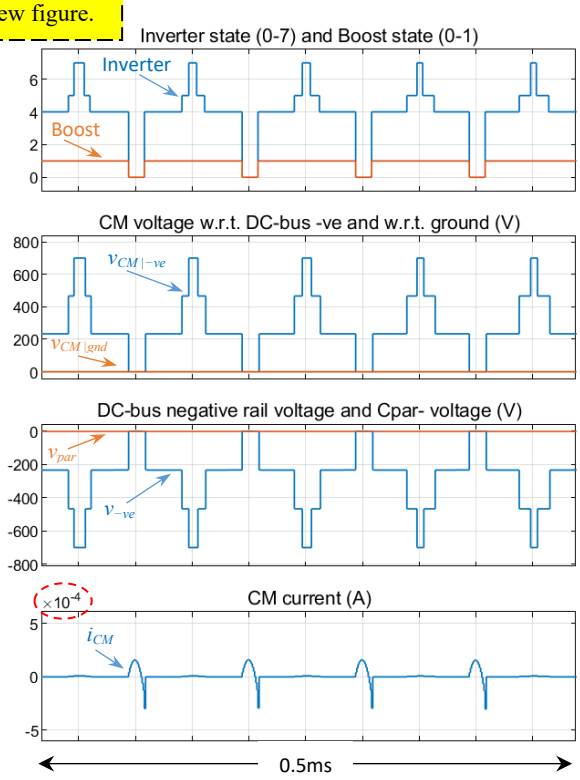


Fig. 5. Simulation results illustrating example waveforms of $v_{CM|-ve}$, $v_{CM|gnd}$, v_{par}, v_{-ve} and i_{CM} for different inverter and boost converter states (with reference to Fig. 4).

thus generating high-quality output voltage and current waveforms, but also all different levels of CM voltage. As detailed in [27], the proposed topology achieves CM current elimination (i.e., complete suppression) if the boost and inverter stages are switched in a coordinated manner. Namely, the boost stage switching element, T1, must be turned OFF when the inverter is in state 000 (see Fig. 2), whereas it must be turned ON during any other inverter state. Fig. 4 illustrates the corresponding equivalent circuits for the different converter states, while Fig. 5 presents a corresponding set of waveforms. Elimination of CM current is achieved because the voltage v_{par} across the parasitic capacitor C_{par-}, is maintained to approximately zero for all inverter states. This originates from the addition of D2, in combination with the fact that the voltage of the inverter's negative rail with respect to ground, v_{-ve}, is approximately equal to $-V_{CM}$ (shown in Fig. 2) for each inverter state. With reference to Fig. 4(a), which corresponds to the inverter state 000 ($V_{CM} = 0$), v_{-ve} is equal to 0 and D2 is conducting, thus v_{par} also becomes approximately zero (actually takes a slightly negative value due to the voltage drop across D2). In Fig. 4(b), on the other hand, given that the inverter is in one of the other states, v_{-ve} varies between $-V_{DC}/3$, $-2V_{DC}/3$ and $-V_{DC}$ (according to Fig. 2). Since these values are all negative while v_{par} is approximately equal to zero from state 000, D2 is reverse-biased and does not allow CM current to flow towards capacitor C_{par-}. It can be observed that diode D1 is also reverse-biased, which prevents CM current from flowing out from C_{par-}. Consequently, v_{par} retains its previous, approximately zero value and CM current is suppressed, as shown in the bottom two graphs of Fig. 5. The above analysis holds equally if capacitor C_{par+} is considered, while it does not hold if either D1 or D2 is missing, which is the case for the conventional boost converter.

1.2

1.2

III. Inverter PWM Strategy

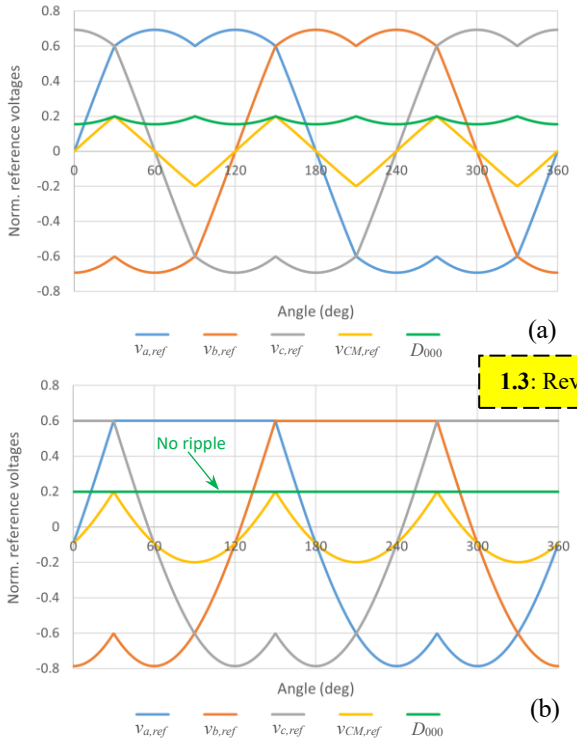
A. Stabilization of Boost Converter Duty Cycle and DC-Bus Voltage Control

According to the above proposed method, T1 is turned ON when the inverter is in any other state apart from 000. Consequently, the duty cycle, D, of the boost converter stage will be equal to the sum of duty cycles of all PV inverter states, except 000. Thus, if D_{000} is the duty cycle of state 000,

$$D = 1 - D_{000} \,. \tag{2}$$

Fig. 6(a) illustrates the variation of D_{000} over one fundamental cycle, assuming that the inverter is modulated using a carrier-based equivalent of space-vector modulation (SVPWM), and the modulation index, M, is equal to 0.8 (with $2/\sqrt{3}$ representing the limit of the linear range). It can be observed that the value of D_{000} varies, which can be shown to create severe oscillations on the boost inductor current and the DC-link voltage. Nevertheless, the variations of D_{000} can be eliminated by applying the following modulation strategy, which will be referred to as PWM_{000} [28]. The common-mode reference voltage, $v_{CM,ref}$, added to the three normalized sinusoidal inverter reference voltages, $v_{a/b/c,ref}$, is set to

$$v_{CM,ref} = 1 - \max\left(v_{a,ref}, v_{b,ref}, v_{c,ref}\right) - X \,, \tag{3}$$



1.3: Revised figure.

Fig. 6. Inverter reference voltages, common-mode reference voltage, and D_{000} for (a) classical SVPWM, and (b) proposed modulation strategy (PWM_{000}), respectively, for M = 0.8. PWM_{000} removes the ripple from the waveform of D_{000}.

1.3

where X is an offset that can be adjusted to vary the value of the boost converter duty cycle. This provides the boost converter with the degree of freedom required for performing Maximum Power Point Tracking (MPPT) of the PV array. Moreover, it can be shown that the variables X and D_{000} relate to each other with

$$D_{000} = X/2\,. \tag{4}$$

Fig. 6(b) illustrates the effect of adopting the PWM_{000} strategy, with X set to 0.4. It can then be observed that, according to (4), the value of D_{000} is equal to 0.2, thus, based on (2), D for the boost converter will be fixed to 0.8. Moreover, D_{000} is constant, thus avoiding the undesirable effects of duty cycle ripple on the operation of the boost converter.

It is noted at this point that X cannot be set to zero, as this would result in D being set to 1. Thus, the three voltage reference waveforms of PWM_{000} can never be fixed to ±1 for significant portions of the fundamental period, which is a characteristic of discontinuous PWM (DPWM) strategies. As a result, the proposed strategy retains the high output voltage quality of standard, continuous PWM strategies.

B. Limitations on the DC-Link Voltage and Inverter Modulation Index

The value of X (> 0) is limited by the requirement to avoid inverter over-modulation, which will occur if any of the three voltage reference waveforms exceeds ±1. It can be observed in Fig. 6(b) that the maximum value of these waveforms is equal to (1 – X), thus it can never exceed +1. Besides, their minimum value is given by the following expression:

$$v_{ref,min} = 1 - X - \sqrt{3}\,M \tag{5}$$

To ensure that $v_{ref,min}$ does not drop below −1, X must be restricted as follows:

$$X \leq 2 - \sqrt{3}\,M \tag{6}$$

Equivalently, it must hold that:

$$D \geq \frac{\sqrt{3}}{2}\,M \tag{7}$$

Equation (7) poses a constraint on the maximum value of M and the minimum value of D for the proposed topology, respectively. Namely, the proposed PV inverter cannot be operated with M approaching $2/\sqrt{3}$, which corresponds to the limit of the linear modulation region for common modulation strategies (e.g., THIPWM, SVPWM), because this would force the boost converter to operate with $D \approx 1$. Assuming that the highest acceptable value for D is close to 0.9, the maximum value for M for the PWM_{000} strategy is approximately equal to 1 (as for SPWM). In practice, this means that the inverter will have to operate with a higher DC-link voltage level than normal, by at least 15%.

C. Operation with Higher PV Array Voltages

The PWM_{000} modulation strategy proposed above achieves almost complete leakage current elimination, based on the mechanism presented in Section II. However, it results in high values of boost converter duty cycle, low values of inverter modulation index, and high DC-link voltages. Namely, D has to be in the range of 0.7 – 0.9, M is bounded to approximately 1 instead of $2/\sqrt{3}$, while V_{DC} must be higher than normal, which increases the inverter switching losses and the voltage stress on its components. The high values of D practically restrict the acceptable PV array voltages to a low range, around 100 – 150 V for a 400 V grid.

With the aim of extending the operating range of the proposed PV inverter, it is further proposed as an extension to the above method, to relax the condition for switching T1 by keeping it turned OFF not only during the 000 state, but also for portions of the adjacent inverter states. This reduces the value of D, thus allowing for higher PV array voltage levels, and brings M and V_{DC} towards their desired values. At the same time, though, it causes CM current flow, as it partially violates the principle for CM current suppression described in Section II. Nevertheless, if the above approach is applied to a limited extent, the RMS value of the resulting CM current can still be within the limit of 300 mA specified in [29].

As it will be shown in the following sections, the reduction of D can considerably extend the acceptable range of PV voltages and allow the inverter to operate with nominal values of M and V_{DC}. Furthermore, it decouples the inverter modulation index from the boost converter control, thus rendering unnecessary the modifications introduced in PWM_{000} for stabilising the value of D. Namely, D in this method is independent from D_{000}, thus is ripple-free and does need to abide by the constraint of (7). As a result, it is allowable to apply conventional modulation strategies, such as SVPWM, on the inverter in this case. The only requirement is for the boost converter (T1) PWM signal to be synchronized to the inverter PWM signals, e.g., by using a common carrier waveform, so that the overlap between the inverter state 000 and the T1 OFF state is maximized.

IV. Simulation Results

This section presents simulation results in MATLAB/Simulink, illustrating the operation of the proposed topology as a three-phase PV inverter rated at 5 kVA. The PV array is simulated as a DC source with parasitic capacitances to ground split equally between its positive and negative terminals, with $C_{par+} = C_{par-} = 250$ nF (giving a total of 100 nF per PV array kWp, in accordance with [7]). The value of L1 is set to 200 μH so that the boost stage operates in Continuous Current Mode (CCM), while the capacitances of C1 and C2 are set to 2 mF. The inverter is connected to a three-phase 400 V / 50 Hz grid through an LCL filter with $L_{f1} = L_{f2} =$ 5 mH and $C_{delta} = 1$ μF, while the grid is also assumed to have a phase inductance $L_{grid} = 0.5$ mH. Both converters are switched at 10 kHz. The ground resistance R_g, through which the leakage current returns to the grounded neutral of the grid (see Fig. 1), is assumed to have a value of 1 Ω.

A. Operation with Low PV Array Voltage – CM Current Elimination

This paragraph presents a first set of results that

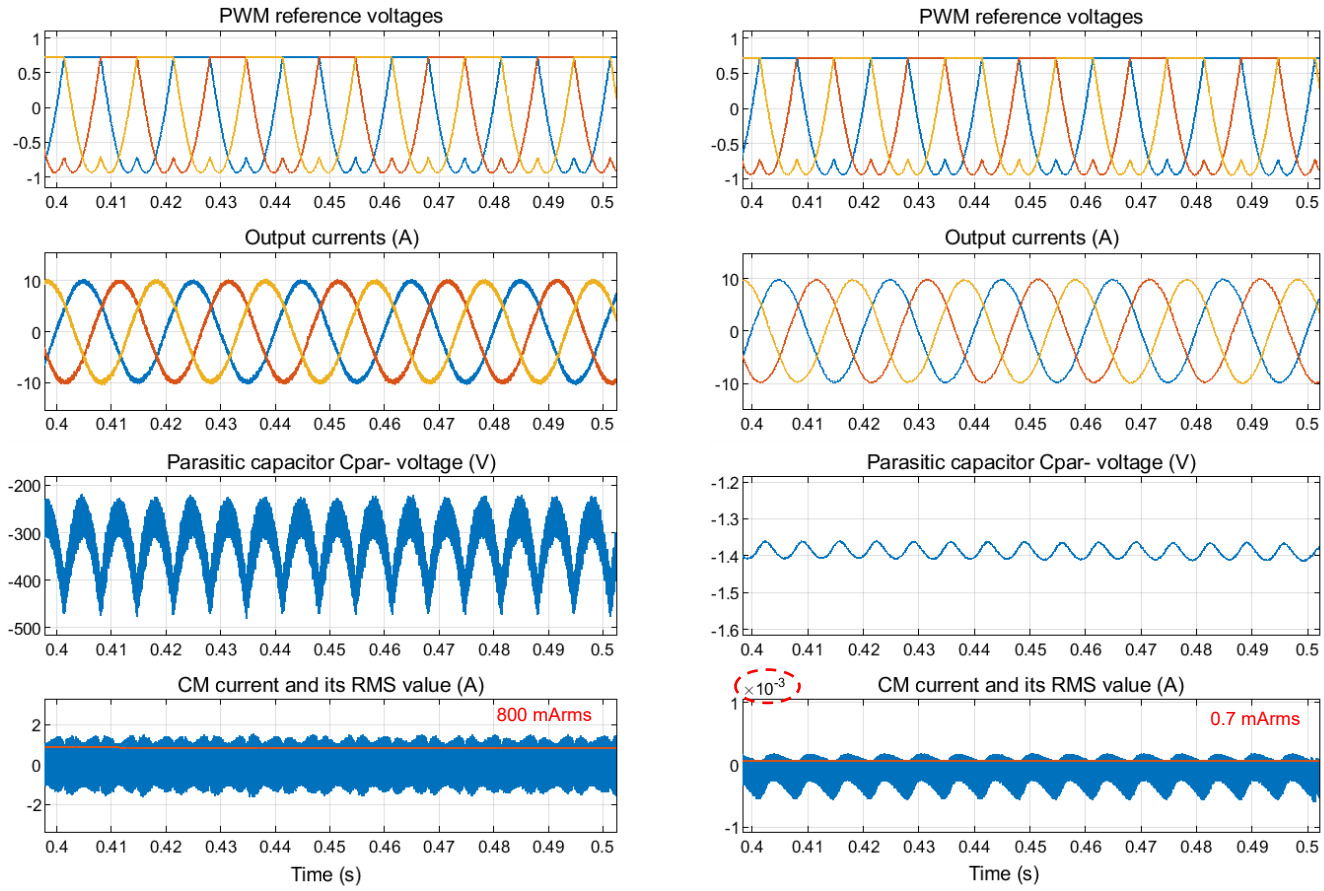


Fig. 7. Simulation results for V_{PV} = 100 V – Illustrating the effect of diode D2 and PWM_{000} modulation: (a) Waveforms for conventional boost converter, and (b) Waveforms for the proposed boost topology.

demonstrate the CM current elimination capability of the proposed topology when the PV array voltage is low, set to V_{PV} = 100 V. The converter is modulated with the PWM_{000} strategy, presented in Section III-A. For the given conditions, the inverter operates with a modulation index, M = 0.98 (85% of the linear region), the boost converter operates with a duty cycle, D = 0.86, and the resulting DC-link voltage is $V_{DC} \approx$ 685 V. To provide a benchmark, Fig. 7(a) presents a set of waveforms which corresponds to the case of using a conventional boost converter. The resulting CM current RMS value is 800 mA. Fig. 7(b) presents the same waveforms if the diode D2 is added. It can be observed in Fig. 7(b) that the parasitic capacitor C_{par-} voltage remains at approximately zero (actually −1.4 V, due to semiconductor voltage drops), as discussed in Section II. The CM current is negligible, with an RMS value of only 0.7 mA, which is three orders of magnitude lower than the previous case. To provide a further comparison, if SVPWM is used instead of PWM_{000}, with D2 in place, the resulting RMS value of CM current is 44 mA.

B. Operation with Higher PV Array Voltage

The simulation results presented in this paragraph illustrate the CM current suppression capability of the proposed converter when operating with higher PV array voltages and conventional values for D, M and V_{DC}, as discussed in Section III-*C*. The PV array voltage is now set to 400 V and the inverter is modulated using SVPWM. The inductance of L1 is also increased accordingly (to 800 µH) to ensure operation of the boost converter in CCM, without this affecting the generated CM current. The value of D is reduced to 0.35, and the inverter operates with M = 1.1 (95% of the linear region) and $V_{DC} \approx$ 615 V. Fig. 8(a) presents the waveforms corresponding to these conditions when using a conventional boost converter, which results in a CM current RMS value of 567 mA. Fig. 8(b) illustrates the respective waveforms for the proposed converter. The latter achieves a CM current RMS value of 213 mA, which is lower by 62.5%, and below the limit of 300 mA. Moreover, supplementary simulations showed that the value of V_{PV} that results in a CM current of 300 mA, is approximately 480 V for the simulated setup (which uses widely accepted values of 100 nF per PV array kWp for parasitic capacitance). This represents a very significant increment of 4.8 times (from 100 V to 480 V) in the acceptable PV array voltage, which greatly extends the applicability of the proposed topology.

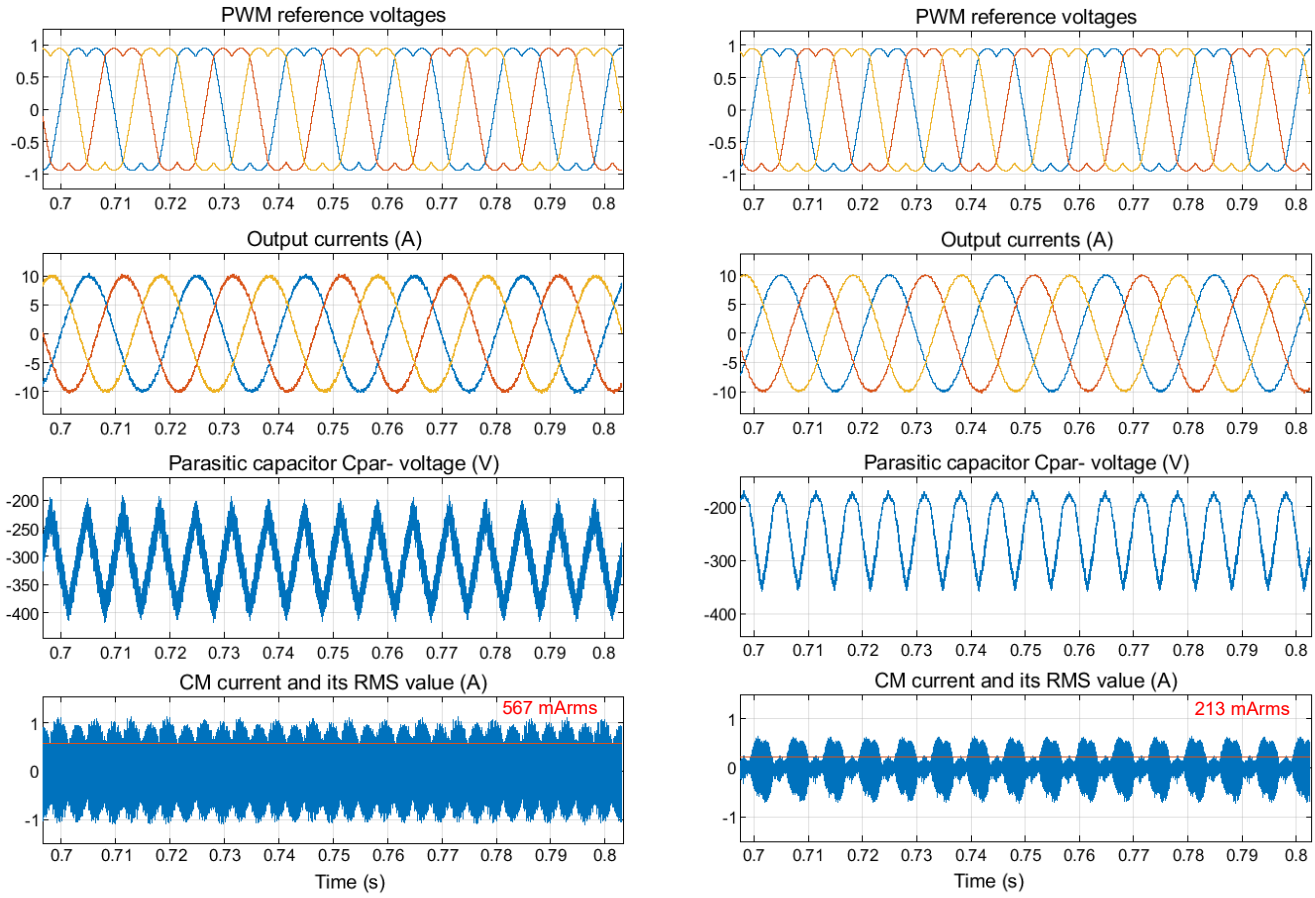


Fig. 8. Simulation results for V_{PV} = 400 V and conventional values for D, M and V_{DC} – Illustrating CM current reduction when operating with SVPWM: (a) Waveforms for conventional boost converter, and (b) Waveforms for the proposed boost topology.

V. Experimental Results

A laboratory-scale prototype of the proposed boost converter topology, shown in Fig. 9, was built to validate the presented analysis and confirm its capability for CM current reduction. The converter was tested as part of a complete experimental setup, which emulates the CM current generation mechanism of Fig. 1 in a controlled laboratory environment. The setup photograph and block diagram are presented in Figs. 10 and 11, respectively. The PV array in this setup was emulated by a DC power supply, feeding the proposed boost converter stage. A manual switch was connected in parallel to the added diode (D2) of the converter, so that it could be bypassed (i.e., shorted), to provide comparative results with a conventional boost converter. The output of the boost converter was connected to the DC bus of an Intelligent Power Module (IPM)-based three-phase inverter board including an electrolytic capacitor bank. The inverter output was connected to an isolation transformer through an LC filter. The isolation transformer leakage inductance, L_{TX}, represented the (LCL) filter grid-side inductance.

2.6: Revised table.

TABLE I
Main Parameters and Components of the Experimental Setup

Component	Model / Value
Converter power rating	1 kW
Boost converter max input current	10 A
Max DC-link voltage	200 V
Boost converter MOSFETs	2×STW25NM60N, in parallel
Boost converter diodes D1, D2	AIDW12S65C5
Inductor L1	805 µH
Capacitor C1	442 µF
Capacitor C2	50 µF
Inverter IPM	IRAM256-1067A
Inverter DC-link capacitance	2.35 mF
Inductors L_f	500 µH
Capacitors C_f	3.15 µF
Inductance L_{TX}	1 mH
Variac ratio	1:10
Resistance R_g	500 mΩ
Capacitance C_{par}	200 nF

The star point (neutral, N) of the primary transformer winding was wired back to the negative terminal of the DC power supply through an RC branch, with R = R_g representing the ground resistance and C = C_{par} representing the total parasitic capacitance of the PV array. It is noted that using a single parasitic capacitor is equivalent to having two capacitors of half the total value, connected at the positive and negative power supply terminals, as shown in Fig. 1. Finally, the secondary of the isolation transformer was connected to the grid (400 V / 50 Hz) through a variable autotransformer (Variac). The types/values of the main components of the experimental setup are listed in Table I.

Closed-loop grid current control in the synchronous reference frame and DC-bus voltage control were performed for the inverter and boost converter, respectively, based on voltage/current measurements from a laboratory measurements board. Both converters were switched at 20 kHz, while the control interrupt rate was set to 40 kHz. The controllers and modulators were implemented on a Texas Instruments LAUNCHXL-F28069M board, programmed through a corresponding Simulink model by means of MATLAB/Simulink embedded coder. Moreover, monitoring and references were provided through serial connection with a PC running a host Simulink model.

Two cases are considered below: 1) Operation with low PV array voltages and ground leakage current elimination using PWM_{000}, and 2) Operation with higher PV array voltages and ground leakage current suppression using SVPWM. In Fig. 12 the boost converter is supplied with V_{in} = 16 V and operates with D = 80%. The resulting DC-link voltage is V_{DC} = 70 V. The inverter is modulated with PWM_{000} and outputs a current of 1 A with unity power factor (PF) towards the primary side of the isolation transformer, whose voltage is approximately 40 V (line-line). Fig. 12(a) illustrates an inverter output voltage and current, the capacitor C_{par} voltage and the CM current waveforms, for the case of a conventional boost converter (i.e., with diode D2 shorted). It can be observed that the C_{par} voltage and CM current waveforms resemble the respective waveforms of Fig. 7(a): they have a fundamental frequency of 150 Hz and include both 150 Hz and PWM-frequency components. The RMS value of the CM current in this case is 67.8 mA. Fig. 12(b) illustrates the same waveforms for the modified boost converter. It can be seen that the CM current reduces radically, with its RMS value dropping to 0.52 mA, while the capacitor voltage remains approximately constant and equal to a small negative value, as it is also shown in Fig. 7(b).

1.8 & 2.4

Figs. 13 and 14 refer to the same conditions as Fig. 12(b), but aim to demonstrate different aspects of the converter operation. Namely, Fig. 13 captures the CM voltage (v_{CM}), capacitor C_{par} voltage (v_{par}), DC-bus negative rail voltage (v_{-ve}) and CM current (i_{CM}) waveforms (see Fig. 11), to verify the CM current suppression mechanism of Section II.

1.8 & 2.4

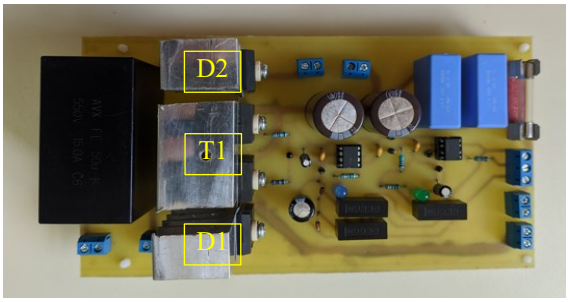


Fig. 9. Proposed boost converter stage experimental prototype. Inductor shown in Fig. 10.

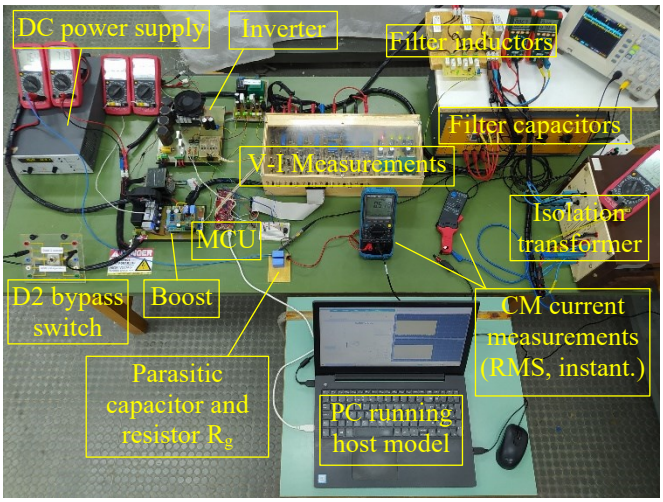


Fig. 10. Photograph of the experimental setup.

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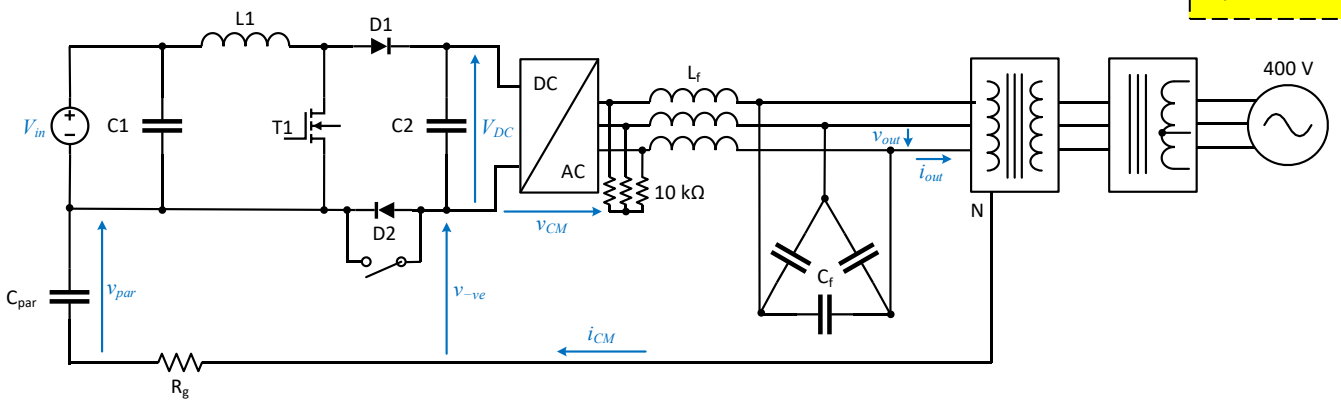

Fig. 11. Block diagram of the experimental setup.

1.8 & 2.4: Revised figure.

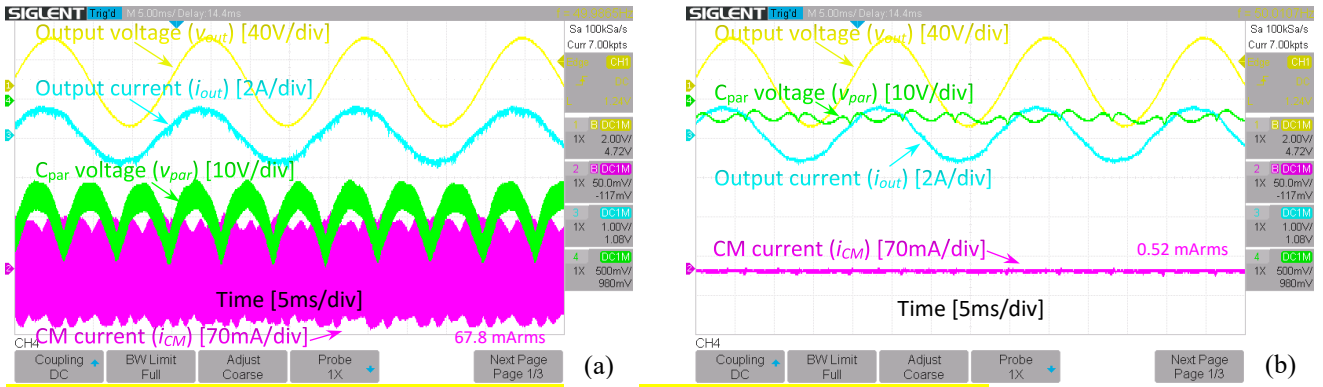

Fig. 12. Output voltage, output current, capacitor C_{par} voltage and CM current waveforms while operating with PWM_{000}, V_{in} = 16 V and V_{DC} = 70 V, (a) without diode D2, and (b) with diode D2.

1.8 & 2.4: New figures.

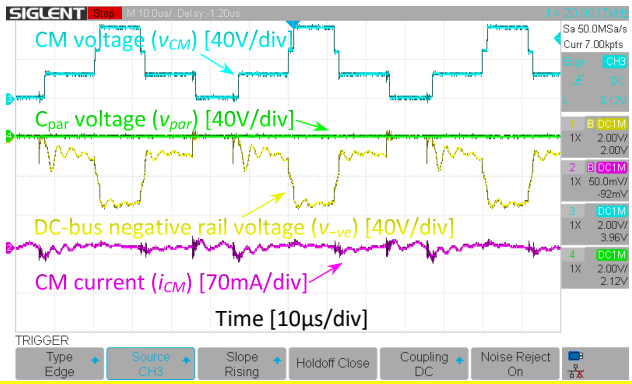

Fig. 13. CM voltage, capacitor C_{par} voltage, DC-bus negative rail voltage and CM current waveforms while operating with PWM_{000}, V_{in} = 16 V and V_{DC} = 70 V, with diode D2.

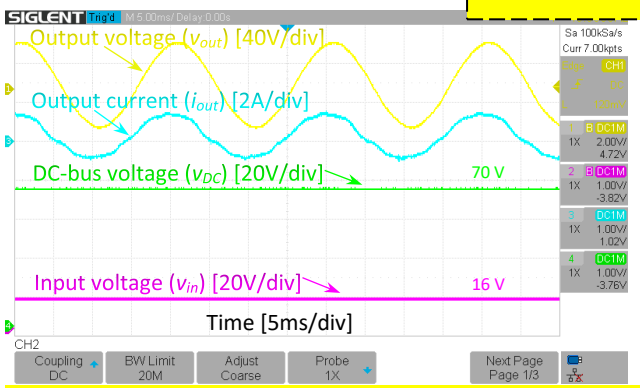

Fig. 14. Output voltage, output current, input voltage and DC-bus voltage while operating with PWM_{000}, V_{in} = 16 V and V_{DC} = 70 V, with diode D2.

1.8 & 2.4: Revised figure.

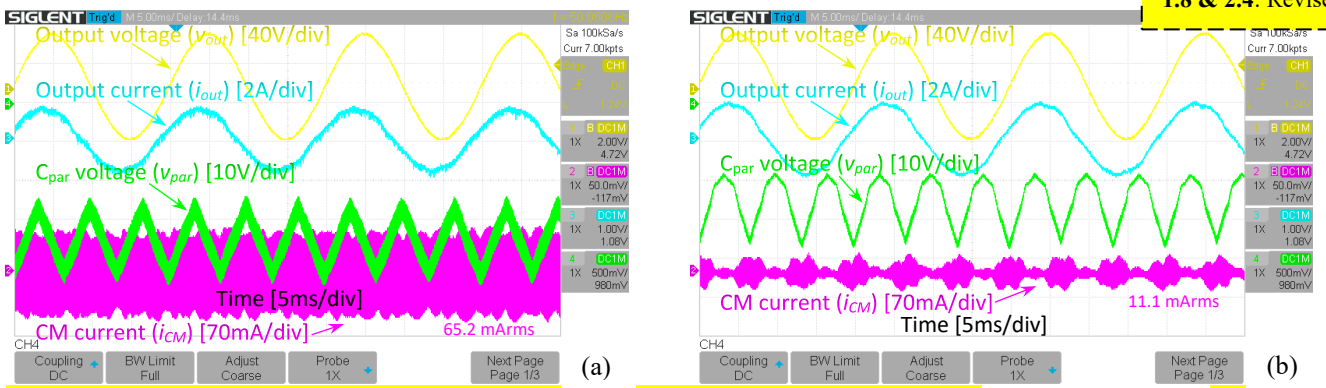

Fig. 15. Output voltage, output current, capacitor C_{par} voltage and CM current waveforms while operating with SVPWM, V_{in} = 40 V and V_{DC} = 70 V, (a) without diode D2, and (b) with diode D2.

1.8 & 2.4 **1.6**

The waveforms match those of Fig. 5, with the key observation being that v_{par} is consistently higher or equal to v_{-ve}, which leads to reverse biasing of diode D2 and CM current suppression. Fig. 14, on the other hand, illustrates the input (v_{in}) and DC-bus (v_{DC}), verifying that they are ripple-free, as discussed in Section III-A.

2.6

In Fig. 15 the boost converter is supplied with V_{in} = 40 V and operates with D = 48%. The DC-link voltage, transformer primary voltage and inverter output current are the same as above, but the inverter in this case is modulated with (the carrier-based equivalent of) SVPWM. Fig. 15(a) refers to a conventional boost converter and its results resemble those of Fig. 8(a). The RMS value of the CM current in this case is 65.2 mA. Fig. 15(b) illustrates the same waveforms for the modified boost converter. Again, the CM current reduces significantly, with its RMS value dropping to 11.1 mA, while the parasitic capacitor voltage ripple reduces, as also seen in Fig. 8(b).

Fig. 16 presents further simulation and experimental results, illustrating the effect of inserting the diode D2 in the boost converter, as a function of the voltage ratio V_{PV} / V_{DC}. The inverter is modulated using conventional SVPWM with M = 1.1 (95% of the linear range), thus representing operation with a typical DC-bus voltage level. The aim of the figure is to illustrate the percentage reduction of RMS CM leakage current achieved over the entire range of practical PV array

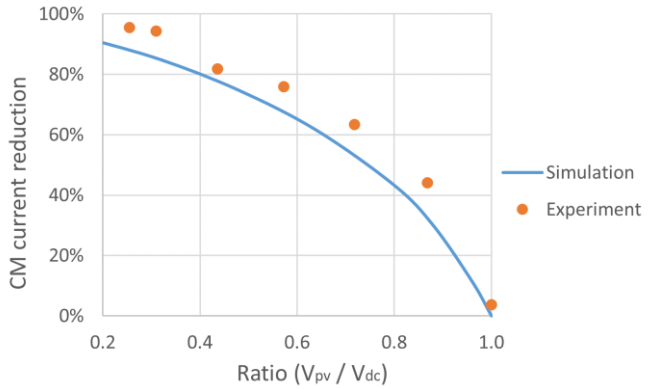

Fig. 16. Simulation and experimental results illustrating the percent reduction of RMS CM current by the insertion of diode D2, as a function of (V_{PV} / V_{DC}).

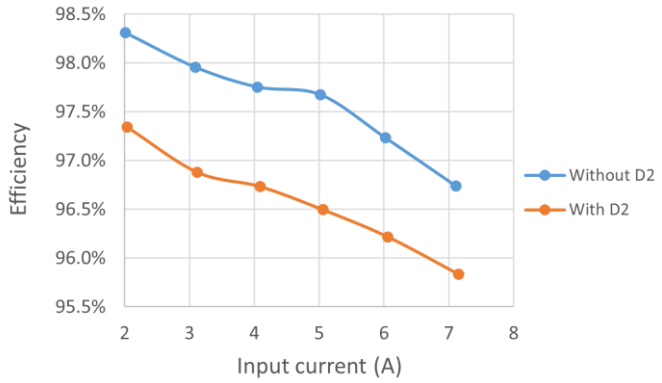

Fig. 17. Experimental results comparing the boost converter efficiency with/without diode D2.

voltages, which can be as low as 0.2 × V_{DC} up to 1 × V_{DC} (or more). The horizontal axis is the ratio V_{PV} / V_{DC}, because this (and not actual values of V_{PV}, V_{DC}) determines the duty cycle of the boost converter and thus the percentage reduction of the RMS CM current. It can be observed from Fig. 16 that the proposed topology can achieve very high CM current reduction, above 90%, even with conventional SVPWM, for voltage ratios in the range of 0.2. The reduction drops to 50% for ratios in the order of 0.7 – 0.8 and to 0% when the ratio is equal to 1 (or more). Moreover, the discrepancy between the simulation and experimental results is due to the fact that the former assumed an ideal boost converter, whereas the latter were obtained from the converter prototype of Fig. 9. The ideal converter achieves PV voltage step-up using the theoretical values of D (= 1 – V_{PV} / V_{DC}), whereas an actual converter operates with higher values of D (for the same input and output voltages) to compensate for its losses.

These higher values increase the degree of CM current suppression, as explained in Section III. Thus, the line corresponding to simulation results in Fig. 16 represents the absolute minimum CM current reduction, while actual converters will achieve higher percentages, as shown by the respective experimental results.

Finally, experiments were conducted to quantify the effect of the insertion of diode D2 on the converter's efficiency. Given that the operation of the three-phase inverter stage is not affected by this modification, these experiments focused on the efficiency of the boost converter stage. Fig. 17 presents measured efficiency values as a function of input current while operating the boost converter with/without diode D2, with an input voltage V_{in} of 70 V and an output voltage V_{DC} of 180 V. It can be observed that the average efficiency reduction in these conditions is approximately 1%. Nevertheless, the efficiency reduction is expected to be less while operating at higher input-output voltages, as explained in the following section.

VI. Discussion

The insertion of diode D2 in the proposed topology will introduce additional conduction, but not switching losses to the boost stage. This is because D1 and D2 are connected in series with regards to the main power circuit, thus sharing the converter output voltage, which results in the generation of approximately the same overall diode reverse recovery losses. It is noted at this point that D2 must retain the rating of D1, since it is reverse-biased with the full DC-link voltage across it during inverter state 111, as shown in Fig. 5 (state 7). The experimental results using the setup of Fig. 17 show a 1% efficiency drop at a converter output of approximately 180 V – 2.75 A (500 W). Given that the conduction losses only depend on the converter output current (and not the output voltage), they are expected to be similar for a converter that operates with a DC-link voltage of 600 V and the same output current (600 V – 2.75 A – 1650 W). The corresponding efficiency drop will be 0.3% in these conditions, which are representative for the case of connecting directly to a 400 V grid. For higher-power converters, a smaller efficiency drop can be expected, as the losses do not normally increase at the same rate as the nominal power of a converter (i.e., higher-power converters tend to be more efficient) [30]. It is also noted that reduction of the additional losses can be achieved if diodes D1 and D2 are replaced by MOSFETs as in the synchronous boost topology [31].

2.2

2.3

The proposed transformerless PV inverter topology therefore features high efficiency, comparable to that of a series connection of a conventional boost converter and a three-phase inverter. Moreover, the converter design (switches-diodes, PV-side and DC-link capacitor, boost inductor, etc.) [32 – 34] and control [35] are identical to the conventional converter's, since the added diode does not affect the differential-mode operation of the circuit. It is therefore important that the above efficiency is achieved without significantly increasing the component count/size of the power circuit and the complexity of the controller, or adversely affecting the quality of the output voltage. As also mentioned in Section I, this is not the case for the majority of past-proposed topologies. Table II presents a comparative summary of different concepts applied to three-phase transformerless PV inverters. It can be observed that the proposed topology achieves similar efficiency to existing alternatives, which however require several extra semiconductor switches (with

1.4 & 1.5

TABLE II
COMPARISON WITH OTHER THREE-PHASE TRANSFORMERLESS PV INVERTERS INCLUDING A BOOST STAGE

Topology / Topology family[1]	No. of switches[2,3]	No. of diodes[2]	Size of passive components	DC bus voltage utilization	Output voltage quality	Efficiency[4]	CM current RMS	Comments
Proposed	7	2	Normal	Moderate (PWM_{000}) / Normal (SVPWM)	Normal	94.9% – 95.3%	< 10 mA to > 300 mA	1) Efficiency lower by 0.3% compared to two-level inverter with standard SVPWM, 2) CM current depending on V_{PV}.
Two-level inverter, with standard SVPWM	7	1	Normal	Normal	Normal	95.2% – 95.6%	990 mA – 1530 mA	Efficiency and CM current values based on [3].
Two-level inverter, with modified modulation	7	1	Normal	Low / Normal	Low	95.3% – 96.4%	460 mA – 620 mA	Efficiency and CM current values based on [3].
Two-level inverter, with DC bypass	8 – 11	1 – 3	Normal	Normal	Normal	94.8% – 97.1%	192 mA – 544 mA	1) Efficiency based on [7], considering only semiconductor losses of inverter stage, 2) CM current depending on topology, C_{par} and modulation.
Two-level inverter, with AC bypass	10	13	Normal	Normal	Low / Moderate	≈ 95%	200 mA – 240 mA	1) Efficiency claimed to be similar to conventional two-level inverter [36], 2) CM current depending on topology, C_{par} and modulation.
Two-level, four-wire inverter	9	1	Normal	Low / Normal	Low	*Not reported*	< 300 mA	CM current based on [37].
NPC converter	13	7	Small	Moderate	High	96.5 – 98.1%	Negligible	1) Assuming connection of NP to grid neutral, 2) Power semiconductors rated at half voltage than the two-level inv., 3) Efficiency based on [13, 15, 16].
Modified CHB converter	18 – 21	3	Large	Normal	Low	≈ 96.5%	< 300 mA	1) Efficiency based on [18], 2) Requires three independent PV strings and three boost converters.
Flying capacitor converter	13	1	Large	Normal	Low	*Not reported*	120 mA	CM current based on [38].
Z-source converter	7 – 8	1	Large	Low / Moderate	Low	96 – 98%	15 – 300 mA	Efficiency and CM current based on [20, 22].

[1]Each row covers different variants based on the relevant concept. [2]Including the boost stage. [3]Switches include anti-parallel diodes. [4]Except for Z-source converters, efficiencies refer to the inverter stages, as reported in the literature.

their gate drivers), diodes, and/or passive components. Additionally, the modulation strategies developed for these topologies normally result in low DC-link voltage utilization (i.e., high DC-link voltage) and low quality of output voltage. This is normally because the inverter is operated without making use of certain states that generate very low / high values of CM voltage (such as states 000 and 111 in Fig. 2). In addition to the undesirable effects on the grid current (i.e., higher ripple due to the bipolar-type of modulation and/or high DC-link voltage), it is noted that high DC-link voltage also has a negative impact on the efficiency of the boost converters of these topologies, which is not considered in any of the relevant studies.

Furthermore, the proposed concept can be applied to PV inverters supplied by two or more boost converters performing MPPT for independent PV arrays, as is commonly desirable for three-phase PV inverters (which normally have higher power ratings than single-phase inverters). This is not an option for certain other alternatives, such as Z-source PV inverters, which rely on the inverter modulation (shoot-through state) to boost their PV array voltage.

Among the different PV inverter concepts presented in Table II, the NPC inverter (with its variants) offers several advantages, such as high efficiency and output voltage quality, as well as CM current elimination. Nevertheless, it requires an increased number of switches and gate drivers, which increases the power circuit complexity and cost. Moreover, in order to achieve CM current elimination, the NPC inverter requires a low-inductance connection to the grid's neutral [12], which may not be always available. A neutral connection is commonly not available in other applications, either, where the proposed concept can be applicable. An example is three-phase AC motor drives (that require DC voltage step-up), for reducing CM currents that cause motor bearing failures [26, 39, 40].

The proposed topology may not exhibit the above-discussed drawbacks of existing alternatives, but a restriction remains for it in relation to the maximum PV array voltage. This originates from the fact that the topology's CM current suppression mechanism relies on the operation of its boost stage. Thus, the PV array voltage is required to be low, so that it can be stepped up by operating the boost stage as described in Sections II-III. In case that the PV array voltage is already high, then the proposed topology achieves low CM current suppression, as shown in Fig. 16. Hence, the proposed topology is suited for installations with relatively low PV array voltages, for example up to 480 V for connection to a 400 V grid, according to Section IV-B.

Finally, it is noted that the voltage of the negative terminal of the PV array with respect to ground, i.e., the voltage of the parasitic capacitor C_{par-}, is negative in the proposed converter, as it can be seen in Figs. 7, 8, 12 and 15. Such negative voltages have been associated with deterioration of PV cells due to the Potential-Induced Degradation (PID) effect [41]. Nevertheless, the PID effect is strongly dependent on the PV array voltage, or more accurately on the voltages of the PV array terminals w.r.t. ground. The effect can be intense for high-voltage PV arrays (600 – 1000 V), for which a boost stage is not required or operates only at low-irradiance conditions, which is not the case in the present study. Moreover, the applicable PV array voltages of up to 480 V, as well as the negative PV array terminal voltages that vary between approximately 0 and −400 V, as shown in Figs. 7(b) and 8(b), are safe with regards to the PID effect.

2.2

VII. Conclusion

A new three-phase transformerless PV inverter topology with a modified boost stage and its operating principle were presented in this paper. The topology can offer significant reduction of CM ground leakage current, especially for installations with low PV array voltages. Namely, by means of the proposed PWM_{000} strategy, it achieves CM current elimination when the PV array voltage is in the range of 100 – 150 V for a 400 V grid. For higher PV array voltages, up to approximately 480 V, it offers CM current reduction between 40% and 90% as compared to a conventional boost converter and three-phase two-level inverter configuration, while retaining a high efficiency of only around 0.3% lower than the latter. Compared to other alternatives, the advantage of the proposed topology is that CM current suppression is offered without requiring several additional components, deteriorating the output current quality, or operating with excessive DC-link voltages. Finally, the topology does not require a connection to the neutral of the electric grid, which renders it suitable for incorporation in other applications suffering from CM leakage currents where a neutral connection is not available, such as three-phase motor drives.

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References

[1] M. C. Cavalcanti, K. C. de Oliveira, A. M. de Farias, F. A. S. Neves, G. M. S. Azevedo and F. C. Camboim, "Modulation Techniques to Eliminate Leakage Currents in Transformerless Three-Phase Photovoltaic Systems," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 4, pp. 1360-1368, April 2010.

[2] E. Serban, C. Pondiche and M. Ordonez, "Modulation Effects on Power-Loss and Leakage Current in Three-Phase Solar Inverters," in *IEEE Transactions on Energy Conversion*, vol. 34, no. 1, pp. 339-350, March 2019.

[3] J. Xu, J. Han, Y. Wang, S. Habib and H. Tang, "A Novel Scalar PWM Method to Reduce Leakage Current in Three-Phase Two-Level Transformerless Grid-Connected VSIs," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 5, pp. 3788-3797, May 2020.

[4] J. Lee and J. -W. Park, "Selection of PWM Methods for Common-Mode Voltage and DC-Link Capacitor Current Reduction of Three-Phase VSI," in *IEEE Transactions on Industry Applications*, vol. 59, no. 1, pp. 1064-1076, Jan.-Feb. 2023.

1.9

[5] Z. Li, Y. Guo, J. Xia, Y. Duan and X. Zhang, "Modified Synchronized SVPWM Strategies to Reduce CMV for Three-Phase VSIs at Low Switching Frequency," in *IEEE Transactions on Industry Applications*, vol. 56, no. 5, pp. 5245-5256, Sept.-Oct. 2020.

[6] T. K. S. Freddy, N. A. Rahim, W. Hew and H. S. Che, "Modulation Techniques to Reduce Leakage Current in Three-Phase Transformerless H7 Photovoltaic Inverter," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 322-331, Jan. 2015.

[7] A. K. Gupta, H. Agrawal and V. Agarwal, "A Novel Three-Phase Transformerless H-8 Topology with Reduced Leakage Current for Grid-Tied Solar PV Applications," in *IEEE Transactions on Industry Applications*, vol. 55, no. 2, pp. 1765-1774, Apr. 2019.

[8] D. Ronanki, P. H. Sang, V. Sood and S. S. Williamson, "Comparative assessment of three-phase transformerless grid-connected solar inverters," *2017 IEEE International Conference on Industrial Technology (ICIT)*, Toronto, ON, 2017, pp. 66-71.

[9] T.-D. Duong, M.-K. Nguyen, T.-T. Tran, D.-V. Vo, Y.-C. Lim, and J.-H. Choi, "Topology Review of Three-Phase Two-Level Transformerless Photovoltaic Inverters for Common-Mode Voltage Reduction," *Energies*, vol. 15, no. 9, p. 3106, Apr. 2022.

[10] R. Rahimi, M. Farhadi, G. R. Moradi, B. Farhangi and S. Farhangi, "Three-Phase Filter-Clamped Transformerless Inverter for Grid-Connected Photovoltaic Systems with Low Leakage Current," in *IEEE Transactions on Industry Applications*, in press, 2020.

1.9

[11] A. Hota and V. Agarwal, "A New Three-Phase Inverter Topology for Reducing the dv/dt and Peak-to-Peak Value of Common Mode Voltage," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 12, pp. 11979-11986, Dec. 2022.

[12] T. Kerekes, R. Teodorescu, M. Liserre, C. Klumpner and M. Sumner, "Evaluation of Three-Phase Transformerless Photovoltaic Inverter Topologies," in *IEEE Transactions on Power Electronics*, vol. 24, no. 9, pp. 2202-2211, Sept. 2009.

[13] M. N. H. Khan, M. Forouzesh, Y. P. Siwakoti, L. Li, T. Kerekes and F. Blaabjerg, "Transformerless Inverter Topologies for Single-Phase Photovoltaic Systems: A Comparative Review," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 805-835, March 2020.

[14] V. Sonti, S. Jain and V. Agarwal, "Analysis of Terminal Voltage in Single-Phase Extended Three-Phase Transformerless PV Inverter Topologies," in *IEEE Journal of Photovoltaics*, vol. 10, no. 1, pp. 226-235, Jan. 2020.

[15] Y. Wang and F. Wang, "Novel Three-Phase Three-Level-Stacked Neutral Point Clamped Grid-Tied Solar Inverter with a Split Phase Controller," in *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2856-2866, June 2013.

[16] K. Kim, S. Lee, W. Cha and B-H Kwon, "Three-level three-phase transformerless inverter with low leakage current for photovoltaic power conditioning system," in *Solar Energy*, vol. 142, pp. 243-252, Jan. 2017.

[17] X. Guo, J. Zhou, R. He, X. Jia and C. A. Rojas, "Leakage Current Attenuation of a Three-Phase Cascaded Inverter for Transformerless Grid-Connected PV Systems," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 676-686, Jan. 2018.

[18] P. K. Chamarthi, A. Al-Durra, T. H. M. EL-Fouly and K. A. Jaafari, "A Novel Three-Phase Transformerless Cascaded Multilevel Inverter Topology for Grid-Connected Solar PV Applications," in *IEEE Transactions on Industry Applications*, vol. 57, no. 3, pp. 2285-2297, May-June 2021.

[19] W. Liu, K. Niazi, T. Kerekes and Y. Yang, "A Review on Transformerless Step-Up Single-Phase Inverters with Different DC-Link Voltage for Photovoltaic Applications," in *Energies*, MDPI, Open Access Journal, vol. 12 (19), pp. 1-17, Sept. 2019.

[20] N. Noroozi and M. R. Zolghadri, "Three-Phase Quasi-Z-Source Inverter with Constant Common-Mode Voltage for Photovoltaic Application," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4790-4798, June 2018.

[21] N. Noroozi, M. Yaghoubi and M. R. Zolghadri, "A Modulation Method for Leakage Current Reduction in a Three-Phase Grid-Tie Quasi-Z-Source Inverter," in *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5439-5450, June 2019.

[22] T. -D. Duong, M. -K. Nguyen, T. -T. Tran, Y. -C. Lim, J. -H. Choi and C. Wang, "Modulation Techniques for a Modified Three-Phase Quasi-Switched Boost Inverter With Common-Mode Voltage Reduction," in *IEEE Access*, vol. 8, pp. 160670-160683, 2020.

[23] M. Kamalirad, H. Iman-Eini, B. Farhangi and S. Bacha, "A Reliable Three-Phase Transformerless Grid-Connected PV Inverter with Inductive DC Link," in *IEEE Journal of Photovoltaics*, vol. 8, no. 5, pp. 1305-1312, Sept. 2018.

[24] E. Lorenzani, F. Immovilli, G. Migliazza, M. Frigieri, C. Bianchini and M. Davoli, "CSI7: A Modified Three-Phase Current-Source Inverter for Modular Photovoltaic Applications," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 5449-5459, July 2017.

1.9 [25] A. Singh and B. Mirafzal, "An Efficient Grid-Connected Three-Phase Single-Stage Boost Current Source Inverter," in *IEEE Power and Energy Technology Systems Journal*, vol. 6, no. 3, pp. 142-151, Sept. 2019.

[26] A. Hota, M. M. Qasim, J. L. Kirtley and V. Agarwal, "Novel Switched Capacitor Boost Inverter Configuration for Three-Phase Induction Motor Driven Home Appliances," in *IEEE Transactions on Industry Applications*, vol. 57, no. 2, pp. 1450-1458, March-April 2021.

[27] G. I. Orfanoudakis, E. Koutroulis, M. A. Yuratich and S. M. Sharkh, "A three-phase transformerless Boost inverter for the reduction of common-mode leakage current in photovoltaic applications," *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, Ghent, Belgium, 2021.

[28] G. I. Orfanoudakis, E. Koutroulis, M. A. Yuratich and S. M. Sharkh, "Extended Boost PV inverter topology for the reduction of common-mode leakage current in three-phase applications," *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, Lyon, France, 2020, pp. 1-10.

[29] *Automatic Disconnection Device Between a Generator and the Public Low-Voltage Grid*, German National Standard DIN VDE V 0126-1-1, Aug. 2013.A.

2.3 [30] S. Yilmaz and F. Dincer, "Impact of inverter capacity on the performance in large-scale photovoltaic power plants – A case study for Gainesville, Florida," in *Renewable and Sustainable Energy Reviews*, vol. 79, pp. 15-23, May 2017.

[31] Rodriguez, A. Vazquez, M. R. Rogina and F. Briz, "Synchronous Boost Converter with High Efficiency at Light Load Using QSW-ZVS and SiC MOSFETs," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 386-393, Jan. 2018.

1.4 [32] T. Messo, J. Jokipii, J. Puukko and T. Suntio, "Determining the Value of DC-Link Capacitance to Ensure Stable Operation of a Three-Phase Photovoltaic Inverter," in *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 665-673, Feb. 2014, doi: 10.1109/TPEL.2013.2255068

[33] A. Hayat, D. Sibtain, A. F. Murtaza, S. Shahzad, M. S. Jajja, and H. Kilic, "Design and Analysis of Input Capacitor in DC–DC Boost Converter for Photovoltaic-Based Systems," *Sustainability*, vol. 15, no. 7, p. 6321, Apr. 2023, doi: 10.3390/su15076321.

[34] B. Hauke, "Basic Calculation of a Boost Converter's Power Stage," Texas Instruments, App. Note SLVA372D, Nov. 2022.

[35] F. Blaabjerg and D. M. Ionel (Eds.), Renewable Energy Devices and Systems with Simulations in MATLAB® and ANSYS®, 1st ed., CRC Press, 2017. 1.5

[36] V. L. Srinivas, B. Singh and S. Mishra, "Enhanced Power Quality PV Inverter With Leakage Current Suppression for Three-Phase SECS," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 6, pp. 5756-5767, June 2022.

[37] X. Guo, R. He, J. Jian, Z. Lu, X. Sun and J. M. Guerrero, "Leakage Current Elimination of Four-Leg Inverter for Transformerless Three-Phase PV Systems," in *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1841-1846, March 2016.

[38] X. Guo *et al*., "Leakage Current Suppression of Three-Phase Flying Capacitor PV Inverter With New Carrier Modulation and Logic Function," in *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2127-2135, March 2018.

[39] E. Robles, M. Fernandez, J. Andreu, E. Ibarra and U. Ugalde, "Advanced power inverter topologies and modulation techniques for common-mode voltage elimination in electric motor drive systems," in *Renewable and Sustainable Energy Reviews*, vol. 140, April 2021.

[40] Y. Xu, Y. Liang, X. Yuan, X. Wu and Y. Li, "Experimental Assessment of High Frequency Bearing Currents in an Induction Motor Driven by a SiC Inverter," in *IEEE Access*, vol. 9, pp. 40540-40549, 2021.

[41] W. Luo et al, "Potential-induced degradation in photovoltaic modules: a critical review," in *Energy Environ. Sci.*, vol. 10, pp. 43-68, 2017. 2.2

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In his industrial career he has worked widely in electro-mechanical systems and instrumentation for downhole exploration equipment. He has worked intensively for over twenty years on development and commercialization of specialist permanent magnet machines up to 1500kW: motors, generators and integrated subsea thrusters, with associated development and commercialization of variable speed drives and vector control algorithms. He holds 65 patents and has published 20 papers and a book.

Dr Yuratich was the winner of The Engineer Energy Innovation and Technology Award 2008 for integrated thrusters, and twice winner of Society of Petroleum Engineer technology awards. He is a Chartered Physicist.