A Soft-switched Multi-port Converter for PV/Supercapacitors Hybrid Systems enabling Frequency Response Services

Sivakrishna Karpana, Efstratios Batzelis, *Senior Member, IEEE,* Georgios Kampitsis, *Member, IEEE,* Suman Maiti, *Member, IEEE,* Chandan Chakraborty, *Fellow, IEEE*

***Abstract*—Supercapacitors (SC) have superior performance for frequency response services in grid-tied photovoltaic (PV) systems owing to high power density. However, their variable voltage makes PV/SC hybridization quite challenging. The current body of literature lacks solutions that offer either a substantial step-up gain for the SC ports when controlled as a voltage source or a significant capability for high current discharging when controlled as a current source. To tackle this concern, this paper proposes a new compact multi-port dc/dc converter that integrates SC at the PV side by modifying the standard boost converter with three additional switches (two switches are soft switched and one is hard switched with low voltage) and three diodes. This topology allows SC operation at almost their entire voltage range, while a decoupling control method ensures separate regulation of the PV array and SC. The complete control scheme leverages both the SC and PV array for frequency response and comprises voltage recovery and protection for the SC. The proposed system is supported by theoretical analysis and design recommendations, as well as experimental validation results on a 675 Watt lab prototype.**

***Keywords*—Frequency services, multi-port converter, photovoltaic systems, supercapacitors, synthetic inertia.**

NOMENCLATURE

SC	Supercapacitors
PV	Photovoltaic
FRS	Frequency Response Services
PFR	Primary Frequency Response
ES	Energy Storage
BES	Battery Energy Storage
SOC	State of Charge
MPC	Multi-Port Converter
ZVS	Zero Voltage Switching
CFF	Continuous Frequency Fluctuation
UFE	Under-frequency Event
OFE	Over-frequency Event
SSV	Steady-state Voltage
MPPT	Maximum Power Point Tracking
PU	Per Unit

I. INTRODUCTION

THE ongoing decarbonization of the power systems worldwide sees a rapid reduction of system inertia with the replacement of synchronous generation by inverter-based resources, such as PV systems, wind farms etc. [1]. Low-inertia systems are more susceptible to disturbances and stability issues [1], [2], which is why nowadays most grid guidelines mandate FRS from distributed generation (e.g. IEEE 1547 [3], NREL (USA) [4], CERC (India) [5], National Grid ESO (UK) [6]), including PV systems.

To enable a comprehensive range of FRS, e.g. PFR, synthetic inertia emulation, it is imperative for the PV system to have the capability to increase its output as needed. This necessitates the integration of some form of ES. *Virtual* ES approaches involve either DC link energy extraction [7], [8] or keeping power headroom in the PV generator [9], [10]. Although no additional capital investment is required, this approach suffers from limited DC link capacity in the former case and PV capacity under-utilization and weather dependency in the latter. Common *physical* ES solutions for PV and other grid applications are based on BES, compressed air storage, pumped storage, superconducting magnetic ES, or hydrogen and fuel cells [11]. However, such ES technologies feature high energy density and are more suited for energy-intensive services, such as peak-shaving and load-shifting, rather than power-intensive FRS. SC are a more compact and well-suited ES solution for FRS, owing to their high power density and burst power handling capability, extensive charging/discharging cycle capacity, very fast dynamic response, and minimal maintenance requirements [11], [12]. This paper delves into the optimal integration of SC into a PV system for FRS, aiming at a compact and cost-effective solution.

Many studies explore SC hybridization for dynamic performance improvement in micro-grids with PV, battery, diesel, and/or wind power generation [12]–[19]. A study on optimal BES/SC hybridization is performed in [17]–[19] either for generation smoothing, FRS, voltage or frequency stability improvement. However, these investigations often overlook a key challenge in SC integration—their varying operating voltage based on the SOC [11], [12]. The conventional parallel connection to the DC link via a low gain DC-DC converter [17], [18] results in an oversized SC unit that operates in a limited voltage range and thus poor utilization factor. Alternatively, direct connection of the SC to the DC link of the inverter [20], [21] or across the PV array [22], [23] are also sub-optimal, given the limited allowable voltage range and the high parasitic resistance of the SC causing excessive losses due to continuous power exchange [11], [12]. An AC-coupled SC inverter is proposed in [24] to convert any grid-following system to grid-forming, which still requires an unnecessarily

large SC bank due to the low gain DC-DC stage. None of the above approaches satisfy the compactness requirement of the PV/SC hybridization.

Addressing the voltage variability challenge, a cascaded PV/SC topology in [25] sets the SC effectively in series with the PV array through a DC-DC and DC-AC configuration. Although this approach leverages up to 80% of SC capacity, it involves two additional power converters for the SC, one of which is part of the main conduction path even when the SC stays idle, which entails high complexity/cost and reduced system efficiency. Alternative high-gain architectures that employ voltage multiplier cells with either coupled- or switched-inductors [26]–[29], switched capacitors [30] or such hybrids [31] may help in efficient SC utilization. However, these approaches come with high additional costs, reduced reliability, efficiency, and low power density [32]. Consequently, these drawbacks make them less justified for PV/SC hybridization, especially when primarily targeting FRS.

A promising alternative towards both compact and cost-effective PV/SC hybridization is the multi-port power converter. Fully or partially *isolated multi-port topologies*, as proposed in [33], [34], aiming for SC/BES integration in renewable energy applications, could theoretically be utilized for this purpose. It is indeed true that the use of an isolation transformer provides more protection from fault point of view, however, the substantial increase in switching components may diminish the system reliability. In addition, the associated complexity, particularly in achieving a wide operational voltage range, undermines the primary objective. *Non-isolated Multi-port topologies* are more suited to this application instead. Nevertheless, the main challenge with such multi-port converters is the voltage range in their ports, usually being either all high [34]–[41] or all low [42]–[45] voltage ports with respect to the DC link. That poses a real challenge in this application, in which the SC voltage is not only much lower than the PV array voltage, but it is also variable with the SOC.

Energy stored Quasi-Z source inverter in [46] can be a potential candidate that can support ES operating voltage variability by modulating the shoot-through duration. However, its drawback lies in interfering with the inverter operation due to lack of intermediate DC-DC stage. In contrast to traditional voltage source inverters, the associated pulse-width modulation techniques in the prior case lead to either substantial common mode leakage current at PV stray capacitance or suffers from higher order harmonics at the inverter end, presenting a trade-off [47]. Due to these limitations, this topology is not considered here. In [48], a boost-multi-port topology has been presented which deals with different voltage levels in the ES port. However, the major drawbacks were, 1) low efficiency due to more switches in the current flow path at any instant (all are hard switched), 2) Pulsating common-mode voltage at PV terminal. Consequently, this topology may not be the right choice for the study-case application.

Keeping in view all the spotlighted issues, including compactness, cost, and SC capacity utilization etc, the authors in [49], proposed a single inductor based compact boost derived topology for PV/SC hybridization, which connects a small SC unit in series fashion with PV as shown in Fig. 1. This was the

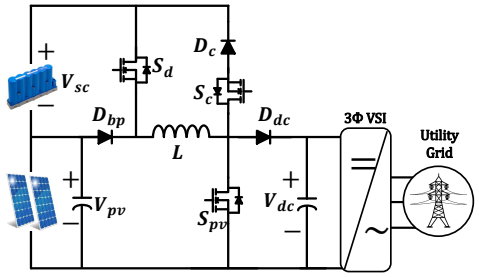

Fig. 1. Basic PV/SC tri-port topology proposed in [49]

first of its kind simple multi-port approach to provide FRS to PV system leveraging the wide voltage variability of the SC port. However, it comes with certain limitations, outlined as follows:

1) Limited current discharging capability of the ES port: A PFR with stiffer droop would rather demand large voltage SC than needed during low PV operation.
2) Effective control decoupling between PV and SC is not addressed: It is required to ensure independent and interference-free operation.
3) The operation, capability and control of the converter during an over frequency event is not discussed.
4) The requisite SC protection control to avoid surpassing extreme voltage limits is not addressed.
5) last but not the least, the much needed voltage recovery control of the SC, post-frequency event is not covered.

This research article is the extension of the concept presented in [49], which attempted to address all those limitations and proposed solutions to meet the gap. A mature *PV/SC MPC* is introduced here that exhibits the following novel features:

1) Compact single-inductor design by adding just three switches and three diodes to the PV-side boost converter
2) The two primary switches for the SC operation are soft switched (ZVS ON), hence improved efficiency.
3) Improved discharging capability ensures optimum SC capacity utilization by allowing operation at almost the entire SC voltage range.
4) Virtually no impact on the PV conversion efficiency, as just one diode is added on the PV current path.
5) Decoupled and independent operation of the PV and SC components via a novel feed-forward control loop.
6) Complete FRS control scheme that leverages both the SC and PV capacity and accounts for the SC protection and voltage recovery.

The flow of the paper is as follows. Section II talks about the system under consideration and the proposed PV/SC MPC and its working principle, followed by sizing and design considerations in Section III. The proposed control scheme is elaborated in Section IV, followed by experimental results on a 675 W lab prototype in Section V. Section VI performs the loss analysis, efficiency calculation and a qualitative comparison to other topologies and Section VII concludes the paper.

TABLE I. PARAMETERS OF THE PV SYSTEM AND THE BENCHMARK FREQUENCY EVENTS UNDER CONSIDERATION

Targeted PV system and frequency events	Ratings and Parameters
PV System	PV Side: 10 kWp, 510 V, 19.6 A DC Link: 700 V AC side: 3 Phase VSI, 10 kVA 400 V(L-L rms), 50 Hz
Worst case CFF across nominal frequency	Δf_{max}: $\pm$ 0.003 PU ($\pm$ 150 mHz) $RoCoF_{max}$: $\pm$ 0.8 Hz/s
Benchmark PFR profiles	Duration (T_f) : 16.1 s Frequency nadir (f_{nadir}) : 50 $\pm$ 0.55 Hz Frequency settling value (f_{off}): 50 $\pm$ 0.2 Hz Instance of f_{nadir} (t_{nadir}) : $0.214T_f$

II. PROPOSED PV/SC MPC

This section sets out the PV system under consideration and targeted FRS, followed by the details of the proposed PV/SC MPC and its working principle.

A. PV System Under Consideration

This study focuses on the application of small-scale rooftop PV systems with capacities typically in the range of a few kilowatts peak, which usually operate in grid-following mode and are not typically equipped with ES. The objective is to upgrade such systems with FRS capability by integrating SC directly into the PV inverter in a single-package and cost-effective manner. Such FRS capability is required by grid codes and system operators at increasingly lower voltage levels and generation capacities [3]–[6], and are seen today as a requirement for the low-inertia decarbonised power system of the future. Table I provides the PV system under consideration and benchmark frequency events, namely inertia emulation for CFF and PFR for an UFE and an OFE. Additional information on FRS services are available in [3], [18], [19].

B. Proposed PV/SC MPC Topology

Although, the series connection of the SC with PV in case of basic PV/SC tri-port topology introduced in [49] helped utilizing the full SOC of the SC, the discharging current capacity of the SC port was limited to the maximum available PV current (when the duty of S_d (d_d) equals to 1 in Fig. 1). This under-utilises the power handling capability of the SC during discharging and would demand large SC unit to address FRS at low PV output. In order to meet this issue and to make the SC discharging independent of the PV current, a modified topology is proposed here by adding a switch-diode pair (S_{d2}-D_{d2}) to the basic version as shown in Fig. 2. Conduction of this additional leg can help stepping up the SC current beyond the PV current by increasing the inductor current with momentary decoupling of SC from PV. The detailed operation of the proposed PV/SC MPC is illustrated in the next subsection.

C. Operating Principle of PV/SC MPC

The PV/SC MPC can operate by bringing the SC either in series to the PV array or in parallel to the inductor through six different modes in which the SC are either idle, discharging or charging as summarized in Table II and illustrated in Fig. 3. These modes are described in detail in the following paragraphs.

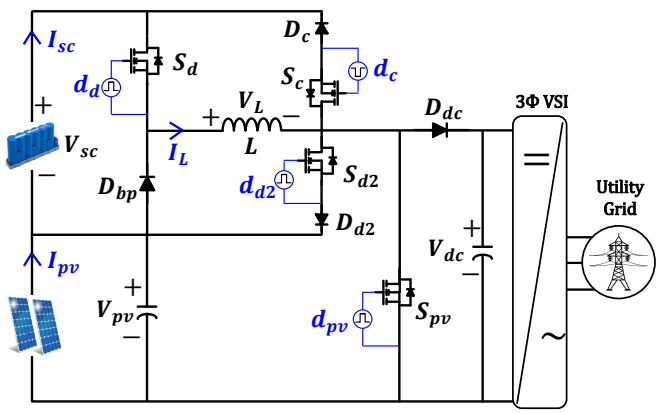

Fig. 2. Proposed PV/SC MPC topology.

1) SC is idle (only PV is active): During normal undistorted conditions, the SC should remain idle and only the PV array should deliver power to the grid. This is effectively managed by means of the diode D_{bp}, which bypasses the SC module when the switches S_c, S_d and S_{d2} are OFF. The corresponding operating modes SC-I-ON and SC-I-OFF, shown in Fig. 3(a)-(b) align with the standard boost converter modes based on the ON/OFF status of S_{pv}. This is an effective bypass mechanism that introduces only one diode (D_{bp}) in the conduction path when the SC stays idle, in contrast to cascaded alternatives such as in [25]. Clearly, in these modes the inductor current (I_L) equals the PV current (I_{pv}).

2) SC is discharging: During UFE or CFF frequency distortions, the PV system should be delivering additional power to the grid by discharging the SC. There are three possible SC discharging modes denoted SC-D-ON, SC-D-OFF and SC-TD, as illustrated in Fig. 3(c)-(e) respectively. However, with the first two modes the SC discharging current $\left(I_{sc}^{dis}\right)$ is capped by I_{pv}, as the case in [49], given by

$$I_{sc}^{dis} = d_d I_L = d_d I_{pv} \tag{1}$$

where d_d is the duty ratio of switch S_d. To achieve higher discharging rates, the turbo-discharge (SC-TD) mode is introduced, as shown in Fig. 3(e). In this mode, S_d and S_{d2} are turned ON simultaneously, discharging the SC directly onto the inductor by momentarily disconnecting the PV array from the inductor, thus boosting I_L beyond I_{pv}. The SC current expression with this mode is given by

$$I_{sc}^{dis} = I_L = \frac{I_{pv}}{1 - d_{d2}^*} \tag{2}$$

Here, d_{d2}^* denotes the effective conduction duration of S_{d2} as shown in Fig. 4(b). To clarify, d_{d2}^* is the duration of the system-generated gate pulse (d_{d2}), except when S_{pv} is ON i.e.

TABLE II. OPERATING MODES OF PV/SC MPC

Mode	Involvement of PV array	SC state
SC-I-ON	✓	idle
SC-I-OFF	✓	idle
SC-D-ON	✓	discharging
SC-D-OFF	✓	discharging
SC-TD		turbo-discharging
SC-C		charging

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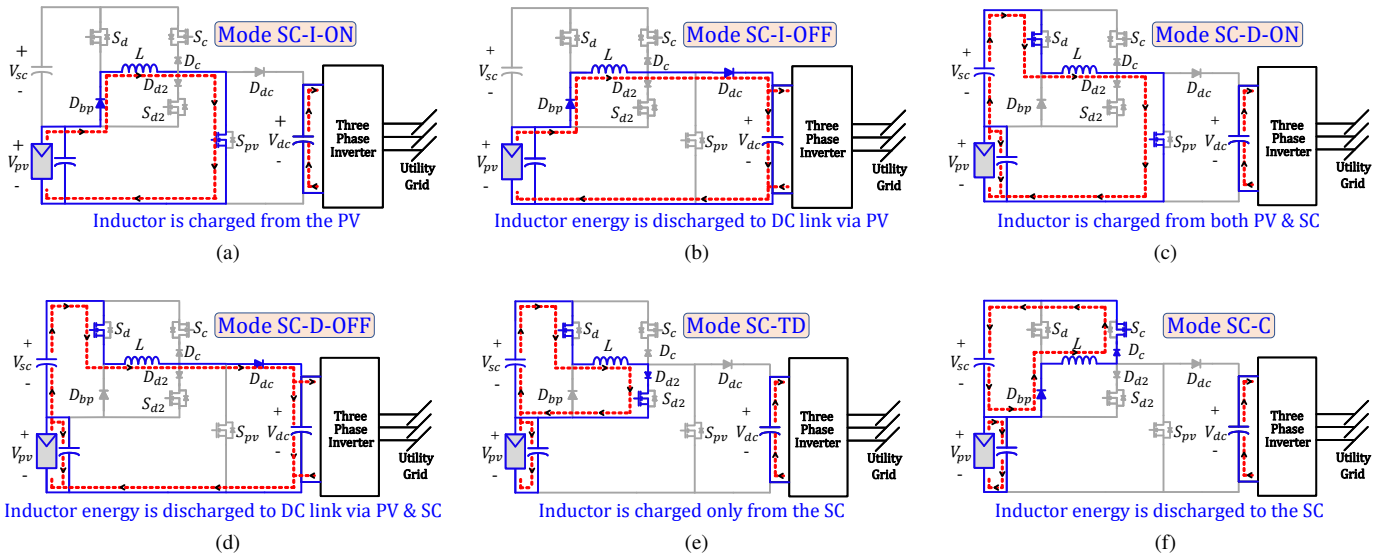


Fig. 3. The six operating modes of the proposed PV/SC MPC when the SC is (a)-(b) idle, (c)-(e) discharging, or (f) charging.

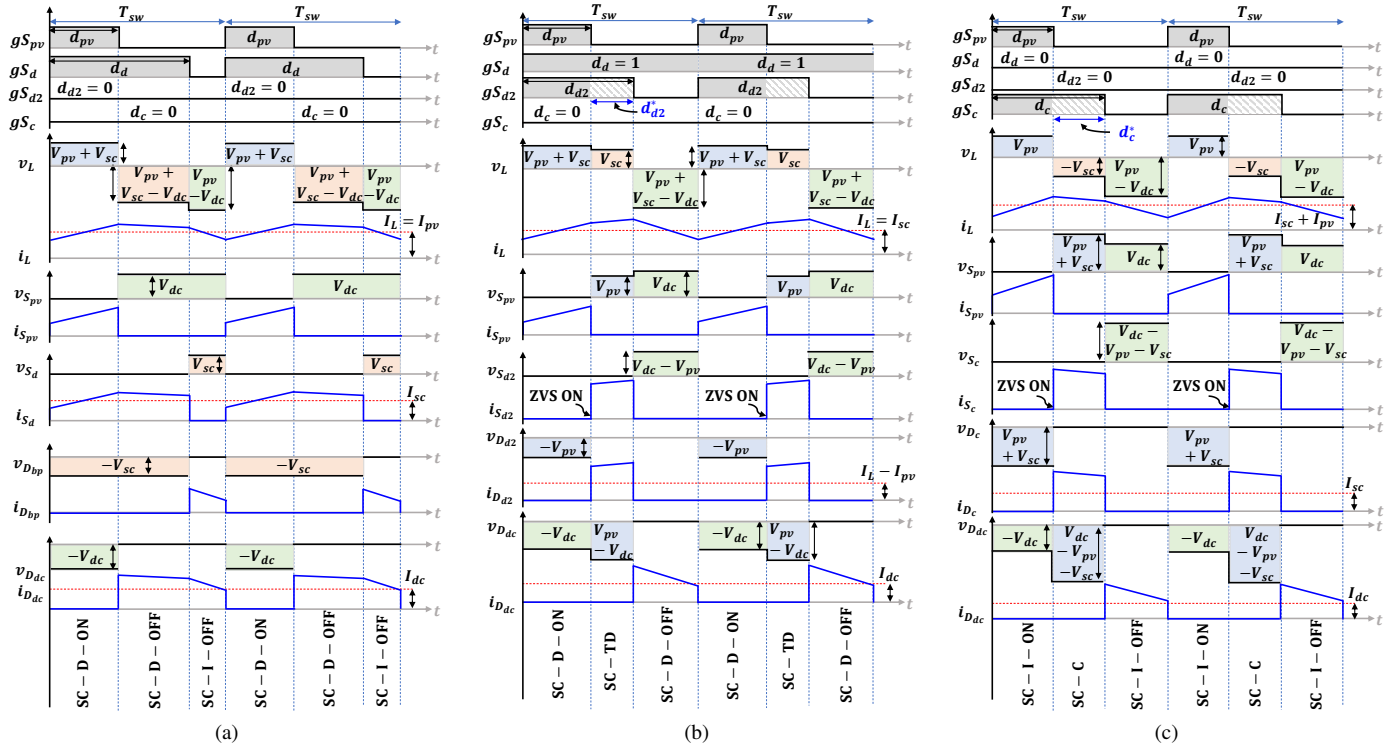


Fig. 4. The mode sequences when the SC is (a) discharging, (b) turbo discharging or (c) charging.

$d^*_{d2} = min(d_{d2} - d_{pv}, 0)$. Fig. 4(a)-(b) depict waveform examples of normal and turbo discharging operations, providing a visual representation of the effective conduction duration of each switch along with their voltage and current profiles in a switching cycle. Note in Fig. 4(a) the mode sequence {SC-D-ON, SC-D-OFF, SC-I-OFF} when $d_d > d_{pv}$, and how this changes to {SC-D-ON, **SC-TD**, SC-D-OFF} in Fig. 4(b) when $d_{d2} > d_{pv}$ and $d_d = 1$. The SC-TD mode is invoked when d_d has reached to its maximum value (i.e. d_d = 1) and d_{d2} comes into the picture.

3) SC is charging: This scenario occurs during an OFE or during CFF frequency distortions, when the grid frequency

goes beyond the nominal frequency momentarily. That means the PV system needs to decrease its power output by charging the SC with the desired power command. This can be achieved by modulating the duty cycle of the switch S_c (d_c), once S_{pv} is OFF, which leads to buck-boost operation for both the PV array and SC as shown in Fig. 3(f). The mode sequence becomes {SC-I-ON, SC-C, SC-I-OFF} as in Fig. 4(c), while the current expressions are given by

$$I_{sc}^{ch} = d_c^* I_L = \frac{d_c^*}{1 - d_c^*} I_{pv} \tag{3}$$

Here, d_c^* denotes the effective conduction duration of S_c. To clarify, d_c^* is the duration of the system-generated gate pulse (d_c), except when S_{pv} is ON i.e. $d_c^* = min(d_c - d_{pv}, 0)$.

Utilizing this PWM method for both switches, S_{d2} and S_c along with S_{pv} as in Fig. 4(b)-(c) facilitates achieving Zero Voltage Switching (ZVS-ON) for both. This is attributed to the fact that the reverse voltage, when S_{pv} is ON appears across the diodes connected in series (i.e. D_{d2} and D_c respectively), causing the body-diodes of the switches to become forward-biased. Consequently, the forward voltage drop of the body-diodes eventually manifests as the off-state voltage stress for the respective switches before they starts conducting, once S_{pv} turns-off.

A generalised expression for the voltage gain of the DC link port with respect to both PV port and SC port, irrespective of SC operating modes can be given by

$$\frac{V_{dc}}{V_{pv}} = \frac{1}{1 - d_{pv} - d_{d2}^* - d_c^*} \left(1 - d_{d2}^* - d_c^* + \frac{V_{sc}}{V_{pv}}(d_d - d_c^*)\right) \tag{4}$$

$$\frac{V_{dc}}{V_{sc}} = \frac{1}{1 - d_{pv} - d_{d2}^* - d_c^*} \left(d_d - d_c^* + \frac{V_{pv}}{V_{sc}}(1 - d_{d2}^* - d_c^*)\right) \tag{5}$$

When SC is idle $(d_c^* = d_d = d_{d2}^* = 0)$, Eq. (4) reduces to the regular boost converter voltage gain expression, while Eq. (5) is valid only if PV is connected (i.e. the day-time operation). Detailed derivation of Eqs. (4) and (5) are carried out in Eqs. (A1) to (A4) of the Appendix section.

It is important to note that the system is not configured for night-time operation, considering its intended application. The SC enhancement serves as a supplement to the PV system rather than functioning as a standalone energy storage system capable of independent operation. From a technical standpoint, the SC could potentially discharge even without PV contribution, but its ability to provide substantial UFE support is limited due to the converter's extreme duty operation, leading to higher losses. Moreover, addressing OFE and CFF is not feasible, as both scenarios necessitate SC charging, which is impossible without the PV as the primary source and no provision for grid-based charging due to the limitation in switch configuration, as it falls outside the scope of intended application.

This paper also sheds light on another crucial aspect of this converter–its capability in the absence of one of the sources. Undoubtedly, the converter will continue to operate even if the SC is disconnected, seamlessly maintaining PV side generation. This flawless operation is facilitated by the bypass diode D_{bp}, ensuring a continuous path for PV current in the event of an open circuit in either the SC or the associated switches or diodes following a fault. In this scenario, the proposed converter will function exclusively in SC-I-ON and SC-I-OFF modes, depicted in Fig. 3(a) and (b) of the manuscript, resembling a conventional boost converter. Under these conditions, the circuit retains the ability to address an OFE by curtailing some power from the PV. However, it forfeits its capability to handle a UFE, which demands surplus power beyond the PV MPPT power to be dumped into the grid. In the absence/fault in PV, the system behaves similarly to the night-time operation explained in the preceding paragraph.

TABLE III. FRS REQUIREMENTS

FRS variables	Values
Dynamic Inertia constant (H)	2 s to 9 s
Droop coefficient (k_{PFR})	5 %
FRS power and energy requirements	**Values**
Max power demand at CFF (P_{sc}^{CFF})	$\pm$1.05 kW
Max power demand at PFR (P_{sc}^{PFR})	$\pm$1.6 kW
Max energy demand at CFF (E_{sc}^{CFF})	$\pm$540 Jules
Max energy demand at PFR (E_{sc}^{PFR})	$\pm$15.1 kJules
SC Module EATON (XTM-18R0626-R)	**Values**
Nominal voltage (V_{sc}^{nom})	18 V
Nominal capacitance (C_{sc}^{nom})	61.7 F
Nominal stored energy (E_{sc}^{nom})	10.08 kJ
Peak current capacity (I_{sc}^{pk})	235 A

III. SIZING AND DESIGN OF THE PV/SC MPC

This section outlines a design methodology for the PV/SC MPC to meet the FRS requirements considering a 10 kW PV system with a $\pm$1.6 kW SC port (see Table I). In addition, this section includes the SC characteristics and current rating of the inductor and switches. The first step is to derive the power and energy requirements for the prescribed FRS of Table I, for which the straightforward methodology of [25], [50] can be applied. Table III gives these values for different inertia constants and droop setting.

A. SC Bank Sizing

The size of the SC bank is determined by the energy requirements. While the proposed topology theoretically allows complete discharge of the SC (i.e. to zero voltage), in practice a lower voltage bound (V_{sc}^{min}) is introduced to account for parasitic voltage drops across the switches and inductor in the path. A value of 5 V is considered in this case, which corresponds to about 98% capacity utilization for the selected SC bank, as detailed below. The SC voltage rating V_{sc}^{req} needs to cover the total peak energy demand $E_{sc}^{tot} = E_{sc}^{PFR} + E_{sc}^{CFF}$, i.e. the combined demand during UFE and CFF, after accounting for V_{sc}^{min} as in (6). More information on the selected SC module (XTM-18R0626-R) is at [51] (see Table III).

$$\begin{aligned} E_{sc}^{tot} &= \left[0.5\left(\frac{C_{sc}^{nom}}{N_{sc}}\right)\left(V_{sc}^{req2} - V_{sc}^{min2}\right)\right] \\ &\leq \left[0.5\left(\frac{C_{sc}^{nom}}{N_{sc}}\right)\left(V_{sc}^{nom2} N_{sc}\right)\right] \Longleftrightarrow \\ V_{sc}^{req} &= \sqrt{V_{sc}^{min2} + \frac{2\, N_{sc}\, E_{sc}^{tot}}{C_{sc}^{nom}}} \leq V_{sc}^{nom}\, N_{sc} \end{aligned} \tag{6}$$

Rearranging (6) yields the quadratic inequality (7), which can then be solved for the No.of SC modules (N_{sc}) in series to form the required SC bank as in (8). Please note the positive root in (8), as the negative one does not have a physical meaning, and the ceiling operator that rounds up N_{sc} to the closest integer. This leads to selection of two no.s of such SC modules, which can now together provide almost 20 kJ of energy, enough to meet the objective of 15.1 kJ.

$$V_{sc}^{nom2}\, C_{sc}^{nom} N_{sc}^2 - 2\, E_{sc}^{tot}\, N_{sc} - V_{sc}^{min^2}\, C_{sc}^{nom} \geq 0 \quad (7)$$

$$N_{sc} = \left\lceil \frac{E_{sc}^{tot} + \sqrt{E_{sc}^{tot^2} + (V_{sc}^{nom}\, V_{sc}^{min}\, C_{sc}^{nom})^2}}{V_{sc}^{nom^2}\, C_{sc}^{nom}} \right\rceil \quad (8)$$

Detailed explanation on Eqs. (6) to (8) is in the sub-section B of the appendix section of the manuscript.

B. SC Voltage Set-point

Now that the SC bank has been sized, the next step is to determine the SSV of the SC (V_{sc}^{SS}) at normal conditions. This voltage set-point should provide the appropriate footroom and headroom for the prescribed FRS, i.e. being within the following bounds:

$$V_{sc}^{req} \leq V_{sc}^{SS} \leq V_{sc}^{ul} \quad (9)$$

The lower bound is obviously V_{sc}^{req}, which can be evaluated via (6) for the selected N_{sc} modules. For the headroom, the charging strategy during CFF and OFE needs to be determined first. CFF involves minimal net energy requirements and can be solely supported by the SC; conversely, an OFE entails significant energy surplus in the system that would lead to unnecessarily high SC headroom and oversizing if it was to be delivered by the SC alone. Instead, a hybrid PV/SC approach is followed here at OFE that leverages the PV array down-regulation capacity (power curtailment) when the SC get full (more details in Section IV). Therefore, the upper voltage limit V_{sc}^{ul} is designed according only to the CFF energy requirements E_{sc}^{CFF} and is given by [50]:

$$V_{sc}^{ul} = \sqrt{(N_{sc}\, V_{sc}^{nom})^2 - \frac{2\, N_{sc}\, E_{sc}^{CFF}}{C_{sc}^{nom}}} \quad (10)$$

For the study-case system and FRS, (6) and (10) bound V_{sc}^{SS} within 32.2 V and 35.5 V. Despite the chosen operational constraints on SC voltage for control ease, a substantial portion of the total energy, ranging from 78-95%, can still be harnessed from the SC bank. Here, a mid-range value of 34 V is selected, representing 88% of the energy-extraction capability, but any value within that range would be suitable as well.

C. Current Ratings

Once the SC bank size has been selected based on the FRS *energy* requirements, the next step is to consider the *power* requirements. The burst power capability of SC is very high by nature and normally exceeds these requirements (e.g. 7.4 kW capacity vs 1.6 kW maximum demand here - see Table III); therefore, the following calculations refer essentially to the current rating of the involved inductor and switches.

Starting with inductor, the peak current rating $I_{L,pk}^{req}$ should be such as to meet the worst-case power demand. An UFE is such a worst case, in which the maximum power demand P_{sc}^{PFR} is required around the frequency nadir, at a time that the SC voltage has already dropped from the SSV value due to the energy discharged up to that point. That discharged energy depends on the frequency profile. Regardless of the timing of the frequency nadir, the energy spent was consistently in the range of 30% to 40% of the entire UFE energy requirement $\left(E_{sc}^{PFR}\right)$ for common cases [25]. Therefore, in this paper, 40% is approximated as a worst-case scenario to determine the maximum possible current rating for the inductor (L) that should be designed. Based on this, the inductor current rating can be found by

$$I_{L,pk}^{req} = \frac{P_{sc}^{PFR}}{\sqrt{V_{sc}^{SS^2} - 40\% \frac{2\, N_{sc} E_{sc}^{PFR}}{C_{sc}^{nom}}}} \quad (11)$$

For the study-case system $I_{L,pk}^{req}$ is 57.9 A. Additionally, a 5% margin is considered to accommodate any further fluctuations, which gives $I_{L,pk}^{req}$ as 60 A. Thereafter, the worst case current and voltage stress of the associated switches and diodes can be estimated as in Table IV. It is recommended that an 150% safety factor is considered in the final selection.

D. Charging Limitations

The PV/SC MPC topology does not impose any limit on the discharging current, and it can easily reach $I_{L,pk}^{req}$ regardless the PV current by regulating S_{d2} (see (2)). However, this is not the case with the charging current. The highest charging rate is achieved when only modes SC-I-ON and SC-C appear, without being followed by any SC-I-OFF mode (refer to Fig. 4(c) for better clarity); i.e. the entire PV power is directed to the SC via the inductor; which is similar to a buck-boost converter with two ports, where PV acts as the input port and SC as the single output port. In this case, $d_{pv} = V_{sc}/(V_{pv} + V_{sc})$ and $d_c^* = 1 - d_{pv}$, which if substituted into (3) yields (12) below once the inductor current rating is applied:

$$\begin{aligned} I_{sc,pk}^{ch} =& I_{L,pk}^{ch} - I_{pv}, where \\ I_{L,pk}^{ch} =& \begin{cases} I_{L,pk}^{req} & , \text{ if } d_c^* < 1 - d_{pv} \\ \frac{I_{pv}\,(V_{pv}+V_{sc})}{V_{sc}} & , \text{ if } d_c^* = 1 - d_{pv} \end{cases} \end{aligned} \quad (12)$$

TABLE IV. RATING OF THE DIODES AND SWITCHES

Switch/ Diode	Current Rating		Voltage rating	
	Theoretical	Value	Theoretical	Value
S_{pv}	$I_{pv}^{max}\sqrt{\frac{V_{dc}-V_{pv}}{V_{dc}}}$	10.2 A	V_{dc}	700 V
S_c	$\sqrt{I_{L,pk}^{ch}\left(I_{L,pk}^{ch} - I_{pv}^{min}\right)}$	60 A	$V_{dc}-(V_{pv}+V_{sc}^{min})$	190 V
S_d	$I_{L,pk}^{dis}$	60 A	V_{sc}^{max}	36 V
S_{d2}	$\sqrt{I_{L,pk}^{dis}\left(I_{L,pk}^{dis} - I_{pv}^{min}\right)}$	60 A	$V_{dc} - V_{pv}$	200 V
D_{bp}	$I_{L,pk}^{ch} - I_{pv}^{min}$	60 A	V_{sc}^{max}	36 V
D_{dc}	$I_{pv}^{max}\sqrt{\frac{V_{pv}}{V_{dc}}}$	15 A	V_{dc}	700 V
D_c	$I_{L,pk}^{ch} - I_{pv}^{min}$	60 A	$V_{pv} + V_{sc}^{max}$	546 V
D_{d2}	$I_{L,pk}^{ch} - I_{pv}^{min}$	60 A	V_{pv}	510 V

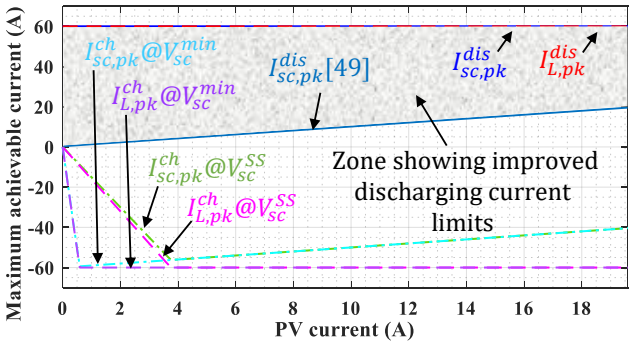


Fig. 5. Charging and discharging current limits of the modified PV/SC MPC with respect to [49].

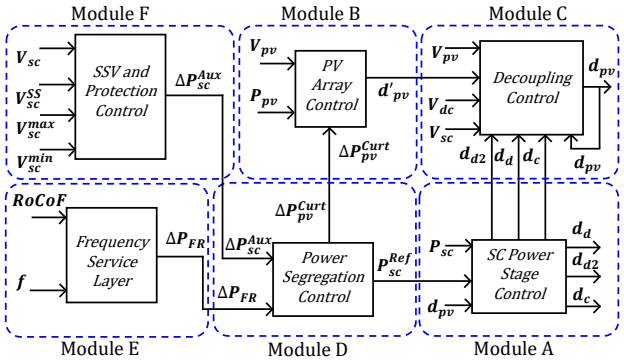


Fig. 6. Concise picture of the control scheme.

Fig. 5 illustrates the impact of I_{pv} and SC voltage on these current limits. During discharging, there is no such dependence on I_{pv} unlike in [49], with the peak current values of SC $(I^{dis}_{sc,pk})$ and inductor $(I^{dis}_{L,pk})$ are constrained only by the hardware current rating set to 60 A. During charging, however, the peak current of the inductor $(I^{ch}_{L,pk})$ is restricted by I_{pv} when the latter is low (i.e. less than 4 A at V^{SS}_{sc} and less than 1 A at V^{min}_{sc}) according to (12). This indicates an enhancement in the charging capability with a lower SC voltage. Moreover, the peak current of the SC $(I^{ch}_{sc,pk})$ is further constrained by the difference between $I^{ch}_{L,pk}$ and I_{pv} as in (12). It shows no modification in charging capability compared to [49]. It is worth noting though that these charging limits do not tamper with the FRS requirements, as the SC charging power can be easily complemented by PV power curtailment for down-regulation of the entire system's output power (detailed explanation is in section IV).

IV. Proposed Control Schemes

This section outlines of the proposed control scheme that meets the frequency response objectives in a grid following PV system via the proposed PV/SC MPC. The entire control scheme is divided into six modules as listed below:

1) Module A: SC power stage control
2) Module B: PV array control
3) Module C: Decoupling control
4) Module D: Power segregation control
5) Module E: Frequency Service layer
6) Module F: SSV and protection control

A concise overview of that scheme is given in Fig. 6. Modules E and F ascertain the adjustment of the output power based on the FRS and SC voltage protection, which is then split in module D into the SC contribution and PV array curtailment (if any). Module A implements the SC power flow by modulating the switches S_d, S_{d2} and S_c, while module B regulates the PV operating point by driving S_{pv}. Module C removes the interaction between SC and PV array, effectively decoupling their operation for improved dynamic performance. The detailed control scheme is shown in Fig. 7 and explained in the following paragraphs.

A. SC power stage control

This module generates the duty cycle of all corresponding switches of the SC power processing stage, as detailed in Fig. 7. A unified PI controller approach is employed here, which regulates the SC power P_{sc} to the reference P^{Ref}_{sc} by outputting a sole signal D that is subsequently demultiplexed into the individual duties d_d, d_{d2} and d_c as follows. A positive D indicates discharging the SC, primarily via S_d (modes SC-D-ON and SC-D-OFF) during regular discharge operation, and via both S_d and S_{d2} during turbo-discharge SC-TD. Therefore, d_d equals D up to the upper bound of 1 (see (1)), with the surplus (D−1) directed to d_{d2} after being interposed to d_{pv} (see (2)). Contrary, a negative D signifies charging the SC managed by S_c, with d_c determined by adding the absolute value of D to d_{pv} (see (3)). The hysteresis blocks prevent unwanted switching between charging and discharging modes when the SC power command is close to zero.

B. PV array control

As discussed in the preceding section, the SC is expected to remain almost fully charged during normal conditions in anticipation of any UFE. This entails little headroom to support solely OFE as well, a gap easily filled by momentary PV curtailment. This strategy optimally utilizes the SC's constrained capacity in a cost-effective manner [50].

Module B implements this logic by regulating the PV operating point in either MPPT or curtail mode. For a smooth transition between the two, the conventional MPPT structure, followed by a voltage PI controller is modified by adjusting the MPP voltage V_{mpp} by ΔV^{Curt}_{pv} to derive the PV voltage reference V^{Ref}_{pv}. This adjustment ΔV^{Curt}_{pv} is a negative value and comes from a separate PI controller, which follows the power command P^{Curt}_{Ref} coming from the MPP power P_{mpp} once reduced by the necessary curtailment ΔP^{Curt}_{pv}. To differentiate between the two modes, the power curtailment ΔP^{Curt}_{pv} is used: when it is zero, MPPT operated normally and the curtailment PI controller is reset; when it is positive, MPPT is frozen, locking P_{mpp} and V_{mpp}, while the PV operation is directed by the activated curtailment controller.

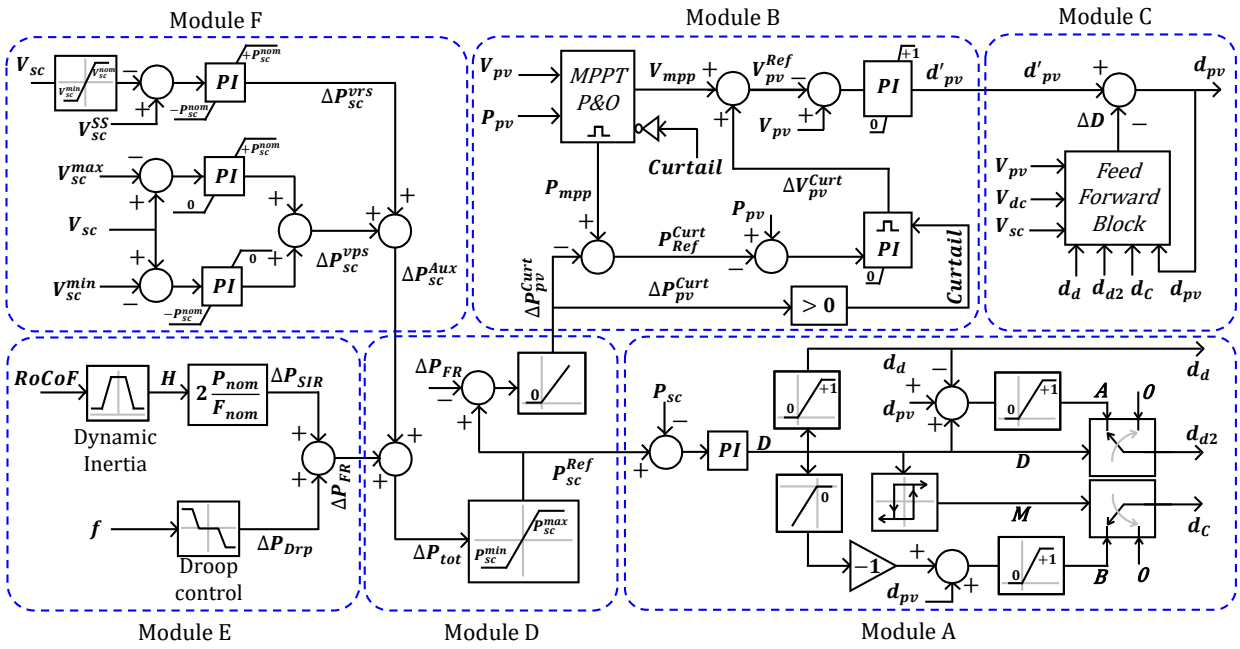


Fig. 7. Proposed control scheme in detail.

C. Decoupling control

The sole inductor in the proposed topology entails coupling of the SC and PV array operation, i.e. when trying to control one of the two, the other is inevitably affected. By utilizing d_{pv} in the calculation of d_{d2} and d_c in Module A, the PV array effect to SC is effectively eliminated, i.e. changes in d_{pv} simply pass through the SC processing stage. However, if it weren't for the decoupling control implemented by Module C, the influence of the SC on the PV stage would have persisted. Such coupling would impede independent control of the two components and compromise the dynamic performance of the PV/SC MPC.

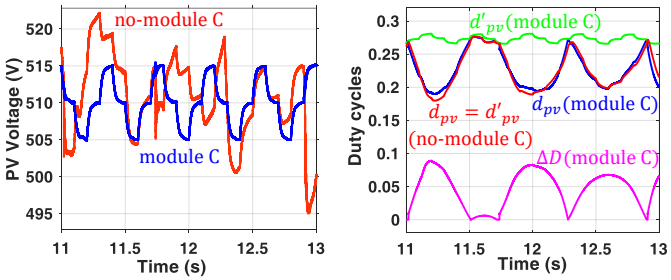
This module breaks this coupling link via a feed-forward stage at the PV control output, introducing a compensation term ΔD to the S_{pv} duty cycle. ΔD is determined by applying the volt-second balance to the inductor at steady state conditions (zero average inductor voltage across a switching cycle):

$$\begin{aligned} V_L =& V_{pv}\left(1-d_{d2}^*-d_c^*\right)+V_{sc}\left(d_d-d_c^*\right) \\ &-V_{dc}\left(1-d_{pv}-d_{d2}^*-d_c^*\right)=0 \Longleftrightarrow \\ V_L =& \left[V_{pv}-V_{dc}\left(1-d_{pv}\right)\right] \\ &-\left[\left(V_{pv}-V_{dc}\right)\left(d_{d2}^*+d_c^*\right)-V_{sc}\left(d_d-d_c^*\right)\right]=0 \end{aligned} \quad (13)$$

Note that in (13) the first term refers to the standard boost converter operation and the second term to the SC-stage effect. Dividing by V_{dc} and rearranging yields:

$$\frac{V_{pv}}{V_{dc}}=\left(1-d_{pv}\right)-\Delta D=1-\left(d_{pv}+\Delta D\right) \quad (14)$$

where ΔD represents the SC-stage effect on the PV operation given by (15). To remove that perturbation, Module C calculates ΔD in real time via (15) using voltage measurements and the SC-stage duty cycles, and subtracts that amount from S_{pv} duty cycle to effectively nullify this coupling.



(a) (b)

Fig. 8. Decoupling SC and PV operation. (a) PV voltage, (b) Duty cycles.

$$\Delta D=\frac{V_{sc}}{V_{dc}}\left(d_d-d_c^*\right)+\left(1-\frac{V_{pv}}{V_{dc}}\right)\left(d_{d2}^*+d_c^*\right) \quad (15)$$

An instance of the coupling effect and the importance of Module C is illustrated in Fig. 8, derived by simulations on the study-case system during intense CFF (see Table I). Without Module C, the PV voltage drifts at times from the MPPT operation in Fig. 8(a) (red line) due to the SC power exchange, an effect completely mitigated with Module C (blue line). Fig. 8(b) shows how d_{pv} is driven away from the optimal value without Module C (red line); with Module C, d'_{pv} reflects the standard MPPT operation (green line), as the calculated ΔD (magenta line) counteracts this coupling in d_{pv} (blue line).

D. Power segregation control

This module processes the total system power adjustment ΔP_{tot} required for FRS and SC protection, and distributes that amount to SC P_{sc}^{Ref} and PV array ΔP_{pv}^{Curt}. First, ΔP_{tot} is bounded within the current limits of the PV/SC MPC, which can be expressed as dynamic power limits by:

$$P_{sc}^{max} = V_{sc} I_{L,pk}^{dis} \tag{16}$$

$$P_{sc}^{min} = -V_{sc} \left(I_{L,pk}^{ch} - I_{pv} \right) \tag{17}$$

It's important to highlight that the peak inductor current limit is the deciding variable, with V_{sc} utilised solely for the conversion to power bounds. The resulting signal P_{sc}^{Ref} after the saturation drives the SC operation. In cases requiring PV curtailment, ΔP_{pv}^{Curt} comes from the positive portion of the difference $\left(P_{sc}^{Ref} - \Delta P_{FR}\right)$ (e.g. $\Delta P_{FR} = -1600$ W but $P_{sc}^{Ref} = -1350$ W due to charging limitations, so $\Delta P_{pv}^{Curt} = +250$ W).

E. Frequency Service layer

This layer calculates the power adjustments for SIR ΔP_{SIR} and droop control ΔP_{Drp}, which, when combined, yields the total FRS power requirement ΔP_{FR}. The implementation is quite standard in the literature and aligns with the IEEE 1547 standard [3], except that the concept of *dynamic inertia constant* is adopted here from [25].

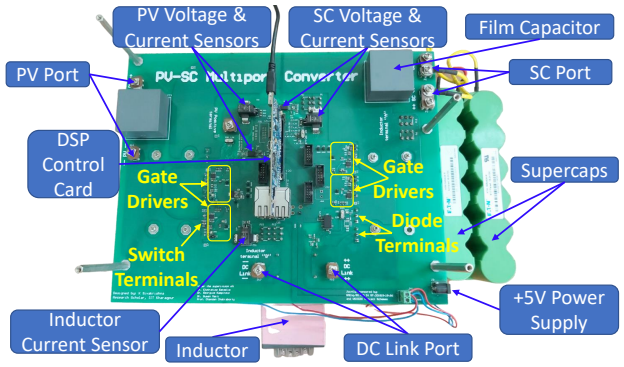
F. SSV and protection control

This is an auxiliary yet pivotal part of the control scheme, adopted from [50]. Its primary functions encompass (i) ensuring the SC voltage remains within the prescribed bounds $(V_{sc}^{min}, V_{sc}^{max})$ for protection, and (ii) gradually guiding the SC voltage back to the SSV target V_{sc}^{SS} following a disturbance. Both tasks are implemented by PI controllers that act upon the SC voltage and output power adjustments that eventually constitute ΔP_{sc}^{Aux} fed into Module D.

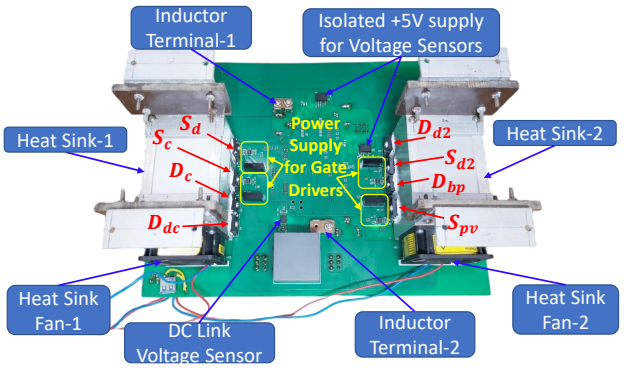
V. Experimental Validation

The proposed topology and control scheme underwent validation via experimental tests conducted on a 675 W lab prototype. The system details are given in Table V and a view of the prototype is depicted in Fig. 9. A solar simulator and a single SC module was used as inputs to PV/SC MPC, while its output was fed into a resistive load for simplicity. For one SC module, the SSV is selected as 15 V. For the selected PV and SC parameters, Eq. (11) sets $I_{L,pk}^{req}$ to 9 A (i.e. $2I_{pv}$). The converter performance is validated in terms of switching modes, followed by the evaluation of its FRS capabilities in three case-studies for CFF, UFE and OFE.

Four different possible sequence of modes are experimentally validated as shown in Fig. 10 to justify the claims in section II. The regular discharging of the SC is shown for $d_d < d_{pv}$ in Fig. 10(a) and for $d_d > d_{pv}$ in Fig. 10(b) respectively. Fig. 10(c) confirms the switching states during turbo-discharging, followed by the validation of modes during SC-charging in Fig. 10(d). As depicted from Fig. 10(c) and



(a)



(b)

Fig. 9. Lab developed experimental prototype for PV/SC MPC: (a) Top view, (b) Bottom view.

TABLE V. Hardware Prototype Characteristics

System	Ratings/Part Numbers
System Parameters	Solar Simulator: SL375-10.4/415+HS PV rating: 675 Wp, 150 V, 4.5 A DC Link rating: 200 ± 20 V, Load: 50 to 100 Ω One SC Module: XTM-18R0626-R, 18 V, 61.5 F Inductor: 320 μH, 15 A Capacitors: 2000 μF, 400 V, 9 A(rms) Switching Frequency F_{sw}: 100 kHz
Major Components	SiC MOSFETs: $C3M0032120K$ (CREE) SiC Schottky Diodes: $E3D30065D$ (CREE) Gate Driver: $UCC5350SBDR$ (TI) Voltage Sensors: $ACPL$-387A-000E (BROADCOM) Current Sensors: $HLSR$10-P/SP33 (LEM)

Fig. 10(d), both the switches S_{d2} and S_c undergoes ZVS ON, firing at the instant of S_{pv}, yet they don't conduct till S_{pv} is ON and the entire revers voltage appears across their respective anti-series diodes.

A. SIR under CFF

The experimental prototype is subjected to the benchmark CFF of Table. I (≈ 67 W @peak RoCoF = 0.4 Hz/s) and its response is captured in Fig. 11(a) and Fig. 11(b) for two distinct cases of the initial SC voltage (V_{sc0}): Case 1 with V_{sc0} = 15 V (normal level), and Case 2 with V_{sc0} = 9 V (reduced level due to a prior UFE). As depicted in Fig. 11(a), in Case 1 no voltage and current limits are breached and the

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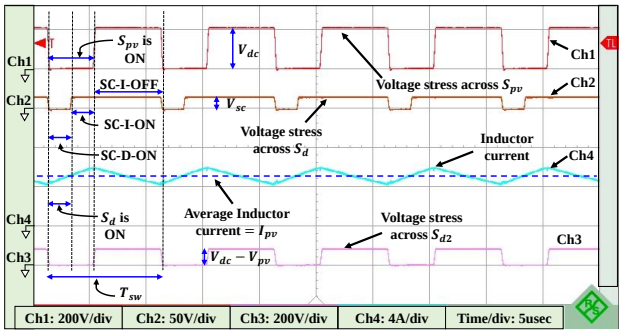
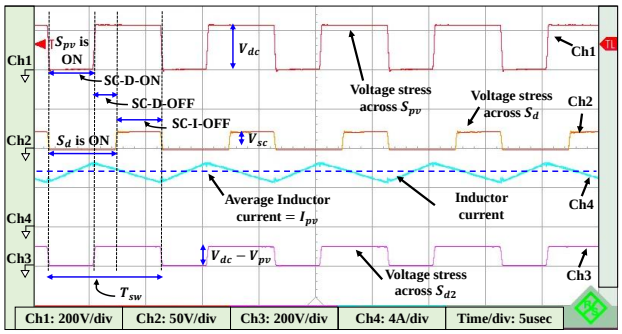


(a)



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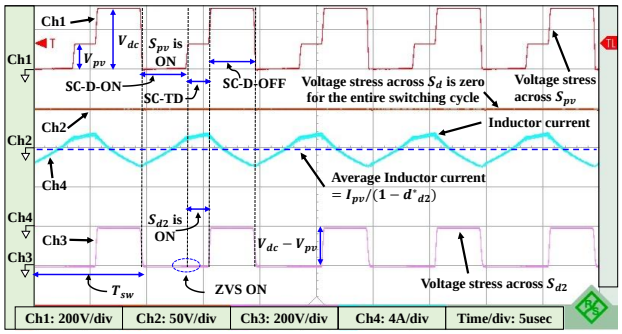
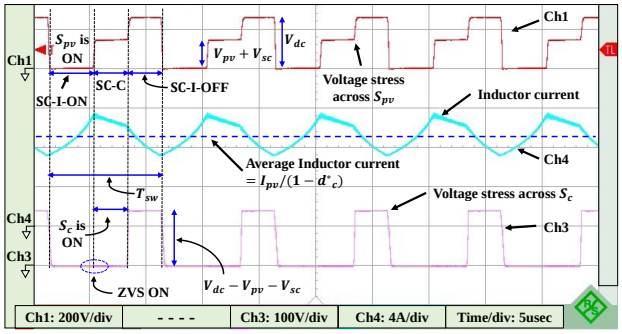


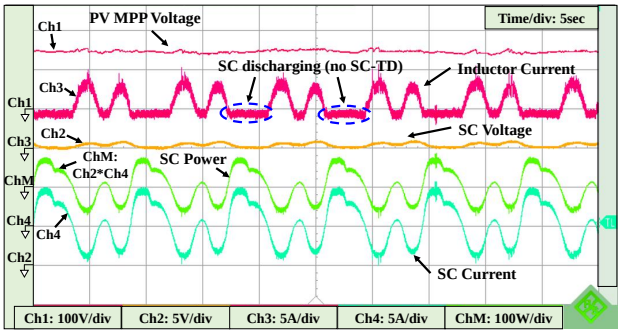
(c)



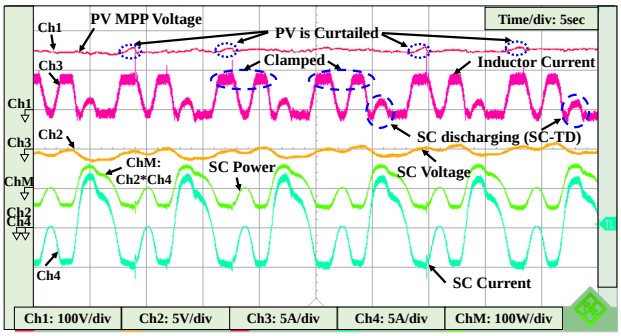
(d)

Fig. 10. The sequence of modes when the SC is (a) discharging ($d_d < d_{pv}$), (b) discharging ($d_d > d_{pv}$), (c) turbo discharging or (d) charging.

system adheres the regular discharging and charging pattern for the SC, following the mode sequence explained in Fig. 4(a)



(a)



(b)

Fig. 11. System performance during CFF: (a) Case 1: V_{sc0} = 15 V, (b) Case 2: V_{sc0} = 9 V. (Note: All the channels are sampled at 1 kHz.)

and Fig. 4(c) respectively. The SC voltage appears nearly unchanged over a period of few seconds due to (almost) net zero energy exchange at CFF. The undisturbed oscillation of the PV voltage around the MPP value of nearly 150 V demonstrates effective decoupling between PV and SC operation.

In Case 2, as illustrated in Fig. 11(b), the situation is similar, but now the operational limits becomes relevant due to the diminished SC voltage level. During discharging, SC-TD mode comes to the rescue adhering to the mode sequence shown in Fig. 4(b). During charging, however, $I^{ch}_{sc,pk}$ is clamped due to the inductor current limit $I^{ch}_{L,pk}$, which mobilises short-term PV curtailment to meet the SIR requirements.

B. PFR under UFE

The performance of the experimental prototype is studied in terms of PFR, subjecting it to the benchmark UFE event of Table I. Once again, two distinct cases of initial SC voltage are shown in Fig. 12: Case 1 with V_{sc0} = 15 V (normal level) and Case 2 with V_{sc0} = 8 V (reduced level due to prior UFE event).

In Case 1, Fig. 12(a) shows that the system adeptly handles the UFE ($P^{dis}_{sc,pk} \approx$ 105 W), as the high V_{sc0} ensures that none of the limits are breached. Observe how the inductor current surpasses the PV current level during the SC-TD mode at the peak of the UFE. Despite such an abrupt output power adjustment of approximately 16% within 2 seconds, the PV operating point remains undisturbed around the MPP. Ultimately, the SC gets discharged down to about 12 V by the end of the event.

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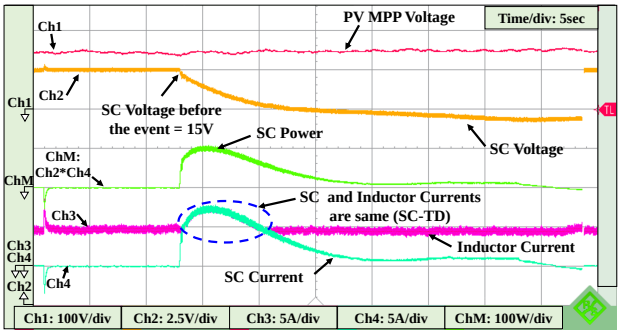
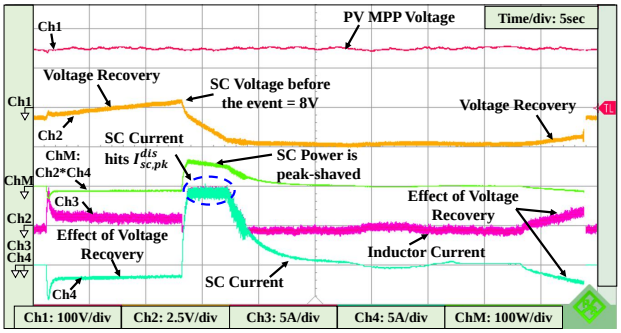


(a)



(b)

Fig. 12. System performance during UFE: (a) Case 1: V_{sc0} = 15 V, (b) Case 2: V_{sc0} = 8 V. (Note: All the channels are sampled at 1 kHz.)

Case 2 in Fig. 12(b) explores the scenario of subsequent back-to-back UFEs that discharge the SC to 8 V, before another UFE takes place. Because of the low voltage, the SC power is peak-shaved as the inductor current limit $I^{dis}_{L,pk}$ is hit despite being in SC-TD mode. A few seconds in the UFE, the V^{min}_{sc} limit is also reached, which brings the SC power to zero to protect the SC. Please also note the SC voltage recovery mechanism of Module F, which is clearly visible in this case study before and after the UFE. These results demonstrate that the PV/SC MPC not only addresses fully one UFE in accordance to the design specifications, but can also cope with multiple subsequent events, delivering quite descent performance.

C. PFR under OFE

This scenario considers two back-to-back OFEs, with an initial SC voltage V_{sc0} = 15 V, illustrated in Fig. 13. When the first event takes place, the SC charges quickly to mitigate the power surplus in the system, but there is still some PV curtailment at the peak of the event when the inductor current tops $I^{ch}_{L,pk}$. This is by design, as discussed earlier, to account for the charging limitations of the PV/SC MPC, which are effectively compensated by the PV curtailment function.

By the time of the second OFE, a small SC voltage headroom has been created by the voltage recovery function of Module F, which extinguishes quickly during the event, resulting in the spiky current and power profiles in Fig. 13. For the core of the event, the PFR is carried out via PV curtailment with the PV voltage visibly shifting away from the MPP value.

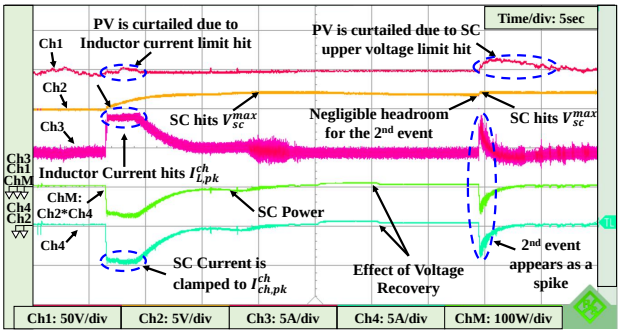


Fig. 13. System performance during OFE. (Note: All the channels are sampled at 1 kHz.)

TABLE VI. RMS AND AVERAGE CURRENT RATINGS

Switches	RMS Current	Diodes	Average Current
S_{pv}	$I_L\sqrt{d_{pv}}$	D_{dc}	$I_L(1-d_{pv}-d^*_{d2}-d^*_c)$
S_d	$I_L\sqrt{d_d}$	D_{bp}	$I_L(1-d_d)$
S_{d2}	$I_L\sqrt{d^*_{d2}}$	D_{d2}	$I_L d^*_{d2}$
S_c	$I_L\sqrt{d^*_c}$	D_c	$I_L d^*_c$

Overall, this scenario shows that the PV/SC MPC can handle an arbitrary number of subsequent OFEs despite a full SC bank, thanks to the flexibility provided by PV curtailment.

VI. Loss Analysis, Efficiency Calculation and Comparison with Prior Arts

This section conducts a detailed loss analysis of the proposed PV/SC MPC using mathematical expressions for the full range of PV and SC operation as discussed in section III followed by a comparison based on the features.

A. Loss Analysis of the proposed PV/SC MPC

The total loss L_{tot} of the converter can be expressed in Eq. (18) as the sum of total conduction losses L^{tot}_{con}, total switching losses L^{tot}_{sw} and the inductor loss L^{tot}_{ind}. For that, the rms and average current expressions for the switches and the diodes are stated in Table VI as a function of I_L (small ripple approximated) and duties of the switches (according to Table VII).

$$L_{tot} = L^{tot}_{con} + L^{tot}_{sw} + L^{tot}_{ind} \tag{18}$$

A generalised expression for d_{pv} irrespective of the modes of the operation can be given by

$$d_{pv} = \frac{\begin{array}{c}(V_{dc}-Vpv)(1-d^*_{d2}-d^*_c)+V_{sc}(d_d-d^*_c)\\ +V_d(2-d_d)+I_L(r_L+r_{on}(d_d+d^*_{d2}+d^*_c))\end{array}}{V_{dc}+V_d-I_L r_{on}} \tag{19}$$

where, r_L and r_{on} are the dc equivalent resistance of the inductor and on-state resistance of the switches respectively; whereas V_d stands for the forward voltage drop of the diodes.

Now, once the rms and average current expressions are known, the L^{tot}_{con} can be expressed as

$$L^{tot}_{con} = \sum I^2_X r_{on} + \sum I_Y V_d \tag{20}$$

TABLE VII. MODE DEPENDENT INDUCTOR CURRENT AND DUTIES

Variables	SC Idle	Discharging	Turbo-discharging	Charging
I_L	I_{pv}	I_{pv}	I_{sc}	$I_{pv} - I_{sc}$
d_d	0	$\frac{I_{sc}}{I_{pv}}$	1	0
d^*_{d2}	0	0	$\frac{I_{sc}-I_{pv}}{I_{sc}}$	0
d^*_c	0	0	0	$\frac{-I_{sc}}{I_{pv}-I_{sc}}$

where, X and Y stands for switches and diodes respectively. Similarly, L^{tot}_{sw} can be expressed as

$$L^{tot}_{sw} = \sum \frac{V^{on}_X I_L t_{on} F_{sw}}{2} + \sum \frac{V^{off}_X I_L t_{off} F_{sw}}{2} \quad (21)$$

where, the first and second terms define the total ON time (t_{on}) and OFF time (t_{off}) switching losses respectively; X denotes the switch type and $V^{on/off}_X$ is the voltage stress of the respective switch at the instant of ON/OFF. (Note: ON time losses for S_{d2} and S_c are zero due to ZVS operation).

Similarly, the total inductor loss can be expressed as the sum of inductor copper loss and the core loss (L^{core}_{ind}).

$$L^{tot}_{ind} = I^2_L r_L + L^{core}_{ind} \quad (22)$$

Eventually, the expression for efficiency η can be expressed as

$$\eta = \frac{P_{pv} + P_{sc} - L_{tot}}{P_{pv} + P_{sc}} \quad (23)$$

The loss and efficiency performance of PV/SC MPC is analysed and is shown in Fig. 14. The rating of the PV system in Table I, the FRS information in Table III and the capability of the converter from section III are considered here. Note that the PV is operated at STC and SC is at its SSV i.e., 34 V. The datasheet parameters of the SiC MOSFETs (r_{on}) and Schottky diodes (V_d) from Table V read 45 mΩ and 1.5 V respectively. The r_L of the inductor is calculated to be 18 mΩ and the associated core loss is calculated for four pieces of *N97:E/70/33/32* ferrite cores. For this core arrangement the datasheet reads 17.2 W for each core, corresponding to F_{sw}=100 kHz and peak Flux density=0.2 T.

As depicted from Fig. 14(a), the system is operating at nearly 98.15% efficiency when SC is idle. The efficiency profile improves slowly to 98.33% when I_{sc} approaches 1 PU (@$P_{sc} \approx$ 0.067 PU) during regular discharging mode. This improvement is due to the continuous replacement of D_{bp} with S_d in SC-D-ON/OFF modes. However, beyond 1PU, the efficiency decreases slowly till I_{sc} = 3 PU during turbo-discharge mode with a reasonable efficiency of 94.61% (@P_{sc} ≈ 0.2 PU). Beyond this point, it is clamped due to hitting the inductor current limit. The charging pattern also leads to fall in efficiency due to additional components on the current path. It becomes clamped at I_{sc} = -2 PU (@η = 94.56%) as the inductor current hits the limit (@$P_{sc} \approx$ -0.1 PU).

In Fig. 14(b), a better visualization of loss segregation among components for four different modes of operation when operated in their respective extreme limits (@I_{pv} = 1 PU and $V_{sc} = V^{SS}_{sc}$). It is observed that during regular PV operation, the total percentage loss is quite small (1.84%) due to low conduction loss of the switches and inductor. The regular discharge operation is slightly better (1.77%) as it experiences

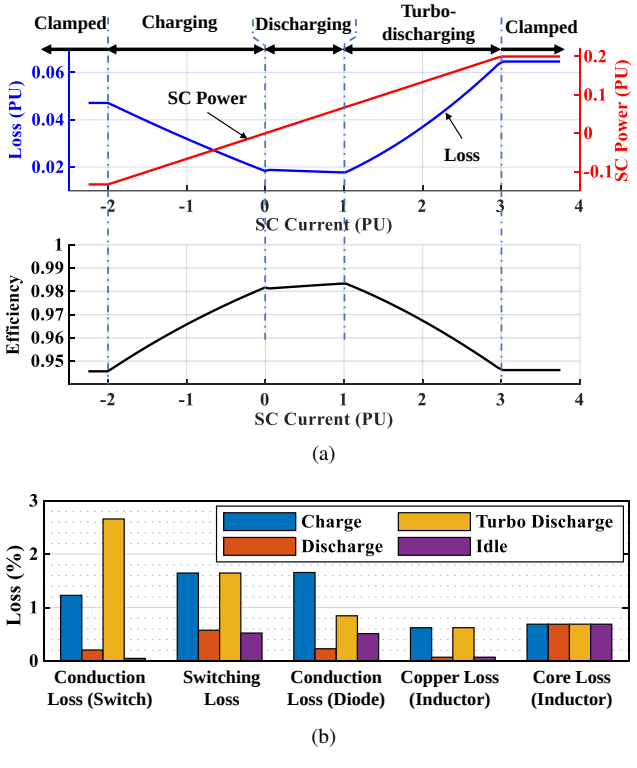


Fig. 14. Loss and Efficiency profile for the 10 kWp PV system under consideration during FRS: (a) for the entire range of SC operation, (b) Loss segregation among components during Charging ($I_{sc} = -2$ PU), Discharging (I_{sc} = 1 PU),Turbo-discharging (I_{sc} = 3 PU), and when Idle (I_{sc} = 0). (Note: PU is done considering nominal PV power).

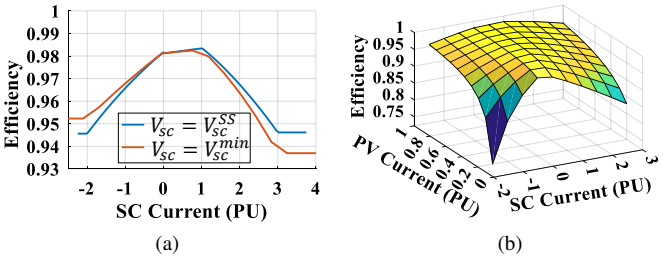


Fig. 15. Impact of (a) SC voltage and (b) PV current on converter Efficiency

lower diode losses than the regular operation. The loss during both charging (5.84%) and turbo-discharging (6.46%) modes of operation is quite comparable and a bit higher than in the previous modes. It is due to the higher conduction losses in most of the components and off-time switching losses in the switches. Conduction loss in the switches predominates compared to diodes during turbo-discharging, and the reverse is true during the charging operation.

In Fig. 15(a), the converter efficiency is studied for the two extreme limits of SC voltage (i.e. V^{ssv}_{sc} = 34 V and V^{min}_{sc} = 5 V). It is observed that SC voltage has a minor impact on the efficiency, mostly due to change in switching losses. Efficiency profile is also verified for the range of PV MPPT current (0.2 PU to 1 PU) @$V_{sc} = V^{SS}_{sc}$ as shown in Fig. 15(b). It shows that the efficiency graph is quite flat for the entire range of

TABLE VIII. COMPARISON OF THE PROPOSED PV/SC MPC WITH THE EXISTING NON-ISOLATED MULTI-PORT TOPOLOGIES

Grounds of comparison	[35]	[36]	[38]	[39]	[40]	[43]	[44]	[48]	[49]	PV/SC MPC
Switches	3	3	4	4	5	2	2	4	3	4
Diodes	3	3	4	5	1	4	3	4	3	4
Switches/Diodes conduct at any instant	2-3	3-4	4	3-5	2-3	3	2-3	4	2-3	2-3
No. of switches with Soft switching	1	1	0	4	3	0	1	0	1	2
Inductors	2	1	1		3	1	2	1	1	1
Coupled Inductors				1		1	1			
Series Capacitors	1					3	3			
Low voltage bidirectional port for ES				✓		✓	✓	✓	✓	✓
Wide voltage variation support			✓					✓	✓	✓
Bypassing possibility	✓	✓	✓	✓	✓			✓	✓	✓
Current Boosting capability of ES port						✓	✓	✓		✓

PV operation ($\eta = 98.15\%$; $@I_{pv} = 1$ PU and $\eta = 95.45\%$; $@I_{pv} = 0.2$ PU) when SC is idle. However, the efficiency falls during both charging and discharging with a reduction in PV output. The decrease in efficiency is quite steeper in case of charging with fall in PV output below 0.4 PU. This is mostly due to reduction in total converter output, while the total SC loss remains unchanged. Nonetheless, this is not an issue; during very low PV periods, curtailment of PV through control would be more efficient over charging the SC.

B. Comparison with Existing Non-isolated Multi-port Converters

A qualitative comparison of the proposed PV/SC MPC with the existing state-of-the art non-isolated multi-port topologies in terms of various aspects are summarized in Table VIII, aligning with the four main objectives of the article. These objectives primarily include: (1) a low-voltage bidirectional port for ES, (2) support for wide voltage variation in the SC, (3) the possibility of bypass when SC is idle, and most importantly, (4) the turbo-boosting (current-boosting) capability of the ES port. These papers are the closest match for this application, but they are not specifically designed for PV/SC hybridization. In terms of components, these topologies use 5-9 switches and diodes, and up to 2 inductors and 3 series capacitors; PV/SC MPC lies in the middle with 4 switches, 4 diodes and 1 inductor with the added benefit of only 2-3 conducting elements at any time with the benefit of ZVS ON in two switches and hence little power losses.

This is further supported by the loss analysis conducted in the preceding sub-section, where the efficiency profile ranges from 98.33% (highest during regular discharging) to 94.56% (lowest during charging). In terms of features, only PV/SC MPC is able to accommodate a variable low voltage ES that can be turbo-discharged when required and bypassed when not needed. Among all alternatives, the converter in [48] (refer to Fig. 8(b) of [48]) is the only case that fulfils all four main objectives like the proposed PV/SC MPC; however, it has a major drawback: more components in the current path, and none are soft-switched. Since, [49] is not having a current boosting mechanism, an oversized SC bank will be required to meet the discharge-related FRS needs.

This comprehensive comparison confirms the superiority of the proposed PV/SC MPC meeting all the desired objectives with the benefit of reasonable number of components and the option for soft-switching, resulting fair efficiency, it outperforms other closely related topologies in the literature, establishing its suitability for PV/SC hybridization.

VII. CONCLUSION

This paper introduces a compact approach to hybridize a small-scale PV system with SC for frequency response services. By incorporating only three additional switches (two switches are soft switched and one switch is low voltage switched) and three diodes into the standard PV boost converter, the proposed PV/SC multi-port converter utilizes the SC almost fully (upto $\approx 95.3\%$ of its stored energy) at high discharge rates. This results in approximately 1.5 times reduction of SC size compared to the previous approach [49] for the study case application. The accompanying control scheme implements the frequency response services for a grid-following system, ensuring effective decoupling of the PV and SC operation for robust dynamic performance.

Both simulation and the experimental findings illustrate the system's capability to achieve a peak SC power equivalent to 20% of the nominal PV power, effectively emulating a wide range of dynamically varying inertia constant (2 s to 9 s). However, the design section highlights potential for further enhancement by optimizing the trade-off between maximum inductor current and the size of the SC bank. These findings underscore the system's efficacy in meeting frequency response services requirements cost-effectively, employing turbo-discharging during under-frequency events, and temporarily reducing PV power during over-frequency events.

Beyond frequency response services, this topology may be leveraged for other services in PV systems, such as generation smoothing during solar irradiance fluctuations, PV ramp-rate control, fault-ride-through and voltage support to resistive grids etc. In addition, the PV/SC multi-port converter exhibits potential for deployment in PV grid-forming systems, where energy storage is a general requirement extending beyond frequency response services.

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APPENDIX

A. Clarification on Eqs. (4) and (5)

These equations are derived by applying volt-sec balance to the inductor (L) in three distinct modes of operation as outlined below ($\langle V_L \rangle$ is the average inductor voltage during a switching cycle):

1) During regular discharging ($0 \leq d_d \leq 1$)

$$\langle V_L \rangle = 0 \Longleftrightarrow V_{pv} + V_{sc} d_d - V_{dc} \left(1 - d_{pv}\right) \quad \text{(A1)}$$

2) During turbo-discharging ($d_d = 1 \;\&\; d_{pv} < d_{d2} \leq 1$)

$$\langle V_L \rangle = 0 \Longleftrightarrow V_{pv} \left(1 - d^*_{d2}\right) + V_{sc} - V_{dc} \left(1 - d_{pv} - d^*_{d2}\right) \quad \text{(A2)}$$

3) During charging ($d_{pv} < d_c \leq 1$)

$$\langle V_L \rangle = 0 \Longleftrightarrow V_{pv} \left(1 - d^*_c\right) - V_{sc} d^*_c - V_{dc} \left(1 - d_{pv} - d^*_c\right) \quad \text{(A3)}$$

On appling superposition theorem to Eqs. (A1) to (A3) results in a generalized equation presented below:

$$\begin{aligned} \langle V_L \rangle = 0 \Longleftrightarrow & V_{pv} \left(1 - d^*_{d2} - d^*_c\right) + V_{sc} \left(d^*_{d2} - d^*_c\right) \\ & - V_{dc} \left(1 - d_{pv} - d^*_{d2} - d^*_c\right) \end{aligned} \quad \text{(A4)}$$

Upon further manipulation of Eq. (A4), we arrive at two equations identical to Eq. 4 and Eq. 5 in the manuscript.

B. Clarification on Eqs. (6) to (8)

These expressions are derived from the standard formula for energy stored in a capacitor ($E = 0.5CV^2$). By considering the lowest bound in the SC voltage $\left(V_{sc}^{min}\right)$, the minimum required voltage of the SC pack (V_{sc}^{req}) can be deducted from the worst-case energy requirement (E_{sc}^{tot}), as expressed below:

$$\begin{aligned} E_{sc}^{tot} &= \left[0.5 \left(\frac{C_{sc}^{nom}}{N_{sc}}\right) \left(V_{sc}^{req\,2} - V_{sc}^{min\,2}\right)\right] \\ &\leq \\ E_{sc}^{nom} &= \left[0.5 \left(\frac{C_{sc}^{nom}}{N_{sc}}\right) \left(V_{sc}^{nom\,2} N_{sc}\right)\right] \end{aligned} \quad \text{(B1)}$$

Where, C_{sc}^{nom} and V_{sc}^{nom} represent the nominal capacitance and voltage, respectively, of the single unit of SC module, as specified in Table III of the manuscript. Additionally, N_{sc} denotes for the number of SC modules required to fulfill the demand. E_{sc}^{tot} and E_{sc}^{nom} stands for the total energy demand from the SC vs nominal energy rating of the SC bank to be sized respectively.

Further solving Eq. (B1) results in Eq. (6) and yields the quadratic inequality presented in Eq. (7) in the manuscript. Obtaining the positive root of Eq. (7) and rounding it up to the nearest higher integer value will furnish the value of Nsc as in Eq. (8) of the manuscript.

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