Space Vector Modulation With Common-Mode Voltage Elimination and Switching Frequency Minimization for Multilevel Converters

Qingle Sun, *Student Member, IEEE,* Suleiman M. Sharkh, *Senior Member, IEEE,* Zhifu Wang, Zeshang Wang, *Student Member, IEEE,* and Guobiao Shi

***Abstract*—This paper proposes novel space vector pulse width modulation (SVPWM) strategies for multilevel converters to achieve two widely desired optimization objectives, common-mode voltage (CMV) elimination and switching frequency minimization (SFM). For CMV elimination, a new coordinate system that looks like the cropped version of the original *abc* frame is proposed, by which zero CMV can be ensured when the identified switching states are transformed from the new frame back into the original one. For SFM, a new approach is proposed to determine the optimal switching sequence, where a voltage reference point dwell mechanism is introduced such that the number of switching actions between adjacent switching periods is minimized by establishing its relationship with a unique variable, namely the number of level shifts. Furthermore, these two objectives can either be implemented independently or in combination to achieve SFM under the premise of CMV elimination, thus allowing the converter's redundancy to be fully exploited. Simulation and experimental results validate the proposed strategies.**

***Index Terms*—Common-mode voltage (CMV) elimination, multilevel converter, space vector pulse width modulation (SVPWM), switching frequency minimization (SFM).**

I. Introduction

MULTILEVEL converters offer lower total harmonic distortion (THD), higher efficiency, reduced electromagnetic interference and lower *dv/dt* than their two-level counterparts [1]–[4]. They have therefore been widely used in electric vehicles, marine propulsion and photovoltaic power generation systems [5], [6]. However, the increased number of switching devices places higher demands on the modulation strategy and the digital controller. Various pulse width modulation (PWM) techniques have been proposed, including carrier-based PWM [7]–[9], space vector PWM (SVPWM) [10]–[12], and nearest level modulation [13], [14]. SVPWM is arguably a more powerful and promising solution for multilevel converters than other methods because it provides a more efficient utilization of the dc voltage, and more importantly, it allows for optimization of the converter's performance through a judicious selection of switching states from the range of available redundant switching states (RSSs) [10].

Despite the significant advantages offered by SVPWM, its high computational and memory requirements hinder its application. Simplified SVPWM strategies have thus been developed: carrier-based implementations [15]–[17], two-level SVPWM-based methods [18]–[23], and non-orthogonal coordinate system-based methods [4], [24]–[29]. In carrier-based implementations, the reference voltages are typically injected with a predefined zero-sequence component; they are then compared with level-shifted [15], [16] or phase-shifted [17] carriers to produce an equivalent output to SVPWM. The main advantage of this approach is that it considerably simplifies the calculation of duty cycles and can naturally generate switching sequences with a minimum number of switching actions within each cycle. However, it does not make efficient use of the RSSs to reduce common-mode voltage (CMV) and switching losses.

In two-level SVPWM-based methods, the reference voltage vector (RVV) is normally decomposed into an offset vector whose tip is located at the center of a two-level hexagon within the multilevel space vector diagram (SVD), and a remainder vector that can be synthesized in a similar way to two-level SVPWM. In [19], the two-level hexagon containing the tip of the offset vector is identified based on the vector's angle by iteratively locating the centers of the nested set of multilevel hexagons enclosing it. A somewhat similar approach can be found in [20], which decomposes the multilevel SVD into its constituent two-level hexagons and identifies the one where the RVV lies. However, both methods involve iterative calculations to locate the desired two-level hexagon, and the increased number of iterations with the number of levels inevitably leads to a rapidly rising computational burden. In [21], [22], the offset vector is determined by directly rounding down the RVV coordinates, which avoids iterative computation and lookup tables, but may result in underutilizing the RSSs to reduce CMV and switching losses. Furthermore, these methods typically involve complex programming of the duty cycles and their respective switching states in the generation of the switching sequence [23], which increases memory requirements.

Other approaches transform the RVV along with the switching vectors from an original orthogonal $\alpha\beta$ or *abc* coordinate system to a non-orthogonal one such as 45° coordinate [4], 60°

This work was supported in part by the National Natural Science Foundation of China under Grant 52075039. (*Corresponding author: Zhifu Wang.)*

Qingle Sun, Zhifu Wang, Zeshang Wang, and Guobiao Shi are with the National Engineering Research Center of Electric Vehicles, School of Mechanical Engineering, Beijing Institute of Technology, Beijing 100081, China (e-mail: sunqingle@bit.edu.cn; wangzhifu@bit.edu.cn; wangzeshang@bit.edu.cn; sgb@bit.edu.cn).

Suleiman M. Sharkh is with the Mechatronics Research Group, Faculty of Engineering and Physical Sciences, University of Southampton, Southampton SO171BJ, U.K. (e-mail: suleiman@soton.ac.uk).

coordinate [24]–[26], line voltage coordinate [27], [28], and so forth [29]. Through coordinate transformation, the RSSs in the original coordinate system are mapped to a single switching state with integer coordinates in the non-orthogonal frame, which simplifies the identification of the triangle containing the RVV and the calculation of the duty cycles. The most widely used is the 60° hexagonal coordinate system [25], in which the switching states of the nearest three vectors (NTVs) can be readily obtained by rounding the RVV coordinates down or up in conjunction with judging the type of triangle formed by the NTVs, and the duty cycles are directly derived from simple arithmetic operations. However, the switching states identified in non-orthogonal frames typically need to be transformed back into the original coordinate system to produce the final output. In this process, the RSSs inevitably reappear as the original coordinate system emerges [24]–[28]. Thus, it is still necessary to consider the impact of all RSSs on the converter's performance and to select the optimal states, a step that is usually computationally intensive.

Several SVPWM strategies combining different modulation algorithms have also been studied. In [3], the interrelationship between SVPWM and nearest level modulation is explored, and a generalized and simple approach is presented to calculate the duty cycles. In [23], nearest level modulation-based implementation is introduced into the two-level SVPWM-based method, such that complex programming to generate the switching sequence is avoided. In [30], the three-phase components are decoupled to equal leg voltages and phase voltages by selecting a specific switching state as the offset vector. On this basis, the two-level SVPWM-based method and carrier-based implementation are combined to achieve high flexibility and low complexity. Although these existing methods exploit SVPWM from different aspects, most of them use the NTVs to synthesize the RVV. When the non-NTVs are the desired output, such as in CMV elimination, these methods may no longer be applicable.

The possibility of using RSSs to optimize converter's operation is one of the distinct advantages of SVPWM. CMV suppression has become a subject of great interest due to its detrimental effects in terms of electromagnetic interference, bearing currents, power loss, and insulation protection [12], [30], [31]. In [31], [32], only the switching states with the minimal CMV magnitude in the NTVs are selected, by which the CMV peak in most cases can be exactly reduced to 1/3 of the dc voltage step. In [26], time-averaged CMV cancellation is achieved by introducing a fourth switching state and redistributing the duty cycles, but the CMV peak increases to 2/3 of the dc voltage step. These two objectives are also implemented in [30] by establishing their relationships with available voltage reference points (RPs). However, both objectives can only reduce the CMV to a certain extent, so its negative effects cannot be completely eradicated.

In [33], the switching states with zero CMV are extracted to form a new SVD, and complete CMV elimination is achieved by synthesizing the RVV in it. Nevertheless, triangle identification and lookup tables are required to determine the switching states and duty cycles, increasing computational and storage complexity. Selecting the non-NTVs with zero CMV as output to completely eliminate CMV can also be found in [34], but the details of how to determine the desired switching states and duty cycles is not presented. In [4], the reference phase voltages are conveniently considered as line voltages, and the switching states with zero CMV are then identified based on the new reference in a 45° frame. However, there is not a systematic procedure for determining the switching sequence, which can potentially increase the device switching frequency considerably. Besides, these methods are typically only used to achieve a single control objective, and they may not be applicable to other objectives such as switching frequency minimization (SFM).

Device switching frequency is critical in terms of switching losses, device lifetime and electromagnetic interference [31]. In [22], the number of switching actions in each switching period is minimized by sorting the switching states according to the sum of their coordinates. The same optimization is conducted in [19] through second mapping on the basis of region identification of the remainder vector. Nonetheless, neither of them considers the number of switching actions between adjacent periods. In [31], the switching losses between adjacent periods are minimized by introducing a cost function to evaluate available switching sequences, but it is only applicable in the context of minimal CMV magnitude. In [20], SFM is achieved by simultaneously minimizing the number of switching actions within and between switching periods, but it needs to compare all available RSSs at each switch change, leading to high computational complexity.

This paper proposes flexible and efficient SVPWM strategies, and the main contributions are summarized as follows.

1) Complete CMV elimination instead of limited CMV suppression [26], [30]–[32] is accomplished by introducing a new coordinate system, by which the desired non-NTVs can be readily derived using existing NTVs-based methods without complex region identification and lookup tables [33].
2) Global SFM not local SFM [19], [22] is achieved both within and between switching periods by simple logical judgment and arithmetic calculation without multiple comparisons and lookup tables [20], in which a voltage RP dwell mechanism is proposed to establish the relationship between the number of switching actions and a unique variable, i.e., the number of level shifts.
3) These two optimization objectives are skillfully combined to achieve SFM in the context of CMV elimination, which allows the converter's redundancy to be fully utilized, thus providing higher flexibility.

The rest of this paper is organized as follows. Section II describes a candidate multilevel converter system and the existing problems. The proposed strategies are detailed in Section III. Section IV evaluates the linear modulation range of the proposed strategies. Section V presents simulation results and experimental validation. Section VI concludes the paper.

II. Problem Formulation

A. System Configuration

As shown in Fig. 1, an n-level cascaded H-bridge (CHB) converter is selected as the study case. The number of voltage

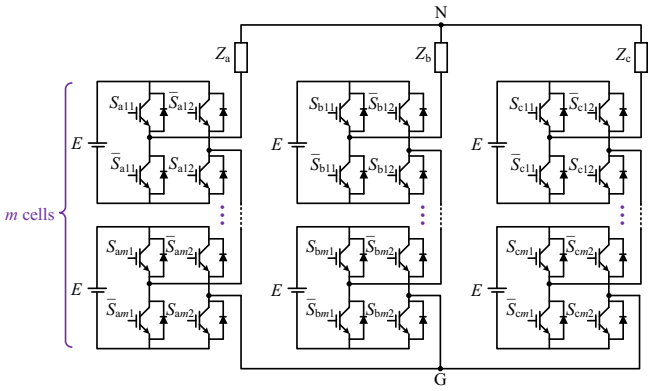

Fig. 1. The n-level three-phase CHB converter.

levels n determines the number of H-bridge cells per phase as $m = (n-1)/2$. Each cell can offer three dc voltages $\{-E, 0, E\}$, normalized as $\{0, 1, 2\}$. The voltage levels of each phase can thus be designated as $\{0, 1, 2, ..., n-1\}$, which constitute n^3 switching states $(S_\mathrm{a}, S_\mathrm{b}, S_\mathrm{c})$ in three phases.

In this paper, the voltage space vector is defined as [19]

$$\boldsymbol{V}_\mathrm{out} = V_\mathrm{dc}(S_\mathrm{a} + S_\mathrm{b}e^{j\frac{2}{3}\pi} + S_\mathrm{c}e^{j\frac{4}{3}\pi}) \tag{1}$$

where $V_\mathrm{dc} = (n-1)E$ for CHB converters.

As an example, a five-level SVD in the *abc* coordinate system is shown in Fig. 2. For two-level SVPWM-based methods, the RVV $\boldsymbol{V}_\mathrm{ref}$ in Fig. 2 can be synthesized as

$$\begin{aligned}\boldsymbol{V}_\mathrm{ref} &= d_1\boldsymbol{OQ} + d_2\boldsymbol{OR} + (1-d_1-d_2)\boldsymbol{OP} \\ &= \boldsymbol{OP} + d_1\boldsymbol{PQ} + d_2\boldsymbol{PR} \\ &= \underbrace{\boldsymbol{OP}}_{\boldsymbol{V}_\mathrm{off}} + \underbrace{\boldsymbol{PS}}_{\boldsymbol{V}_\mathrm{rmd}}\end{aligned} \tag{2}$$

where $\boldsymbol{V}_\mathrm{off}$ and $\boldsymbol{V}_\mathrm{rmd}$ are defined as the offset vector and the remainder vector, respectively, and d_1 and d_2 represent the duty cycles. Clearly, the combination of these two vectors is not unique: $(\boldsymbol{OQ}, \boldsymbol{QS})$ and $(\boldsymbol{OR}, \boldsymbol{RS})$ can also be taken as $(\boldsymbol{V}_\mathrm{off}, \boldsymbol{V}_\mathrm{rmd})$. Once the vector combination is determined, the remainder vector can be synthesized in a similar way to two-level SVPWM to calculate the duty cycles and consequently generate the switching sequence.

B. Problem Analysis

A modulation scheme combining the two-level SVPWM-based method and carrier-based implementation presented in [30] is used to illustrate the existing problems. As explained below, the stated problems exist in most conventional SVPWM methods, such as in [18], [19], [21]–[32].

1) Calculating RVV Coordinates: As the coordinates $(S_\mathrm{a,ref}, S_\mathrm{b,ref}, S_\mathrm{c,ref})$ and $(S_\mathrm{a,ref}+\alpha, S_\mathrm{b,ref}+\alpha, S_\mathrm{c,ref}+\alpha)$ $(\alpha \in \mathbb{R})$ in the SVD point to the same voltage vector, a voltage RP is introduced to link reference phase voltages $v_{x,\mathrm{ref}}$ and RVV coordinates $S_{x,\mathrm{ref}}$ $(x \in \{\mathrm{a}, \mathrm{b}, \mathrm{c}\})$, which denotes a point on the converter side with the same potential as the neutral point, such that reference phase voltages are transformed to reference leg voltages, and the RVV coordinates can be calculated based on reference leg voltages as

$$S_{x,\mathrm{ref}} = (v_{x,\mathrm{ref}} - v_\mathrm{min})/E \tag{3}$$

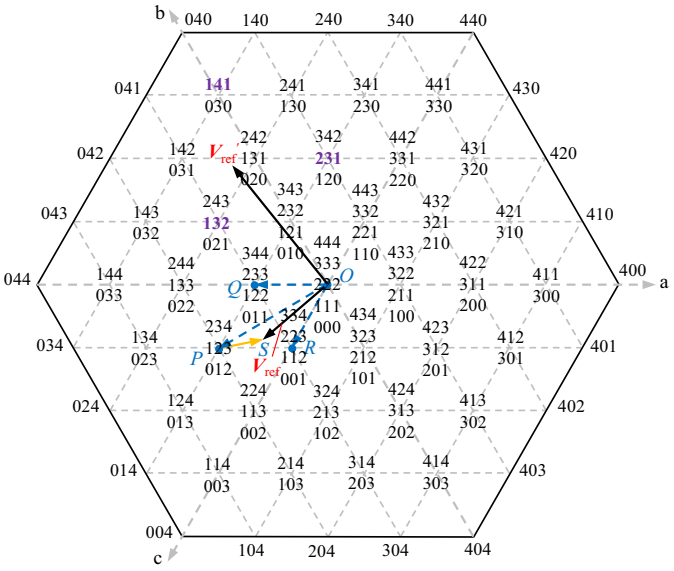

Fig. 2. SVD of the five-level CHB converter.

where v_min is the minimum leg voltage per phase, and point G in Fig. 1 is first chosen as the RP to derive $S_{x,\mathrm{ref}}$, namely $v_\mathrm{min} = -V_\mathrm{dc}/2$. Based on (3), different RVV coordinates can be obtained by regulating the selected RP, i.e., v_min.

2) Phase Decoupling of the Vectors: The switching vector nearest to the RVV is then taken as the offset vector to decompose the RVV, and the coordinates $S_{x,\mathrm{nst}}$ and $R_{x,\mathrm{nst}}$ of the offset and remainder vectors are calculated as

$$\begin{cases} S_{x,\mathrm{nst}} = \mathrm{round}(S_{x,\mathrm{ref}}) \\ R_{x,\mathrm{nst}} = S_{x,\mathrm{ref}} - S_{x,\mathrm{nst}} \end{cases} \tag{4}$$

where $\mathrm{round}(S_{x,\mathrm{ref}})$ represents the integer nearest to $S_{x,\mathrm{ref}}$.

However, the three-phase components of both vectors derived from (4) are coupled, that is, the leg and phase voltages defined by either vector are not equal, which brings indefinite vector coordinate relationship, complex sequence programming, and limited modulation range or switching pattern [30]. To decouple the three-phase components, the coordinates of a certain phase derived from (4) are modified as

$$\begin{cases} S_j = S_{j,\mathrm{nst}} + R_\mathrm{sum} \\ R_j = S_{j,\mathrm{ref}} - S_\mathrm{j} \end{cases}, \ \text{for } j = \underset{x=\mathrm{a,b,c}}{\arg\max}\{|R_{x,\mathrm{nst}}|\} \tag{5}$$

where $|\cdot|$ is the absolute value function, and R_sum represents the sum of $\{R_\mathrm{a,nst}, R_\mathrm{b,nst}, R_\mathrm{c,nst}\}$, $R_\mathrm{sum} \in \{-1, 0, 1\}$.

By this means, the resulting offset vector will satisfy

$$S_\mathrm{sum} = S_\mathrm{a} + S_\mathrm{b} + S_\mathrm{c} = 1.5(n-1). \tag{6}$$

3) Calculating Redundant Vector Combinations: For a given RVV, the vector combination determined previously is unique. In order to provide high flexibility, a dynamic RP mechanism is introduced based on (3).

If a new virtual point is selected as the RP such v_min changes by Δv, the new coordinates can be calculated by (3), and the new vector combination can be derived from (4) and (5). It can be readily shown that the new offset vector satisfies

$$S_\mathrm{a}' + S_\mathrm{b}' + S_\mathrm{c}' = 1.5(n-1) - 3\Delta v/E \in \mathbb{N}. \tag{7}$$

TABLE I
AVAILABLE COMBINATIONS OF THE OFFSET AND REMAINDER VECTORS

n_s	(S_a, S_b, S_c)	(R_a, R_b, R_c)	Offset Vec.	Remainder Vec.
-5	(3, 4, 4)	(0.067, -0.433, 0.366)	***OQ***	***QS***
-4	(3, 3, 4)	(-0.267, 0.233, 0.034)	***OR***	***RS***
-3	(2, 3, 4)	(0.4, -0.1, -0.3)	***OP***	***PS***
-2	(2, 3, 3)	(0.067, -0.433, 0.366)	***OQ***	***QS***
-1	(2, 2, 3)	(-0.267, 0.233, 0.034)	***OR***	***RS***
0	(1, 2, 3)	(0.4, -0.1, -0.3)	***OP***	***PS***
1	(1, 2, 2)	(0.067, -0.433, 0.366)	***OQ***	***QS***
2	(1, 1, 2)	(-0.267, 0.233, 0.034)	***OR***	***RS***
3	(0, 1, 2)	(0.4, -0.1, -0.3)	***OP***	***PS***
4	(0, 0, 2)	(0.067, -0.433, 0.366)	***OQ***	***QS***
5	(0, 0, 1)	(-0.267, 0.233, 0.034)	***OR***	***RS***

Equation (7) shows that Δv should fulfill

$$\Delta v = n_s E/3 \tag{8}$$

where n_s is defined as the number of level shifts, $n_s \in \mathbb{Z}$. The value of n_s quantitatively represents the selected voltage RP.

By substituting (8) into (3) and (7), the new RVV coordinates and the new offset vector can be expressed as

$$S_{x,\mathrm{ref}}{}' = S_{x,\mathrm{ref}} - n_s/3 \tag{9}$$

$$S_a{}' + S_b{}' + S_c{}' = 1.5(n-1) - n_s. \tag{10}$$

Based on (9) and (10), different vector combinations can be acquired by selecting different RPs (i.e., regulating n_s). Considering $\boldsymbol{V}_{\mathrm{ref}}$ with ($v_{a,\mathrm{ref}}$, $v_{b,\mathrm{ref}}$, $v_{c,\mathrm{ref}}$) = (-0.6E, -0.1E, 0.7E) in Fig. 2, the offset and remainder vectors at $n_s = 0$ can be obtained as (1, 2, 3) and (0.4, -0.1, -0.3) from (3)–(5). Then, the coordinates of these two vectors at other values of n_s can be calculated by (9), (4), and (5) in sequence, as shown in Table I. Clearly, a one-to-one correspondence between all available vector combinations as well as all possible switching states of the NTVs and the values of n_s is established, converting the selection of the optimal vector combination to the identification of the optimal n_s (denoted as $n_{s,\mathrm{opt}}$).

4) Generating the Switching Sequence: After $n_{s,\mathrm{opt}}$ is selected, the calculation of the duty cycles and the generation of the switching sequence normally follow immediately. To simplify implementation, carrier-based modulation is introduced. Consider $\boldsymbol{V}_{\mathrm{ref}}$ in Fig. 2 with $n_{s,\mathrm{opt}}$ = 0, i.e., (1, 2, 3) and (0.4, -0.1, -0.3) as the selected vector combination.

Essentially, phase decoupling makes the leg voltages defined by the offset vector equal to its phase voltages through selecting the switching state with a specific coordinate relationship [see (10)] as the offset vector. In this way, the phase voltages defined by the offset vector can be generated by directly outputting corresponding leg voltages, i.e., outputting the switching state of the offset vector. Thus, carrier-based implementation for the offset vector is shown in Fig. 3(a).

For the remainder vector with fractional coordinates, it can be synthesized by two-level SVPWM. In this case, carrier-based implementation can also be utilized by injecting a zero-sequence component as

$$u_x = R_x + v_z \tag{11}$$

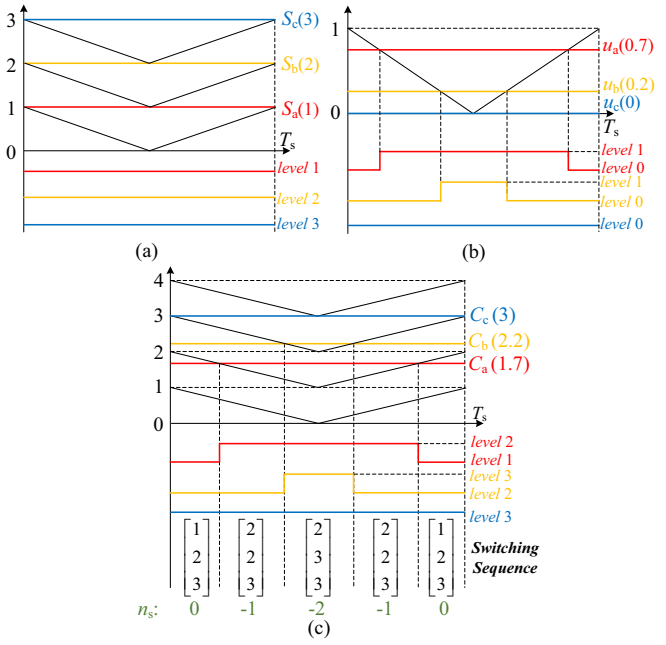

Fig. 3. Carrier-based modulation for the generation of the switching sequence. (a) For offset vector. (b) For remainder vector. (c) Final implementation.

where

$$v_z = \lambda - \lambda R_{\max} - (1-\lambda) R_{\min} \tag{12}$$

and $R_{\max}$ and $R_{\min}$ denote the maximum and minimum values in $\{R_a, R_b, R_c\}$, respectively, and λ stands for the distribution factor of the zero vector, $0 \le \lambda \le 1$. The discontinuous modulation with $\lambda = 0$ is shown in Fig. 3(b).

By combining Figs. 3(a) and (b), the final implementation can be shown in Fig. 3(c), and the final comparison values with the level-shifted carriers can be explicitly derived as

$$C_x = S_x + u_x \tag{13}$$

Problem 1: According to [35], the CMV of any switching state (S_a, S_b, S_c) can be expressed as

$$V_{\mathrm{CM}} = \frac{S_a + S_b + S_c - 1.5(n-1)}{3} E. \tag{14}$$

Clearly, the switching state with zero CMV should satisfy (6), namely $n_s = 0$ according to (10). Since there is a one-to-one correspondence between all switching states of the NTVs and the values of n_s, at most one switching state with n_s = 0 in the NTVs is available. Thus, complete CMV elimination cannot be achieved in the NTVs-based methods [18], [19], [21]–[32]. An obvious solution is to synthesize the RVV using the non-NTVs with zero CMV, but this poses two immediate issues: 1) how to efficiently choose the desired ones from the numerous switching states; 2) the existing NTVs-based methods may no longer be applicable.

Problem 2: Similar to that in [18], [19], [21]–[32], the number of switching actions is minimized in [30] within each cycle for a given λ by carrier-based implementation, as shown in Fig. 3(c), but it can be potentially high between adjacent cycles. According to Fig. 3(c), the first and last switching states in the switching sequence are the same and equal

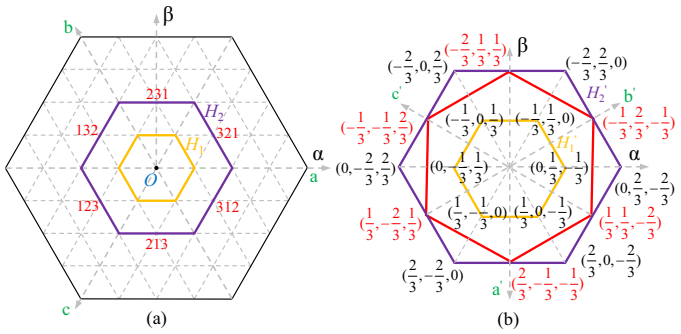

Fig. 4. (a) Five-level SVD in the OCS. (b) Switching vectors in the new coordinate system transformed from the hexagons H_1 and H_2.

$(\text{int}\,(C_\text{a})\,, \text{int}\,(C_\text{b})\,, \text{int}\,(C_\text{c}))$. Thus, the number of switching actions between adjacent cycles can be expressed as

$$N_\text{sw}(t+1) = \sum_{x=\text{a,b,c}} |\text{int}\,(C_x(t+1)) - \text{int}\,(C_x(t))| \quad (15)$$

where $\text{int}\,(C_x)$ denotes the largest integer not greater than C_x. According to (11)–(13), for $\lambda = 1$, there is always one phase satisfying $u_x = 1$, and thus $\text{int}\,(C_x) = S_x + 1$; for $\lambda < 1$, all $\text{int}\,(C_x)$ are equal to S_x since $u_x < 1$ except in the special case of $R_\text{max} - R_\text{min} = 1$. Hence, the change in coordinates of the offset vector directly reflects the number of switching actions between adjacent cycles for $\lambda < 1$. For the sake of illustration, $\lambda < 1$ is considered. Clearly, if the RVVs are located in the same triangle in adjacent cycles, the same offset vector should be chosen to avoid switching actions; if they lie in two distinct triangles, the offset vector that produces the smallest coordinate difference should be selected to minimize the number of switching actions; otherwise, extra unwanted switching actions will occur to increase the device switching frequency. However, this is yet to be implemented in a systematic manner.

III. Proposed SVPWM Strategies

A. Complete CMV Elimination

In this section, a new coordinate system is introduced to achieve complete CMV elimination, which allows the non-NTVs with zero CMV to be readily obtained using NTVs-based methods through coordinate transformation.

The proposed scheme draws on the idea of the line voltage coordinate system [27], which can be expressed as

$$\begin{bmatrix} v_\text{bc} \\ v_\text{ca} \\ v_\text{ab} \end{bmatrix} = \mathbf{T}_\text{p2l} \begin{bmatrix} v_\text{a} \\ v_\text{b} \\ v_\text{c} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} v_\text{a} \\ v_\text{b} \\ v_\text{c} \end{bmatrix}. \quad (16)$$

Since the transformation matrix $\mathbf{T}_\text{p2l}$ is not of full rank, its inverse matrix cannot be calculated directly. For a balanced three-phase system, an additional constraint that the sum of phase voltages is zero can be taken into account, such that the inverse transformation can be derived as

$$\begin{bmatrix} v_\text{a} \\ v_\text{b} \\ v_\text{c} \end{bmatrix} = \mathbf{T}_\text{l2p} \begin{bmatrix} v_\text{bc} \\ v_\text{ca} \\ v_\text{ab} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 0 & -1 & 1 \\ 1 & 0 & -1 \\ -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_\text{bc} \\ v_\text{ca} \\ v_\text{ab} \end{bmatrix}. \quad (17)$$

TABLE II
Mapping Relationship Between Switching States and Their CMV Values From the Hexagons H_1 and H_2

Transformed	Original	CMV	Transformed	Original	CMV
(0, 1/3, -1/3)	(1, 0, 0)	-5*E*/3	(-1/3, 1/3, 0)	(1, 1, 0)	-4*E*/3
	(2, 1, 1)	-2*E*/3		(2, 2, 1)	-*E*/3
	(3, 2, 2)	*E*/3		(3, 3, 2)	2*E*/3
	(4, 3, 3)	4*E*/3		(4, 4, 3)	5*E*/3
(-1/3, 0, 1/3)	(0, 1, 0)	-5*E*/3	(0, -1/3, 1/3)	(0, 1, 1)	-4*E*/3
	(1, 2, 1)	-2*E*/3		(1, 2, 2)	-*E*/3
	(2, 3, 2)	*E*/3		(2, 3, 3)	2*E*/3
	(3, 4, 3)	4*E*/3		(3, 4, 4)	5*E*/3
(1/3, -1/3, 0)	(0, 0, 1)	-5*E*/3	(1/3, 0, -1/3)	(1, 0, 1)	-4*E*/3
	(1, 1, 2)	-2*E*/3		(2, 1, 2)	-*E*/3
	(2, 2, 3)	*E*/3		(3, 2, 3)	2*E*/3
	(3, 3, 4)	4*E*/3		(4, 3, 4)	5*E*/3
(0, 2/3, -2/3)	(2, 0, 0)	-4*E*/3	**(-1/3, 2/3, -1/3)**	(2, 1, 0)	-*E*
	(3, 1, 1)	-*E*/3		**(3, 2, 1)**	**0**
	(4, 2, 2)	2*E*/3		(4, 3, 2)	*E*
(-2/3, 2/3, 0)	(2, 2, 0)	-2*E*/3	**(-2/3, 1/3, 1/3)**	(1, 2, 0)	-*E*
	(3, 3, 1)	*E*/3		**(2, 3, 1)**	**0**
	(4, 4, 2)	4*E*/3		(3, 4, 2)	*E*
(-2/3, 0, 2/3)	(0, 2, 0)	-4*E*/3	**(-1/3, -1/3, 2/3)**	(0, 2, 1)	-*E*
	(1, 3, 1)	-*E*/3		**(1, 3, 2)**	**0**
	(2, 4, 2)	2*E*/3		(2, 4, 3)	*E*
(0, -2/3, 2/3)	(0, 2, 2)	-2*E*/3	**(1/3, -2/3, 1/3)**	(0, 1, 2)	-*E*
	(1, 3, 3)	*E*/3		**(1, 2, 3)**	**0**
	(2, 4, 4)	4*E*/3		(2, 3, 4)	*E*
(2/3, -2/3, 0)	(0, 0, 2)	-4*E*/3	**(2/3, -1/3, -1/3)**	(1, 0, 2)	-*E*
	(1, 1, 3)	-*E*/3		**(2, 1, 3)**	**0**
	(2, 2, 4)	2*E*/3		(3, 2, 4)	*E*
(2/3, 0, -2/3)	(2, 0, 2)	-2*E*/3	**(1/3, 1/3, -2/3)**	(2, 0, 1)	-*E*
	(3, 1, 3)	*E*/3		**(3, 1, 2)**	**0**
	(4, 2, 4)	4*E*/3		(4, 2, 3)	*E*

Based on (16), it can be deduced that the sum of the transformed line voltages is zero regardless of the phase voltages thanks to the matrix property of $\mathbf{T}_\text{p2l}$. Inspired by this, the RVV can first be transformed from the original *abc* coordinate system (OCS) to a new one via $\mathbf{T}_\text{l2p}$ instead of the line voltage one via $\mathbf{T}_\text{p2l}$, and the switching states used to synthesize the new RVV can then be determined in the new frame. When these switching states are transformed from the new frame back into the OCS by $\mathbf{T}_\text{p2l}$, its matrix property apparently ensures that the sum of the coordinates of each counterpart is zero. Further, if an offset of $(n-1)/2$ is added to each coordinate, each final switching state will satisfy $S_\text{sum} = 1.5(n-1)$, i.e., zero CMV.

According to Fig. 2, an implicit prerequisite in the previous process is that the final switching states must all be in integer form within the range of $[0 \;\; n-1]$; otherwise, they will be inaccessible and meaningless. Hence, the right switching states in the new coordinate system need to be identified. Considering the switching vectors on the hexagons H_1 and H_2 in the OCS in Fig. 4(a), their counterparts in the new coordinate system can be derived by $\mathbf{T}_\text{l2p}$, as shown in Fig. 4(b), and the mapping relationship between switching states

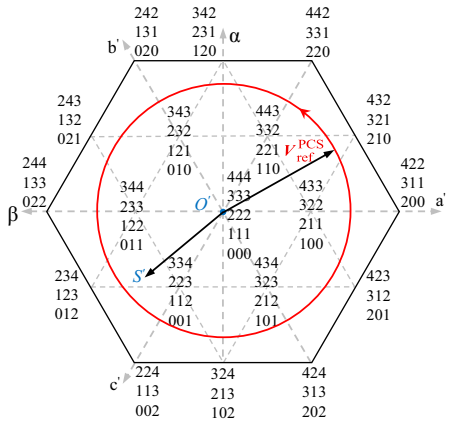

Fig. 5. Simplified SVD in the PCS.

and their CMV values are given in Table II. Obviously, the switching states in the new coordinate system are in fractional form, which undoubtedly complicates the identification of the required switching states.

As shown in Fig. 4 and Table II, the RSSs of a switching vector in the OCS correspond to the same switching state in the new coordinate system, as $\mathbf{T}_{\mathrm{l2p}}$ is not of full rank. Since $\mathbf{T}_{\mathrm{p2l}}$ is also not of full rank, the switching states $(l_{\mathrm{a}}+\gamma, l_{\mathrm{b}}+\gamma, l_{\mathrm{c}}+\gamma)$ ($\gamma \in \mathbb{R}$) in the new frame will also generate the same switching state when transformed back into the OCS. In other words, an offset γ can be added to the switching states $(l_{\mathrm{a}}, l_{\mathrm{b}}, l_{\mathrm{c}})$ in the new coordinate system to try to give them an integer form for simplicity. However, not all of them can be converted to integer form. Classify the switching vectors in the OCS into two categories: those that contain one switching state with zero CMV satisfying $S_{\mathrm{sum}} = 1.5(n-1)$, and those that do not. It can be shown that only the switching states in the new coordinate system resulting from the former have available values of γ to convert themselves to integer form, such as the switching states on the red hexagon in Fig. 4(b) (also bolded in Table II) with γ = 1/3 or 2/3. That is to say, only switching states that can be converted to integer form are desired.

These desired switching states can be extracted separately to obtain the final form of the new coordinate system, and each switching state can be added with different values of γ to fall into the range of $[0\ n-1]$. For instance, the switching state (-1/3, -1/3, 2/3) in Fig. 4(b) can be extracted and converted to (0, 0, 1), (1, 1, 2), (2, 2, 3) and (3, 3, 4) by adding 1/3, 4/3, 7/3 and 10/3, respectively. In this way, a simplified SVD in the proposed coordinate system (PCS) can be attained, as shown in Fig. 5. Comparing Fig. 5 with Fig. 2, it can be observed that Fig. 5 is identical to the SVD formed by the two innermost hexagons in the OCS, and the PCS looks like the cropped version of the OCS. However, the PCS is not simply cropped from the OCS. As described previously, its acquisition undergoes coordinate transformation, fraction elimination, and switching state extraction. Consequently, the PCS essentially implements a mapping between switching states with zero CMV. For example, the vector ***OP*** containing (1, 2, 3) with zero CMV in Fig. 2 is mapped to the vector consisting of (1, 0, 1), (2, 1, 2), (3, 2, 3) and (4, 3, 3) in Fig. 5. Each

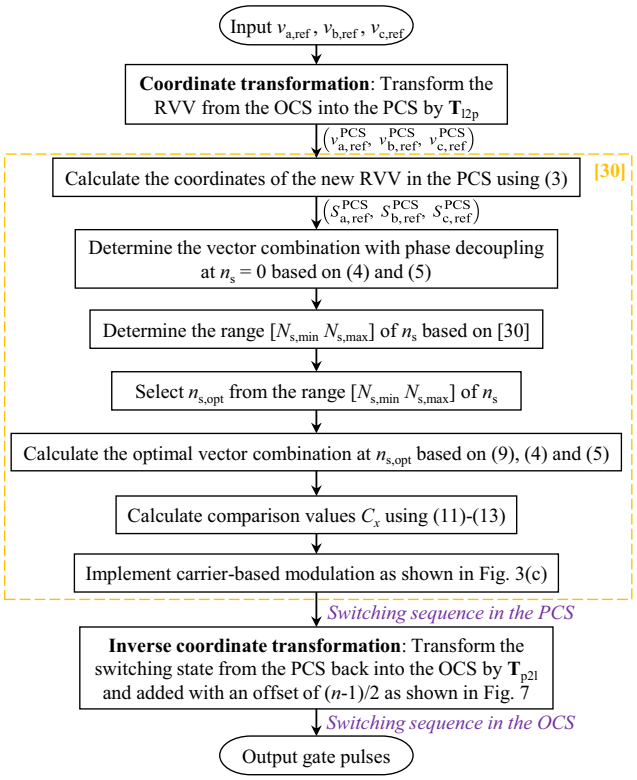

Fig. 6. Flow chart of the proposed complete CMV elimination strategy.

vector in the PCS thus corresponds to a vector containing the switching state with zero CMV in the OCS. More importantly, considering the similarity between the profiles of the PCS and the OCS, the transformed RVV in the PCS can clearly be synthesized using conventional NTVs-based methods, and the identified NTVs in the PCS can then be transformed back into the OCS to derive the final non-NTVs with zero CMV.

As a result, the flow chart of the proposed complete CMV elimination strategy is shown in Fig. 6, where the NTVs-based method presented in [30] is utilized to synthesize the new RVV in the PCS. Combined with Fig. 6, the RVV $\boldsymbol{V}_{\mathrm{ref}}{}'$ with ($v_{\mathrm{a,ref}}$, $v_{\mathrm{b,ref}}$, $v_{\mathrm{c,ref}}$) = (-0.8E, 1.3E, -0.5E) in Fig. 2 is taken as an example to further detail the proposed strategy, and the entire implementation is illustrated as follows:

1) Transform the RVV from the OCS into the PCS by $\mathbf{T}_{\mathrm{l2p}}$. The new RVV $\boldsymbol{O'S'}$ with ($v_{\mathrm{a,ref}}^{\mathrm{PCS}}$, $v_{\mathrm{b,ref}}^{\mathrm{PCS}}$, $v_{\mathrm{c,ref}}^{\mathrm{PCS}}$) = (-0.6$E$, -0.1$E$, 0.7$E$) can be derived, as shown in Fig. 5. As explained previously, the NTVs-based method (i.e., [30]) can then be employed in the PCS. Notice that $\boldsymbol{O'S'}$ is identical to $\boldsymbol{V}_{\mathrm{ref}}$ mentioned in Section II-B, so the previous calculation results can be used directly.
2) Calculate the vector combination at $n_{\mathrm{s}} = 0$ using (3)–(5) based on the new RVV in the PCS. According to Section II-B3, the coordinates of the offset and remainder vectors at $n_{\mathrm{s}} = 0$ are (1, 2, 3) and (0.4, -0.1, -0.3), respectively.
3) Determine the range of n_{s}. Since all redundant vector combinations have a one-to-one correspondence with the values of n_{s}, only the range of n_{s} needs to be determined, which can be derived as [-5 5] based on (21), (22) and (28) in [30].

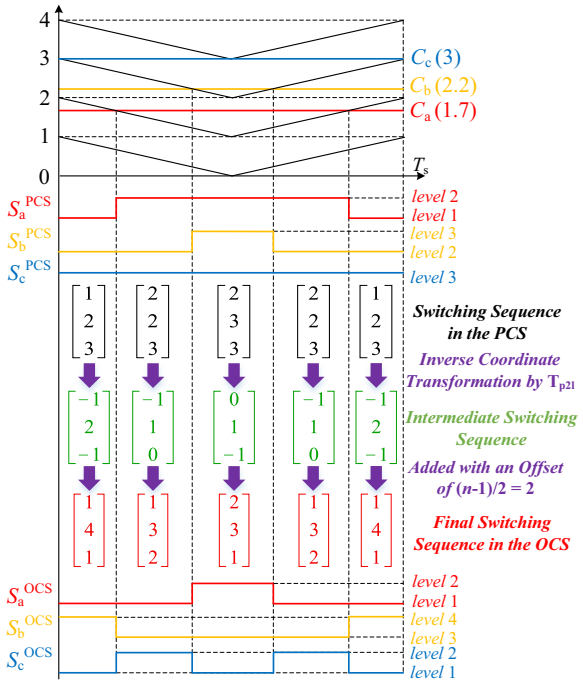

Fig. 7. Schematic of the final switching sequence generation in the OCS.

4) Determine $n_{s,opt}$ from the range of n_s and calculate the optimal vector combination by (9), (4) and (5). For simplicity, $n_{s,opt} = 0$ is chosen here. It can also be identified to reduce device switching frequency as described later.
5) Calculate the comparison values with the carriers using (11)–(13), and implement carrier-based modulation. According to Fig. 3(c), (C_a, C_b, C_c) = (1.7, 2.2, 3) for λ = 0 can be obtained, and these values are compared with the level-shifted carriers at each time step to produce the current switching state in the PCS.
6) Transform the switching state of each time step from the PCS back into the OCS by $\mathbf{T}_{p21}$, and added with an offset of $(n-1)/2$ = 2, as shown in Fig. 7. The final switching sequence are shown as (1, 4, 1)-(1, 3, 2)-(2, 3, 1)-(1, 3, 2)-(1, 4, 1), where all switching states are with zero CMV as each of them satisfies $S_{sum} = 1.5(n-1)$.

The discontinuous modulation (i.e., λ = 0) is used previously to reduce switching losses in each switching period. Due to the similarity between the profiles of the PCS and the OCS, other simplified NTVs-based methods such as carrier-based [8], [16], two-level SVPWM-based [22], [23], and non-orthogonal coordinate system-based solutions [26], [27] can also be utilized. The only modification required is to replace steps 2–5 (i.e., the orange dotted box in Fig. 6) with the target modulation algorithm. The proposed strategy explicitly provides three benefits: 1) complete CMV elimination is achieved through simple coordinate transformation; 2) it creates a convenient interface to the existing NTVs-based methods, thus providing high flexibility; 3) when combined with certain algorithms such as the proposed SFM solution, the converter's redundancy can be further exploited for better operational performance, as explained in Section III-C.

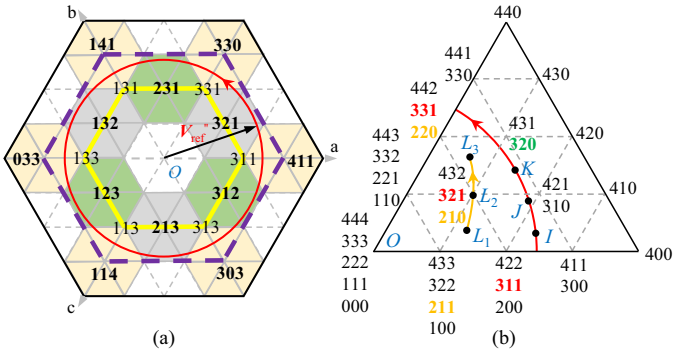

Fig. 8. RVV trajectory in (a) the five-level SVD and (b) the first sector.

B. SFM Solution

In this section, the device switching frequency is minimized for a given carrier frequency and λ. For consistency, the modulation scheme presented in [30] is chosen as the study case. First, a simplified analysis method is introduced considering that all switching states of the NTVs have a one-to-one correspondence with the values of n_s, that is, the switching state at a given n_s for a given RVV can be directly observed in a low-level SVD without complicated calculations. For instance, the switching state at $n_s = 1$ for $\boldsymbol{V}_{ref}$ can be immediately discovered as (1, 2, 2) from Fig. 2 because there is one and only one switching state in the NTVs obeying (10).

As explained previously, carrier-based implementation naturally achieves a minimal number of switching actions within each cycle for a given λ, but it may still be high between adjacent cycles. Consider $\boldsymbol{V}_{ref}''$ rotated counterclockwise in Fig. 8(a). In the case of no optimization, i.e., $n_{s,opt}$ = 0 [30], the sequence of offset vectors in a fundamental period can be directly observed as (4, 1, 1)-(3, 2, 1)-(3, 3, 0)-(2, 3, 1)-(1, 4, 1)-(1, 3, 2)-(0, 3, 3)-(1, 2, 3)-(1, 1, 4)-(2, 1, 3)-(3, 0, 3)-(3, 1, 2)-(4, 1, 1) based on (10). As described in Problem 2 in Section II-B, $\lambda < 1$ can first be considered for simplicity, and it can be shown that up to two switching actions between adjacent cycles can occur simultaneously in the scheme without optimization according to (15).

According to Fig. 8(a), if each offset vector is located on the inner hexagon closest to the RVV trajectory, as marked by the solid yellow line with the sequence as (3, 1, 1)-(3, 2, 1)-(3, 3, 1)-(2, 3, 1)-(1, 3, 1)-(1, 3, 2)-(1, 3, 3)-(1, 2, 3)-(1, 1, 3)-(2, 1, 3)-(3, 1, 3)-(3, 1, 2)-(3, 1, 1), the maximum number of switching actions between adjacent cycles can be reduced from 2 to 1, and the minimal device switching frequency can thus be achieved. Inspired by this, a solution based on the RP dwell mechanism is proposed as shown in Fig. 9, where the vector combination at $n_s = 0$ is calculated based on the optimal RP of the previous moment. That is to say, the initial RP will be updated at the end of each cycle, which can be expressed as (18) based on (8).

$$v_{min}(t+1) = v_{min}(t) + n_{s,opt}(t)E/3. \tag{18}$$

In this way, equation (10) is accordingly updated to

$$S_a(t) + S_b(t) + S_c(t) = N_{sum}(t) - n_s \tag{19}$$

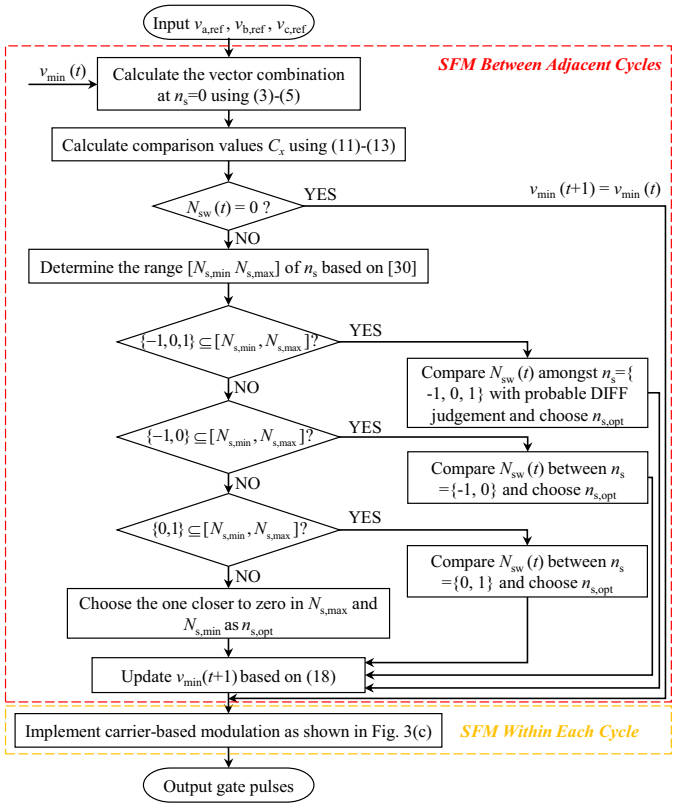

Fig. 9. Flow chart of the proposed SFM approach.

where the initial value of $N_{\rm sum}(t)$ is $N_{\rm sum}(0) = 1.5(n-1)$, and $N_{\rm sum}(t+1) = N_{\rm sum}(t) - n_{\rm s,opt}(t)$.

As shown in Fig. 8(b), the RVV located in the first sector is taken to detail the proposed method. Suppose that the RVV is positioned at ***OI*** and the offset vector is chosen as (3, 1, 1) with $n_{\rm s,opt}$ = 1 at t = 0, namely $N_{\rm sum}(1)$ = 5 and $v_{\rm min}(1)$ is updated accordingly by (18). According to Fig. 9, if the RVV is rotated to ***OJ*** at t = 1, the offset vector at $n_{\rm s} = 0$ is first calculated by (3)–(5) based on $v_{\rm min}(1)$. It can be intuitively observed as (3, 1, 1) as constrained by (19), which can be directly output since $N_{\rm sw}(1) = 0$. Similarly, if the RVV is transferred to ***OK*** at t = 2, the offset vector at $n_{\rm s} = 0$ can be first derived as (3, 2, 0). In this case, it is certain that one coordinate increases by 1 ($S_{\rm b}$: 1→2) while one coordinate decreases by 1 ($S_{\rm c}$: 1→0) to ensure that the offset vector still satisfies (19), which results in the vertices of the offset vectors at t = 1 and t = 2 are distributed in two adjacent triangles [see Fig. 8(b)]. According to Section II-B3 and (19), the coordinates at the common vertices of these two triangles can be deduced just by setting $n_{\rm s} = \{-1, 1\}$, e.g., the offset vector can be shifted from the vertex (3, 2, 0) to the common vertices (3, 2, 1) and (3, 1, 0) by configuring $n_{\rm s} = -1$ and $n_{\rm s} = 1$, respectively. Clearly, each of them differs from (3, 1, 1) by only 1. Thus, the number of switching actions can be reduced from 2 to 1 by selecting $n_{\rm s,opt} = 1$ or $n_{\rm s,opt} = -1$.

Although both (3, 2, 1) and (3, 1, 1) can achieve the minimum number of switching actions relative to (3, 1, 1), their contribution to the switching frequency in a fundamental period is different. As shown in Fig. 8(a), if the vector farther away from the origin O is picked at each cycle, the sequence of offset vectors can be labeled as the purple dashed line. Evidently, the increased number of offset vectors results in a higher total number of switching actions. Hence, the vector closer to the origin is the optimal. According to Table I, the switching states at $n_{\rm s} = 2$ and $n_{\rm s} = -1$ point to the same vector and the coordinates at $n_{\rm s} = 1$ and $n_{\rm s} = 2$ differ only by 1. On this basis, the difference between the squares of the distances of the two vectors from the origin is calculated in $\alpha\beta$ frame, and a judgment factor is accordingly introduced as

$$\mathrm{DIFF} = \begin{cases} S_{\rm a}^1 + S_{\rm a}^2 - S_{\rm b}^1 - S_{\rm c}^1, & \text{if } S_{\rm a}^1 \neq S_{\rm a}^2 \\ S_{\rm b}^1 + S_{\rm b}^2 - S_{\rm a}^1 - S_{\rm c}^1, & \text{if } S_{\rm b}^1 \neq S_{\rm b}^2 \\ S_{\rm c}^1 + S_{\rm c}^2 - S_{\rm a}^1 - S_{\rm b}^1, & \text{if } S_{\rm c}^1 \neq S_{\rm c}^2 \end{cases} \tag{20}$$

where S_x^1 and S_x^2 denote the coordinates of the offset vector at $n_{\rm s} = 1$ and $n_{\rm s} = 2$, respectively, and the positive DIFF means that the vector with $n_{\rm s} = -1$ (or 2) is closer to the origin, and vice versa. In this case, the switching state at $n_{\rm s} = 2$ can be observed as (2, 1, 0). As it is different from that [i.e., (3, 1, 0)] at $n_{\rm s} = 1$ in phase a, we can get DIFF $= 3+2-1-0 > 0$, so the vector with $n_{\rm s} = -1$ [i.e., (3, 2, 1)] is selected. Notice that the proposed scheme is independent of λ. In the case of λ = 1, all S_x in (20) should be replaced with int(C_x).

In the special case of $R_{\max} - R_{\min} = 1$, the tip of the RVV lies on one of the vertices of the SVD, and all u_x will belong to $\{0, 1\}$. For instance, if the RVV is moved from $\boldsymbol{OL}_1$ with the offset vector (2, 1, 1) at t = k to $\boldsymbol{OL}_2$ at t = k + 1, the offset vector at $n_{\rm s} = 0$ can be (2, 1, 1), (2, 2, 0) or (3, 1, 0), and respective remainder vector can be synthesized by (1, 1, 0), (1, 0, 1) or (0, 1, 1). According to (15), $N_{\rm sw}(k+1)$ is 2 regardless of the combinations of the offset and remainder vectors. By setting $n_{\rm s} = 1$, any combination amongst them will be transformed into (2, 1, 0) and (0, 0, 0). Again, the number of switching actions is reduced from 2 to 1, which further verifies the effectiveness of the proposed solution.

C. Hybrid Objective Optimization

As shown in Fig. 7, there are two switching actions between any two switching states in the final switching sequence for CMV elimination, and thus the number of switching actions within each switching period is determined for a given λ. However, choosing different $n_{\rm s}$ as the optimal in step 4 may result in a different number of switching actions between adjacent switching periods. For instance, the output sequence in step 6 will be changed to (2, 3, 1)-(1, 4, 1)-(1, 3, 2)-(1, 4, 1)-(2, 3, 1) if $n_{\rm s,opt}$ = 1. As can be seen, adjusting $n_{\rm s,opt}$ does not change the combination of switching states in the final output, meaning that CMV is still kept at zero, but only changes the order of the switching states.

Similarly, consider $\boldsymbol{V}_{\rm ref}{}''$ in the OCS rotated counterclockwise in Fig. 8(a), and its transformed counterpart $\boldsymbol{V}_{\rm ref}^{\rm PCS}$ in the PCS is shown in Fig. 5. According to Section III-B, if $n_{\rm s,opt} = 0$ is always selected in step 4 of Section III-A, the sequence of offset vectors in a fundamental period in the PCS can be directly observed as (3, 2, 1)-(2, 3, 1)-(1, 3, 2)-(1, 2, 3)-(2, 1, 3)-(3, 1, 2)-(3, 2, 1), and the maximum number of switching actions between adjacent switching periods is

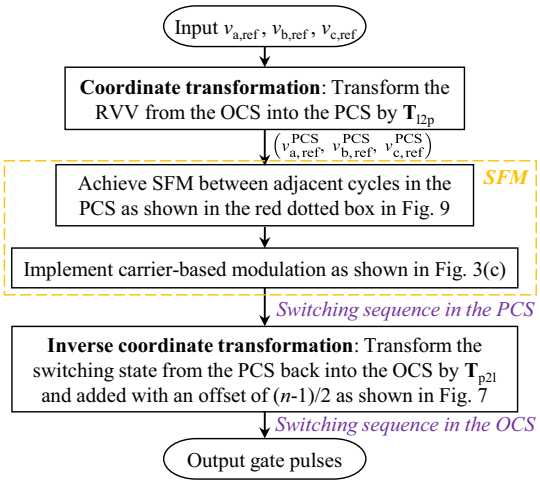

Fig. 10. Flow chart of the proposed hybrid objective optimization strategy.

2 in the PCS, which can be shown to increase to 4 when transformed back into the OCS by $\mathbf{T}_{p2l}$. To solve it, the SFM solution can be introduced. Specifically, steps 2-5 in Section III-A (i.e., the orange dotted box in Fig. 6) can be replaced with the proposed SFM solution, as shown in Fig. 10. In this way, the sequence of offset vectors in the PCS is adjusted to (3, 2, 2)-(3, 3, 2)-(2, 3, 2)-(2, 3, 3)-(2, 2, 3)-(3, 2, 3)-(3, 2, 2), and the maximum number of switching actions between adjacent periods is reduced to 1 in the PCS, which can be shown as 2 in the OCS through $\mathbf{T}_{p2l}$. Hence, the number of switching actions can still be halved by introducing SFM solution.

The proposed two optimization strategies can therefore either be applied separately or combined to minimize device switching frequency in the context of CMV elimination, which allows the converter's redundancy to be fully exploited.

IV. Performance Evaluation

Define the modulation index as $M = \sqrt{3}V_{\rm p}/V_{\rm dc}$, where $V_{\rm p}$ represents the amplitude of the phase voltage. In terms of SFM alone, it mainly provides a new approach to selecting the optimal $n_{\rm s}$ without changing the modulation region. Therefore, the maximum linear modulation index remains $M_{\rm max}$ = 1. For CMV elimination, since the introduced PCS ignores some undesired switching states, the RVV that lies in the linear modulation region in the OCS may exceed the maximum modulation region in the PCS. Thus, its linear modulation range needs to be re-evaluated.

As stated in Section III-A, each of the final switching states must fall within $[0\ n-1]$ after adding an offset of $(n-1)/2$. According to the inverse transformation matrix $\mathbf{T}_{p2l}$, any two coordinates of each switching state generated in the PCS should satisfy

$$|l_x - l_y| \le (n-1)/2 \tag{21}$$

where $x, y \in \{\rm a, b, c\}$ and $x \ne y$.

According to Fig. 3, the comparison values should obey

$$|C_x - C_y| \le (n-1)/2. \tag{22}$$

By substituting $S_{x,\rm ref} = S_x + R_x$, (3) and (13) into (22), the reference phase voltages in the PCS should comply with

$$\left|v^{\rm PCS}_{x,\rm ref} - v^{\rm PCS}_{y,\rm ref}\right| \le (n-1)E/2. \tag{23}$$

Define the three-phase reference voltages in the OCS as

$$\begin{cases} v_{\rm a,ref} = V_{\rm p}\sin\omega t \\ v_{\rm b,ref} = V_{\rm p}\sin(\omega t - 2\pi/3) \\ v_{\rm c,ref} = V_{\rm p}\sin(\omega t + 2\pi/3) \end{cases} \tag{24}$$

By transforming the reference phase voltages into PCS using $\mathbf{T}_{l2p}$ and then substituting it into (23), we get

$$V_{\rm p} \le (n-1)E/2. \tag{25}$$

As a result, the maximum linear modulation index can be derived as $M_{\rm max} = \sqrt{3}/2$.

V. Simulation and Experimental Results

This paper proposes complete CMV elimination, SFM and hybrid objective optimization methods as shown in Figs. 6, 9 and 10, which are denoted in simulations and experiments as Pro_CMV, Pro_SFM and Pro_HBD respectively for simplicity.

A. Simulation Verification

The Pro_SFM strategy is verified in this part by simulations. Since the tip of the RVV at a given modulation index sweeps more small triangle sectors within one fundamental period in the SVD with a higher number of levels, the Pro_SFM method would accordingly have greater potential to reduce the device switching frequency. Here, the model of a seven-level CHB converter is established in PLECS to highlight its optimization effect, where the parameters are from IKFW50N60DH3 produced by Infineon. The dc-link voltage of each H-bridge is set to E = 100 V, and the output voltage per phase is used to drive an inductive load of 20 Ω and 3 mH. In addition, the fundamental and carrier frequencies are configured as 50 Hz and 2 kHz, respectively.

1) Steady-state Performance: The Pro_SFM strategy is first tested under M = 0.5 and λ = 0. The output voltages and the number of switching actions between adjacent cycles in the scheme without SFM [30] and in the Pro_SFM strategy are presented in Fig. 11. Consistent with the theoretical analysis, the number of switching actions is reduced from 2 to 1 by introducing the Pro_SFM solution. The switching frequency of the leg voltage is then counted under different modulation indices, as shown in Table III, where the reduction ratio ξ of the switching frequency is defined as

$$\xi = ({\rm SF_{cmp}} - {\rm SF_{pro}})/{\rm SF_{cmp}} \tag{26}$$

where $\rm SF_{cmp}$ and $\rm SF_{pro}$ represent the switching frequencies of the comparison algorithms and the proposed algorithm to be verified, respectively. A similar definition applies to the loss reduction ratio in Table IV, except that the switching frequency in (26) is replaced by the switching losses.

Clearly, the Pro_SFM solution can effectively reduce the device switching frequency regardless of λ. Notice that there is no reduction in the switching frequency for M = 0.7 and

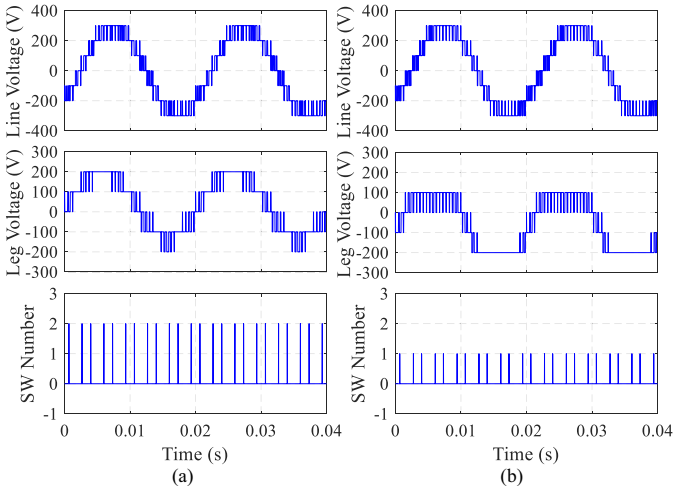

Fig. 11. Simulation results of line voltage v_{ab}, leg voltage v_{ag}, and the number of switching actions between adjacent cycles in the seven-level CHB converter under M = 0.5 and λ = 0. (a) Without SFM [30]. (b) Pro_SFM.

TABLE III
SWITCHING FREQUENCY (HZ) OF LEG VOLTAGE IN DIFFERENT METHODS WITH SAMPLING (CARRIER) FREQUENCY OF 2 KHZ

SVPWM Schemes	Modulation Index						
	0.2	0.3	0.4	0.5	0.6	0.7	0.8
Without SFM [30] (λ=0)	1433	1433	1533	1533	1533	1533	1583
Pro_SFM (λ=0)	1383	1383	1433	1433	1483	1533	1533
Reduction Ratio (%)	3.49	3.49	6.52	6.52	3.26	0	3.16
Without SFM [30] (λ=0.5)	2100	2100	2200	2200	2200	2200	2250
Pro_SFM (λ=0.5)	2050	2050	2100	2100	2150	2200	2200
Reduction Ratio (%)	2.38	2.38	4.55	4.55	2.27	0	2.22
Without SFM [30] (λ=1)	1433	1433	1483	1483	1583	1583	1633
Pro_SFM (λ=1)	1383	1383	1433	1433	1483	1533	1533
Reduction Ratio (%)	3.49	3.49	3.37	3.37	6.32	3.16	6.12

λ = 0 (or 0.5). From Fig. 2 in [21], the sequences of offset vectors in the first sector in the scheme without SFM [30] and in the Pro_SFM strategy can be obtained as (5, 2, 2)-(5, 1, 3)-(4, 1, 4) and (5, 2, 2)-(5, 1, 2)-(5, 1, 3)-(5, 1, 4)-(4, 1, 4), respectively. According to (15), the total number of switching actions in a fundamental period is equal, whereas the Pro_SFM solution can still reduce the number of switching actions between adjacent cycles by spreading the level changes over more cycles.

Fig. 12(a) compares the switching losses of the entire converter in phase-disposition PWM (PDPWM) [8], the scheme without SFM [30] and the Pro_SFM strategy under λ = 0.5. In contrast, the Pro_SFM approach evidently achieves minimal switching losses under different modulation indices; the switching losses can be lowered by up to 7.78% and 7.99% relative to PDPWM at M = 0.6 and that without SFM at M = 0.4, respectively. Furthermore, considering that switching losses are simultaneously affected by phase current or power factor (PF), Fig. 12(b) shows the switching losses under different PFs with the modulation index M = 0.5, where the total impedance of the circuit remains constant to achieve the same apparent power. As shown in Fig. 12(b), although the

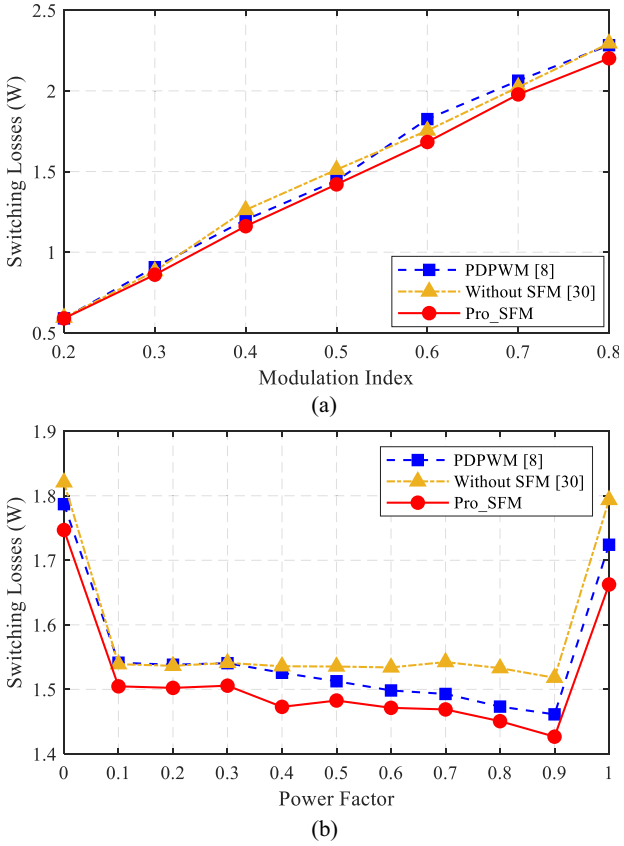

Fig. 12. Simulation results of switching losses in different methods. (a) Switching losses versus modulation index with PF = 0.999 (20 Ω & 3 mH). (b) Switching losses versus PF with M = 0.5.

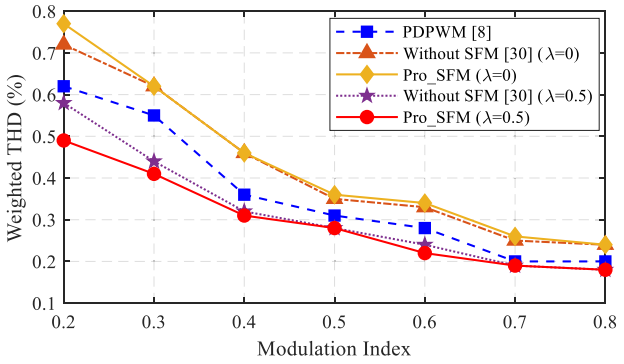

Fig. 13. Weighted THD of the line voltage in the seven-level CHB converter with different modulation methods.

PF also affects the switching losses, the Pro_SFM solution can lower the switching losses to different degrees under different PFs by reducing the device switching frequency. Fig. 13 shows the weighted THD [22] of the line voltage in different methods. As can be seen, the Pro_SFM solution can maintain comparable waveform quality in both continuous and discontinuous modulations. Besides, the removal of unwanted switching actions at λ = 0.5 slightly reduces the harmonic content and thus improves the output waveform.

2) Dynamic Performance: A transient profile is designed to verify the Pro_SFM solution over a wide operating point range, in which the modulation index increases linearly from

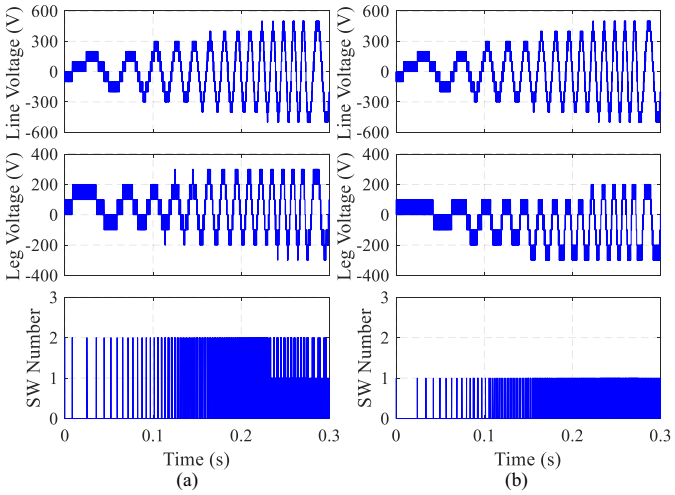

Fig. 14. Simulation results of line voltage v_{ab}, leg voltage v_{ag}, and the number of switching actions between adjacent cycles in the seven-level CHB converter under transient conditions. (a) Without SFM [30]. (b) Pro_SFM.

TABLE IV
AVERAGED SWITCHING LOSSES AND LOSS REDUCTION RATIO UNDER TRANSIENT CONDITIONS

Load	Averaged Switching Losses (W)			Loss Reduction Ratio (%)	
	PDPWM [8]	Without SFM [30]	Pro_SFM	Pro_SFM to [8]	Pro_SFM to [30]
20 Ω[a] 3 mH	1.5166	1.5182	1.4505	4.36	4.46
15 Ω[b] 42 mH	1.4593	1.4606	1.4216	2.58	2.67
10 Ω[c] 55 mH	1.5020	1.5024	1.4732	1.92	1.94

[a] PF = 0.999 at 50 Hz.
[b] PF = 0.75 at 50 Hz.
[c] PF = 0.5 at 50 Hz.

0.2 to 0.8 in 0.25 s, while the fundamental frequency rises linearly from 10 Hz to 50 Hz at the same time. The results when λ = 0.5 are shown in Fig. 14. Obviously, the number of switching actions can still be restricted to be only 1 at maximum throughout the transient process. Moreover, the reduced device switching frequency accordingly contributes to lower switching losses, as shown in Table IV, where different loads are tested for comprehensive comparison. Table IV further verifies the effectiveness of the Pro_SFM solution.

3) Hybrid Objective Optimization: The switching frequencies of the leg voltage in the Pro_CMV and Pro_HBD strategies are compared in Table V. As expected, the Pro_HBD strategy ensures lower device switching frequency and achieves a maximum switching frequency drop ratio of 9.78%. For M = 0.2 and M = 0.6, the switching frequencies remain the same. The former is because the origin (3, 3, 3) is always selected as the offset vector in the PCS, resulting in no switching action between adjacent cycles, while the reason for the latter is similar to that of M = 0.7 in Table III, that is, the Pro_HBD strategy can reduce the number of switching actions between adjacent cycles by spreading the level changes over more cycles although the total switching changes in a fundamental period are equal.

TABLE V
SWITCHING FREQUENCY (HZ) OF LEG VOLTAGE IN CMV SUPPRESSION METHODS WITH SAMPLING (CARRIER) FREQUENCY OF 2 KHZ

SVPWM Schemes	Modulation Index						
	0.2	0.3	0.4	0.5	0.6	0.7	0.8
In [4]	2000	2400	2200	2200	2200	2400	2400
In [26]	2050	2150	2150	2150	2250	2250	2250
In [31]	1433	1433	1483	1483	1583	1583	1633
In [33]	2666	3066	2866	2866	2866	3066	3066
In [35]	2666	2866	2766	2766	3066	2866	2866
Pro_CMV_CB	4100	4100	4100	4100	4200	4300	4300
Pro_CMV	2666	3066	2866	2866	2866	3066	3066
Pro_HBD	2666	2766	2766	2766	2866	2866	2866
Reduction Ratio (%)	0	9.78	3.49	3.49	0	6.52	6.52

B. Experimental Validation

The experimental platform of a five-level CHB converter is then built to validate the Pro_CMV strategy, as shown in Fig. 15. The system parameters are configured the same as in the simulation, except that the dc-link voltage of each H-bridge is adjusted to E = 30 V and the dead time is set to 2 μs. Considering that the Pro_CMV strategy should keep the CMV at zero regardless of the PF, the load of 20 Ω and 3 mH is used throughout the experiments. All modulation algorithms used in the experiments are implemented by the dSPACE SCALEXIO device, which contains an Intel Xeon processor E3-1275V6 with Linux-based real-time operating system and a Xilinx FPGA Kintex-7-160T, and their task assignments are presented in Fig. 15.

1) Steady-state Performance: Fig. 16 shows the experimental waveforms of the line voltage v_{ab}, leg voltage v_{ag}, phase current i_{a}, and CMV v_{ng} with the modulation index stepping from 0.4 to 0.8. As can be seen, the CMV can be controlled to be zero most of the time except for a few non-zero values caused by the dead time. Besides, the non-zero CMV waveform exhibit a sinusoidal characteristic whose fundamental frequency is three times that of the phase current. To explain it, the first H-bridge module of phase *a* in Fig. 1 is considered. Supposing that the IGBT of S_{a11} is close and those of both S_{a12} and $\bar{S}_{\mathrm{a12}}$ are open during the dead time, the output voltage of the H-bridge will be determined by the direction of the phase current: if the current flows from the converter to the load, the diode of $\bar{S}_{\mathrm{a12}}$ is on and the output voltage is 0; otherwise, the diode of S_{a12} is on and the output voltage is E. In this way, the CMV caused by the dead time for a given switching state is dominated by the direction combination of the three-phase currents, which ultimately leads to the preceding third-order harmonic characteristic.

2) Dynamic Performance: The transient profile designed in the simulation is exploited to further validate the Pro_CMV strategy, and the modulation schemes with time-averaged CMV elimination [26] and with minimal CMV magnitude [31] are also tested for comparison. The experimental waveforms

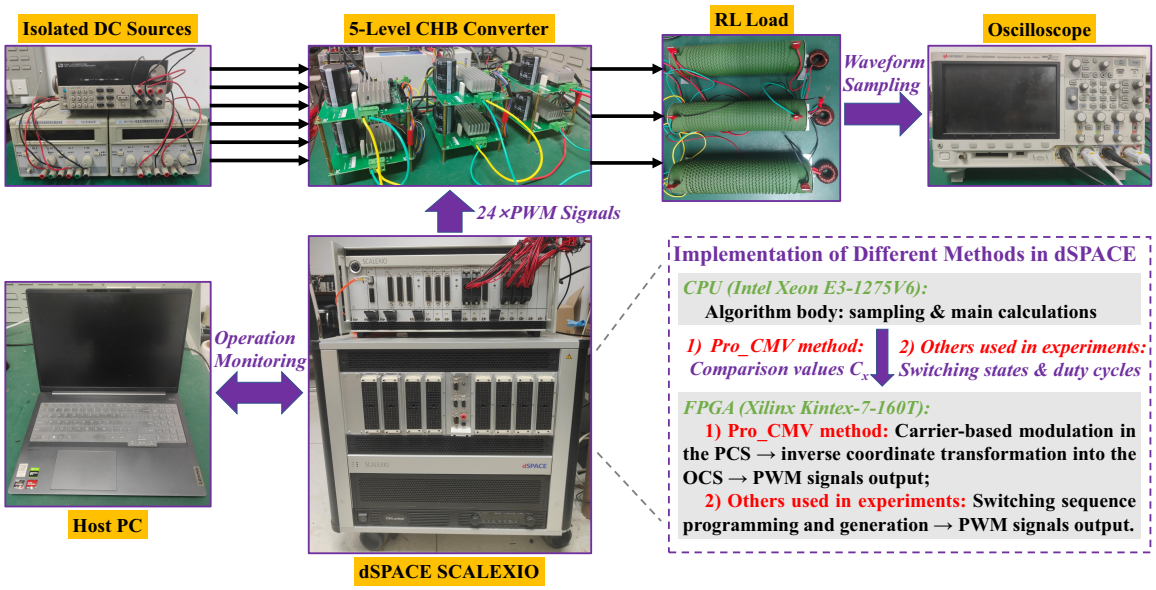

Fig. 15. Experimental platform of the five-level CHB converter system.

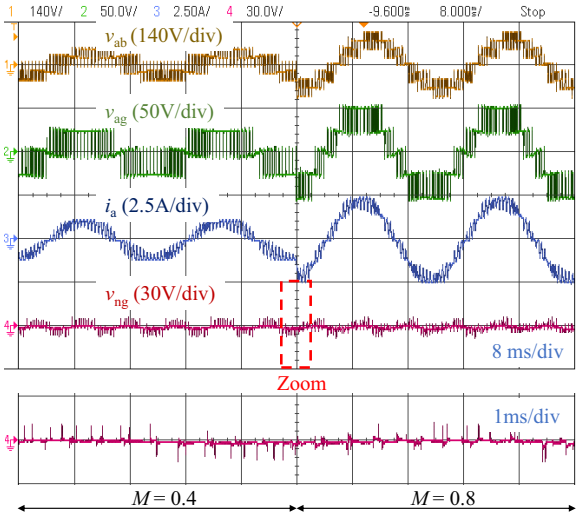

Fig. 16. Experimental results of the line voltage v_{ab}, leg voltage v_{ag}, phase current i_a, and CMV v_{ng} in the five-level CHB converter with the Pro_CMV strategy.

are shown in Fig. 17. Clearly, the latter two schemes can suppress the CMV peak to $2E/3$ (i.e., 20 V) and $E/3$ (i.e., 10 V), respectively, which are consistent with those in [26] and [31]. Again, the Pro_CMV scheme enables the CMV to remain essentially zero throughout the transient process.

Referring to [26], the common-mode current i_{ng} is subsequently measured by connecting an additional inductive load of 3 mH between points N and G. The current waveforms under the same transient profile are shown in Fig. 18. Obviously, the switching states with non-zero CMV in the schemes with time-averaged CMV elimination [26] and with minimal CMV magnitude [31] cause much higher common-mode current. Theoretically, the common-mode current of the Pro_CMV strategy shown in Fig. 18(c) should be kept at zero. As explained previously, the CMV during the dead time is governed by the direction combination of the three-phase currents independent of the operating conditions, such that the CMV waveform caused by dead time in Fig. 17(c) also exhibits a third-order harmonic characteristic, which accordingly results in a third-order common-mode current waveform in Fig. 18(c). Notice that this phenomenon can be further suppressed by decreasing the dead time or shifting the dead time to synchronize the switching actions of all phases [34].

C. Algorithm Comparison

1) Algorithm Flexibility: Several typical CMV suppression [26], [31] or elimination [4], [33], [35] methods are selected for comparison. As explained in Section III-A, the Pro_CMV algorithm can interface with most of the existing NTVs-based methods to provide high flexibility. In this paper, it is combined with the modulation scheme presented in [30], which not only avoids complicated calculation of duty cycles (as in [26]), complex sequence programming (as in [4], [35]), extensive floating-point operations (as in [31]), and lookup tables (as in [33]) to achieve low computational and storage complexity (see Section V-C4), but also offers the potential to further reduce device switching frequency (by introducing the Pro_SFM solution to form the Pro_HBD strategy, as explained in Section III-C). Similarly, carrier-based methods such as PDPWM [8] can be employed to deeply simplify implementation. For consistency, the strategy shown in Fig. 6 is still denoted as Pro_CMV, while that combined with PDPWM [8] is marked as Pro_CMV_CB, as shown in Tables V and VI and Fig. 20. For another example, the SVPWM algorithm presented in [22] can be used to fast calculate switching states and duty cycles. Therefore, the converter's performance can be fully optimized.

2) Waveform Quality: Compared with the NTVs-based methods in [26], [31], the Pro_CMV approach inevitably results in worse waveform quality since the non-NTVs are selected as output. Fig. 19 exemplarily compares the FFT

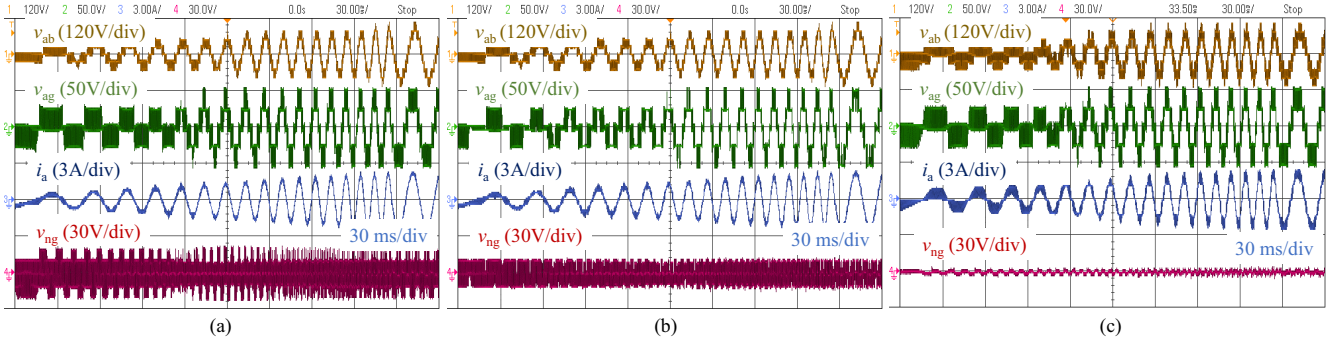

Fig. 17. Experimental results of the line voltage v_{ab}, leg voltage v_{ag}, phase current i_a, and CMV v_{ng} in the five-level CHB converter under transient conditions. (a) Time-averaged CMV elimination [26]. (b) Minimal CMV magnitude [31]. (c) Pro_CMV.

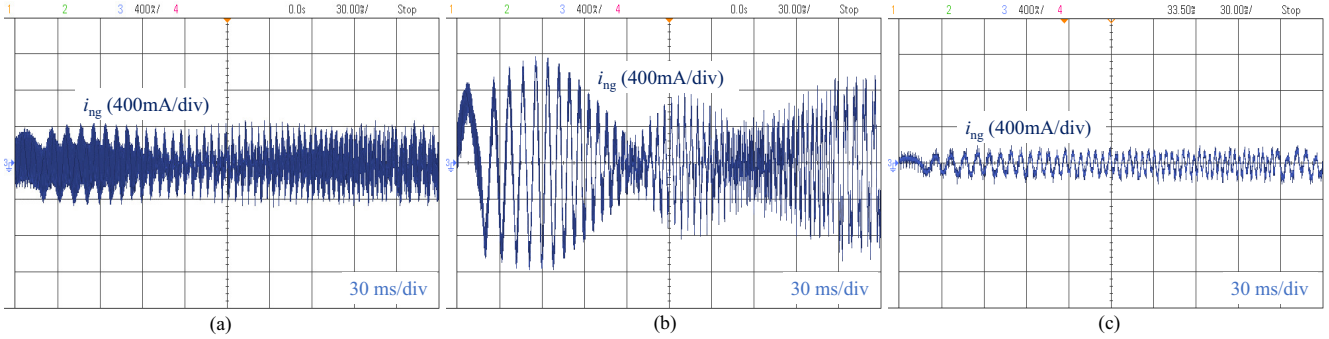

Fig. 18. Experimental results of the common-mode current i_{ng} in the five-level CHB converter with an additional inductive load under transient conditions. (a) Time-averaged CMV elimination [26]. (b) Minimal CMV magnitude [31]. (c) Pro_CMV.

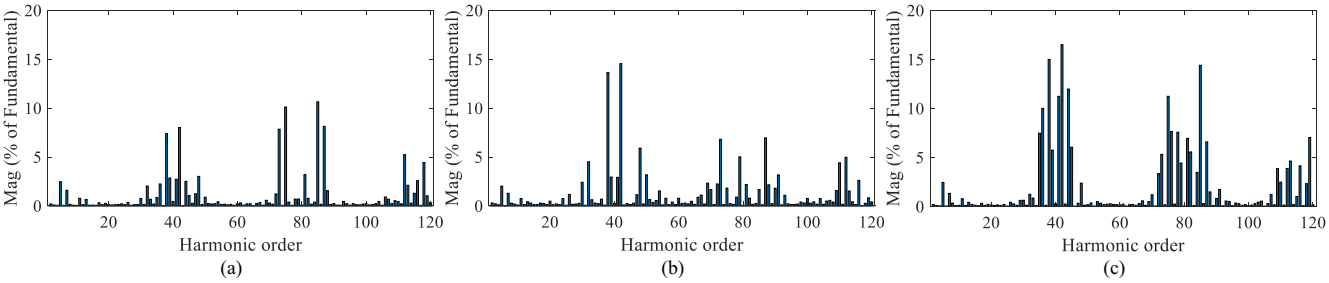

Fig. 19. FFT results of the line voltage in the five-level CHB converter under M = 0.5. (a) Time-averaged CMV elimination [26]. (b) Minimal CMV magnitude [31]. (c) Pro_CMV.

results of the line voltage under M = 0.5. The line voltage in the Pro_CMV approach exhibits a larger number of harmonics around integer multiples of the carrier frequency (e.g., 40th- and 80th-order), which in turn leads to higher weighted THD of the line voltage, as shown in Fig. 20. Compared with other complete CMV elimination algorithms, both the Pro_CMV and Pro_HBD strategies produce a waveform quality comparable to those in [33], [35]. This is because they all employ a five-segment switching sequence consisting of the non-NTVs with zero CMV. Besides, the Pro_CMV_CB strategy using a seven-segment sequence contributes to lower weighted THD of the line voltage. It should be noted that the Pro_CMV strategy can also be switched to seven-segment pattern to improve the waveform quality such as setting $\lambda = 0.5$ in (12). Since a four-segment sequence is applied in [4], higher weighted THD of the line voltage is caused.

3) Switching Frequency: As shown in Table V, the increased number of switching actions within each switching period results in that both Pro_CMV and Pro_HBD strategies yield higher device switching frequency than the NTVs-based methods in [26], [31]. However, compared with the algorithms [33], [35] with the same switching pattern, the Pro_CMV approach can be combined with the Pro_SFM solution to form the Pro_HBD strategy to achieve lower device switching frequency. Although the Pro_CMV_CB strategy achieves higher-quality waveforms, the use of a seven-segment sequence inevitably leads to higher switching frequency. Thus, the switching pattern can be flexibly selected to achieve a compromise between waveform quality and switching frequency according to actual needs, which further verifies high algorithm flexibility. Along with worse waveform quality, the four-segment sequence used in [4] accordingly produces lower device switching frequency. Furthermore, reduced switching

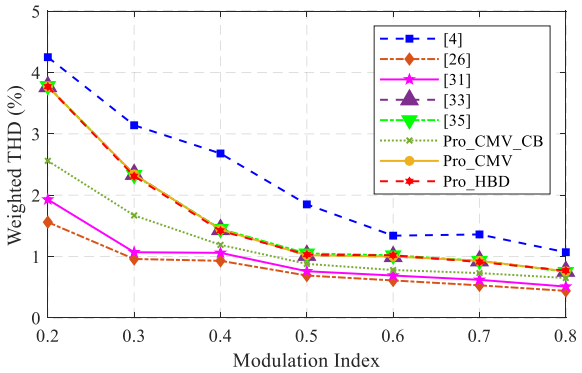

Fig. 20. Weighted THD of the line voltage in the five-level CHB converter with different modulation algorithms.

losses are achieved in [35] under the premise of CMV elimination, similar to the optimization objective of the Pro_HBD method. However, its lower switching losses come at the expense of introducing current feedback, increasing system cost. The Pro_HBD algorithm avoids extra current sensors and therefore has a wider range of applications, such as both open-loop and closed-loop control in motor drives. Moreover, since the number of switching actions between adjacent cycles is not considered in [35], a higher switching frequency is induced, as shown in Table V. Higher switching frequency increases the incidents of high dv/dt that is related to the rise time of the voltage, which leads to higher insulation failure rates [34].

4) Execution Time and Memory Footprint: Table VI shows the execution time and memory footprint of different methods, where each method from reference voltages sampling to gate pulses output for the five-level converter is written in C and implemented on the same processor DSP TMS320F28335, and both execution time and memory utilization are directly observed in the Code Composer Studio software. Compared with the method without SFM [30], the Pro_SFM solution requires a relatively small increase in execution time and memory footprint. This is because the Pro_SFM solution only introduces simple logical judgment and arithmetic calculation on the basis of [30]. Besides, the execution time and space occupation of the Pro_CMV and Pro_HBD strategies are slightly increased compared to those of [30] and the Pro_SFM solution, respectively, because the Pro_CMV strategy only adds simple coordinate transformation and inverse transformation to the original methods. As explained previously, the NTVs-based methods in [26], [31] either require complicated calculation of duty cycles [26], or require extensive floating-point operations [31], leading to high time and space complexity. Compared with other complete CMV elimination algorithms [4], [33], [35], the Pro_CMV strategy can not only be combined with the carrier-based method [8] (i.e., Pro_CMV_CB) to achieve very low execution time and memory footprint, but can also be interfaced with the Pro_SFM solution to achieve the Pro_HBD strategy to reduce device switching frequency while ensuring low time and space complexity.

The implementation complexity of several proposed strategies with increased number of levels is also analyzed and tested. As shown in Figs. 6, 9 and 10, none of the proposed

TABLE VI
COMPARISON OF EXECUTION TIME AND MEMORY FOOTPRINT IN DIFFERENT METHODS FOR THE FIVE-LEVEL TOPOLOGY

SVPWM Schemes	Time (μs)	Memory (Bytes)	SVPWM Schemes	Time (μs)	Memory (Bytes)
In [4]	18.32	3386	In [30]	12.77	3863
In [26]	56.39	6472	Pro_CMV_CB	5.22	3041
In [31]	43.61	6375	Pro_CMV	13.55	3958
In [33]	21.51	6089	Pro_SFM	15.43	4241
In [35]	19.47	4619	Pro_HBD	16.31	4353

TABLE VII
EXECUTION TIME AND MEMORY FOOTPRINT OF THE PROPOSED STRATEGIES FOR THE SEVEN- AND NINE-LEVEL TOPOLOGIES

SVPWM Schemes	Seven-level		Nine-level	
	Time (μs)	Memory (Bytes)	Time (μs)	Memory (Bytes)
Pro_CMV_CB	7.03	3227	8.82	3413
Pro_CMV	15.33	4170	16.93	4382
Pro_SFM	17.04	4445	18.88	4649
Pro_HBD	17.88	4569	19.67	4785

strategies is limited by the number of levels; they all consider the number of levels as a variable in the implementation, and thus the number of levels only affects the relevant calculation results but not the algorithm implementation. Besides, all the proposed strategies only require simple logical judgment and arithmetic calculation without lookup tables and iterative operations, which means that the computational and storage complexity of the main parts of these strategies is basically independent of the number of levels. However, the increased number of switching devices as the number of levels rises requires more gate signals, resulting in an increased number of level-shifted carriers in carrier-based implementation (see Figs. 6, 9 and 10) and higher hardware resource occupation requirements. From the above analysis, it can be readily shown that the computational and storage complexity of all the proposed strategies slightly increases as the number of levels rises. For verification, Table VII shows the execution time and memory requirements of several proposed strategies for seven- and nine-level converters.

Based on the above comparisons, it can be concluded that the proposed strategies are strong complements to existing modulation algorithms: compared with other complete CMV elimination algorithms [4], [33], [35], the Pro_CMV scheme can achieve comparable waveform quality, reduced switching frequency (by forming the Pro_HBD strategy), high flexibility, and low time and space complexity, so it would be preferred in situations sensitive to CMV, such as in machine drives; in the case of higher demands on waveform quality, the scheme with time-averaged CMV elimination [26] or that with minimal CMV magnitude [31] may be a compromise, except that CMV can only be suppressed to some extent; in the case of higher constraints on device switching frequency and electromagnetic interference, such as in medium-voltage and high-power grid

systems, the Pro_SFM method may be a best choice.

VI. Conclusion

This paper proposes novel SVPWM strategies to achieve complete CMV elimination and SFM. First, a new coordinate system is introduced to ensure that the final output switching states are all with zero CMV, which allows existing NTVs-based methods to be utilized to identify the desired non-NTVs, thus offering high flexibility. Then, graphical analysis is presented to establish the relationship between the number of switching actions and the number of level shifts, by which SFM can be readily achieved through simple logical judgment and arithmetic calculation. Furthermore, these two optimization objectives are combined to achieve SFM under the premise of CMV elimination, which allows the converter's redundancy to be fully utilized. Finally, simulation and experimental results as well as comparisons with existing methods validate the merits of the proposed strategies.

References

[1] X. Wu, C. Xiong, S. Yang, H. Yang, and X. Feng, "A simplified space vector pulsewidth modulation scheme for three-phase cascaded H-bridge inverters," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4192–4204, Apr. 2020.

[2] P. Chamarthi, P. Chhetri, and V. Agarwal, "Simplified implementation scheme for space vector pulse width modulation of n-level inverter with online computation of optimal switching pulse durations," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6695–6704, Nov. 2016.

[3] K. J. Pratheesh, G. Jagadanand, and R. Ramchand, "A generalized-switch-matrix-based space vector modulation technique using the nearest level modulation concept for neutral-point-clamped multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4542–4552, Jun. 2018.

[4] C. Wang, Q.-C. Zhong, N. Zhu, S.-Z. Chen, and X. Yang, "Space vector modulation in the 45° coordinates $\alpha'\beta'$ for multilevel converters," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6525–6536, Jun. 2021.

[5] A. S. Hussein and A. M. Y. M. Ghias, "Cascaded multioutput multilevel converter: Modulation and operating limits," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 399–408, Jan. 2022.

[6] S. Choi and M. Saeedifard, "Capacitor voltage balancing of flying capacitor multilevel converters by space vector PWM," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1154–1161, Jul. 2012.

[7] S. H. Montazeri, J. Milimonfared, and M. Zolghadri, "A new modeling and control scheme for cascaded split-source converter cells," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 7618–7628, Aug. 2022.

[8] O. Oghorada, Z. Li, B. Esan, and E. Dickson, "Carrier-based sinusoidal pulse-width modulation techniques for flying capacitor modular multilevel cascaded converter," *Heliyon*, vol. 5, no. 12, p. e03022, 2019.

[9] J.-M. De Paris, C. R. D. Osório, H. Pinheiro, and F. d. M. Carnielutti, "Phase disposition modulation with sorting algorithm for symmetrical cascaded multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7527–7536, Nov. 2019.

[10] J. Ebrahimi, H. Karshenas, S. Eren, and A. Bakhshai, "A fast-decoupled space vector modulation scheme for flying capacitor-based multilevel converters," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 14 539–14 549, Dec. 2021.

[11] D. A. Schuetz, F. B. Grigoletto, F. Carnielutti, and H. Pinheiro, "Discontinuous space vector modulation for three-phase five-levels packed-U-cell converter," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 14 353–14 365, Dec. 2021.

[12] X. Xing, X. Li, F. Gao, C. Qin, and C. Zhang, "Improved space vector modulation technique for neutral-point voltage oscillation and common-mode voltage reduction in three-level inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8697–8714, Sep. 2019.

[13] M. Hassanifar, D. Nazarpour, S. Golshannavaz, and Y. Neyshabouri, "A modular cascaded multilevel converter with high configurability: Design, analysis, and optimization study," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 1, pp. 850–861, Feb. 2021.

[14] J. B. Soomro, F. Akhter, S. Ali, S. S. H. Bukhari, I. Sami, and J.-S. Ro, "Modified nearest level modulation for full-bridge based HVDC MMC in real-time hardware-in-loop setup," *IEEE Access*, vol. 9, pp. 114 998–115 005, 2021.

[15] Q. Yan, Z. Zhou, M. Wu, X. Yuan, R. Zhao, and H. Xu, "A simplified analytical algorithm in abc coordinate for the three-level SVPWM," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3622–3627, Apr. 2021.

[16] B. McGrath, D. Holmes, and T. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293–1301, Nov. 2003.

[17] D. Ronanki and S. S. Williamson, "Discontinuous space vector modulation schemes for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3987–3994, Apr. 2021.

[18] A. Gupta and A. Khambadkone, "A space vector PWM scheme for multilevel inverters based on two-level space vector PWM," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1631–1639, Oct. 2006.

[19] Y. Deng, K. H. Teo, C. Duan, T. G. Habetler, and R. G. Harley, "A fast and generalized space vector modulation scheme for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5204–5217, Oct. 2014.

[20] I. Ahmed, V. B. Borghate, A. Matsa, P. M. Meshram, H. M. Suryawanshi, and M. A. Chaudhari, "Simplified space vector modulation techniques for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8483–8499, Dec. 2016.

[21] X. Li, S. Dusmez, B. Akin, and K. Rajashekara, "A new active fault-tolerant SVPWM strategy for single-phase faults in three-phase multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3955–3965, Jun. 2015.

[22] J.-S. Hu, J.-N. Lin, and H.-C. Chen, "A discontinuous space vector PWM algorithm in abc reference frame for multilevel three-phase cascaded H-bridge voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8406–8414, Nov. 2017.

[23] Y. Deng, Y. Wang, K. H. Teo, and R. G. Harley, "A simplified space vector modulation scheme for multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1873–1886, Mar. 2016.

[24] S. Wei, B. Wu, F. Li, and C. Liu, "A general space vector PWM control algorithm for multilevel inverters," in *18th Annu. IEEE APEC*, vol. 1, Feb. 2003, pp. 562–568.

[25] J. Li, J. Jiang, and S. Qiao, "A space vector pulse width modulation for five-level nested neutral point piloted converter," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 5991–6004, Aug. 2017.

[26] A. Ovalle, M. E. Hernandez, and G. A. Ramos, "A flexible nonorthogonal-reference-frame-based SVPWM framework for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4925–4938, Jun. 2017.

[27] X. Yuan, Y. Gao, and Y. Li, "A fast multilevel SVPWM method based on the imaginary coordinate with direct control of redundant vectors or zero sequence components," *IEEE Open J. Ind. Electron. Soc.*, vol. 1, pp. 355–366, 2020.

[28] Z. Liu, Y. Wang, G. Tan, H. Li, and Y. Zhang, "A novel SVPWM algorithm for five-level active neutral-point-clamped converter," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3859–3866, May 2016.

[29] H. Lin, Z. Shu, J. Yao, H. Yan, L. Zhu, D. Luo, and X. He, "A simplified 3-D NLM-based SVPWM technique with voltage-balancing capability for 3LNPC cascaded multilevel converter," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3506–3518, Apr. 2020.

[30] Q. Sun, Z. Wang, S. M. Sharkh, and W. Hao, "A flexible and decoupled space vector modulation scheme with carrier-based implementation for multilevel converters," *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 8135–8149, Jul. 2023.

[31] H. Yao, Y. Yan, T. Shi, G. Zhang, Z. Wang, and C. Xia, "A novel SVPWM scheme for field-oriented vector-controlled PMSM drive system fed by cascaded H-bridge inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8988–9000, Aug. 2021.

[32] C. Wei, X. Yuan, Y. Zhang, and X. Wu, "A generic multi-level SVM scheme based on two-level SVM for n-level converters," *Energies*, vol. 13, no. 9, p. 2143, 2020.

[33] Q. A. Le and D.-C. Lee, "Elimination of common-mode voltages based on modified SVPWM in five-level ANPC inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 173–183, Jan. 2019.

[34] M. M. Renge and H. M. Suryawanshi, "Five-level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1598–1607, Jul. 2008.

[35] N.-V. Nguyen, T.-K. Tu Nguyen, and H.-H. Lee, "A reduced switching loss PWM strategy to eliminate common-mode voltage in multilevel inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5425–5438, Oct. 2015.

Qingle Sun (Student Member, IEEE) received the B.Eng. degree in vehicle engineering from Taiyuan University of Technology, Taiyuan, China, in 2018. He is currently working toward the Ph.D. degree with the National Engineering Research Center of Electric Vehicles, Beijing Institute of Technology, Beijing, China.

Since November 2023, he has been a visiting Ph.D. student with the University of Western Australia, Perth, Australia. His research interests include machine drives and multilevel inverters.

Suleiman M. Sharkh (Senior Member, IEEE) received the B.Eng. and Ph.D. degrees in electrical engineering from the University of Southampton, Southampton, U.K., in 1990 and 1994, respectively.

He is currently a Professor of Electrical Machines and Drives with the University of Southampton. He is also the Managing Director of HiT Systems Ltd. His main research interests include control, electrical machine, and power electronics with applications to electric vehicles, marine propulsion, exhaust energy recovery, and submersible pumps.

Dr. Sharkh was a recipient of the 2008 Engineer Energy Innovation Award for his work on rim-driven thrusters and marine turbine generators. He is a member of the Institution of Engineering and Technology and a Chartered Engineer.

Zhifu Wang received the B.S. and Ph.D degrees in vehicle engineering from Beijing Institute of Technology, Beijing, China, in 2000 and 2013, respectively.

He is currently a Professor with Beijing Institute of Technology, Beijing, China, where he is also the Director of the National Engineering Research Center of Electric Vehicles. His research interests include vehicle dynamics, machine drives, multilevel converters, and electric machine emulators.

Zeshang Wang (Student Member, IEEE) received the B.S. degree in vehicle engineering from the Harbin Institute of Technology Weihai, Shandong, China, in 2021. He is currently working toward the M.S. degree with the National Engineering Research Center of Electric Vehicles, Beijing Institute of Technology, Beijing, China.

His research interests include electric machine emulators, machine drives, and power converters.

Guobiao Shi received the B.S. and M.S. degrees from Jilin University of Technology, China, in 1995 and 1998, respectively, and the Ph.D. degree in vehicle engineering from Jilin University, China, in 2002.

He is currently an Associate Professor with Beijing Institute of Technology, Beijing, China. His research interests include electric power steering and electric hydraulic power steering, active front steering, steering by wire, etc.