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Vertical Integration of KTN on SOI Wafer

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Abstract:

Optical modulators play an important role in communication systems, and silicon has been a focal point in this field thanks to its compatibility with CMOS fabrication. However, silicon's lack of inherent electro-optic behavior makes it suboptimal for modulation purposes. Conversely, potassium tantalate niobate (KTN) materials boast an improved electro-optic coefficient, presenting a path for improving modulation efficiency. However, limited research exists on KTN materials due to the difficulties associated with their fabrication.

Here, a fabrication methodology is described for wafer-scale vertical integration of KTN material onto silicon-on-insulator (SOI) wafers. The resulting devices exhibit a propagation loss of 3.3dB mm^{-1} and a transition loss within the range of 0.46 to 0.76dB, which are in agreement with simulations. This method tackles the fabrication challenges and showcases the potential of utilising KTN as the integration material on silicon platform for future optical modulators.

1. Introduction

Optical modulators play an essential role in telecommunications due to the increasing usage of photonic devices in the industry, particularly in fiber-optics and data centre communications. The increasing needs for high-bandwidth transmission have propelled silicon-based optical modulator technology to a point where further performance improvements have become increasingly difficult to find, with driver-integrated devices reaching 224Gbps PAM-4 with the efficiency down to sub pJ/bit [1]. Due to the lack of a strong electro-optic effect in silicon, modulators have relied heavily on the plasma dispersion effect, primarily using carrier depletion. This has resulted in a large feature size, greater insertion loss, and limited modulation efficiency. This has motivated research on integrating other materials onto the silicon waveguide platform to realise optical modulation. Perovskite materials offer comparatively large electro-optic effects without the need for extrinsic dopings. This will avoid the absorption loss due to interactions with silicon dopants and provide increased modulation efficiency, allowing the required phase shift to be achieved at a shorter distance or with reduced drive power.

Silicon (Si) serves as the cornerstone material within the semiconductor industry due to its abundance and electronic characteristics. In the photonics field, its stable native cladding, silicon dioxide (SiO_2) with a high refractive index contrast facilitates high light confinement, enabling miniaturizing of devices [2]. Additionally, photonic components integrated onto a silicon-based platform allow the use of the same manufacturing processes as the CMOS technology, yielding better economics and wafers with fewer defects.

In recent years there has been research aiming to overcome the limitations of the plasma dispersion effect by integrating thin film lithium niobate (LN) and barium titanate (BTO) onto the silicon platform [3,4]. Thin film LN modulators have demonstrated high-speed performance with efficiencies comparable with carrier-depletion-based devices while maintaining low propagation loss and a linear transfer function [5, 6]. BTO-based modulators have measured a Pockels coefficient orders of magnitude greater than LN-based devices and in some cases, enhanced efficiency over MOSCAP-based silicon devices, reaching as low as 0.2V cm [7–9]. Among perovskite materials, KTN, characterized by its chemical composition $KTa_{1\text{-}x}Nb_xO_3$ emerges as an alternative. In comparison to other studied perovskites such as KH_2PO_4 and $BaTiO_3$, KTN stands out with the highest electro-optic coefficient of around $10^4 \mathrm{pm\,V}^{-1}$ (around two orders higher than the current research-focused material - lithium niobate ($LiNbO_2$) [10, 11]). [12, 13] demonstrated an EO modulator using buried KTN waveguides with < 0.05 dB mm^{-1} propagation loss, and projected a 5 V mm modulation efficiency through electrode and waveguide optimization. Further improvements on EO modulation of KTN can be achieved by exploiting electric-field enhanced permittivity [14], incorporating nanodisordered regions [15], and adopting a proposed modulation maximisation model in [16].

This paper provides a first demonstration of passive KTN waveguides integrated into a silicon photonic platform monolithically. We demonstrate passive KTN waveguide losses at 3.3dB mm^{-1}, which compare well to initial demonstrations of BTO waveguides with suboptimal loss at 4dB mm^{-1} [17]. Coupling structures to pass the light to and from silicon waveguides are also shown with a loss around 0.46 – 0.76dB. This integration approach holds promise due to its capability to capitalise on the large electro-optics effect with promise of miniaturised device size and enhanced modulation efficiency, harness silicon fabrication technology, and seamless integration with other silicon-based devices.

2. Design and Fabrication

2.1. Design Concept

The design consists of a KTN waveguide on top of a silicon strip waveguide platform separated by a thin silicon dioxide layer. The silicon waveguide is tapered down to a tip, which forces the mode to be coupled to the KTN waveguide. The same structure performs the reverse function. Cutback loss test structures are used for characterising the propagation losses of KTN and silicon waveguides and their transition loss. A passive imbalanced Mach-Zehnder interferometer (MZI) structure consisting of a multi-mode interferometer (MMI)-based splitter and combiner, silicon waveguide bends, and two waveguide arms incorporating transition structures along with KTN waveguides is also present on the chip.

2.2. Si-KTN Waveguide Transition Modelling

Lumerical EME was used to model a single transition from silicon to KTN with a total length of 160µm. The target structure, depicted in Figure 1, features a KTN waveguide with a width and thickness of 1.5µm and 360nm respectively, an oxide thickness of 100nm, and a silicon thickness of 220nm. The silicon waveguides have a tip width of 150nm tapered from a width of 450nm over a distance of 150µm. The simulated transition loss at a wavelength of 1550nm is 0.114dB.

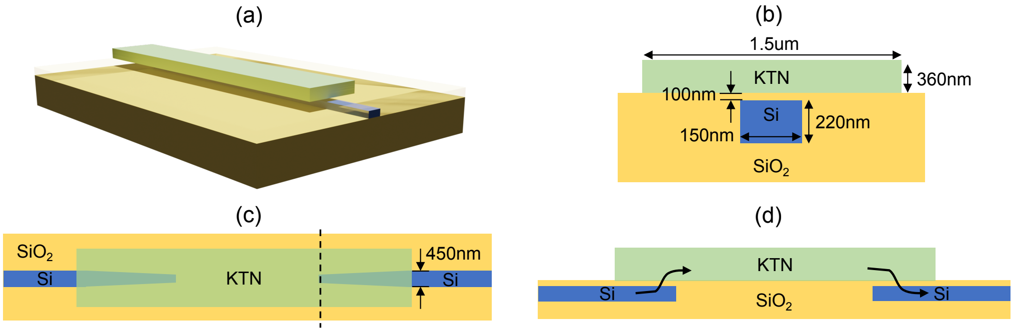

Fig. 1. (a) 3D schematics of the Si-KTN tapering section. (b) 2D cross-section (b) 2D top and (c) 2D yz-plane view of the target design transition structure.

2.3. Fabrication

Device fabrication was performed within the cleanroom facilities at the University of Southampton. It started with 200mm SOI wafers with a 220nm silicon overlayer and a 2µm buried oxide (BOX) layer. Grating couplers were etched 70nm into the silicon surface using a 248nm deep ultraviolet (DUV) scanner lithography and inductively coupled plasma (ICP) etching. Strip waveguides were defined by selectively etching the silicon layer completely through to the BOX layer. A 1µm silicon dioxide layer was deposited onto the wafer surface using plasma enhanced chemical vapour deposition (PECVD). This layer was then planarised and thinned to leave a 100nm silicon dioxide layer on top of the waveguide using chemical mechanical polishing (CMP). DUV lithography was then used to produce a liftoff mask on the wafer to define regions where KTN was required. A 360nm KTN layer was then deposited through RF sputtering at 200mm wafer scale from a KTN target.

Initial recipe parameters were developed from previously reported work [18]. The sputtering parameters were 200W RF power, pressure at 3mT, 100 sccm Ar flow, and 1 sccm O_2 flow. A 30nm silicon dioxide capping layer was deposited on top by RF sputtering with parameters of 90W RF power, pressure at 10mT, and 50 sscm Ar flow. After liftoff, DUV lithography and ion-beam etching was used to define waveguides within the KTN regions with smooth sidewalls. Microscopic and focused ion beam-scanning electron microscope (FIB-SEM) images of the fabricated chips can be seen in Fig.2. Finally, the wafer was diced into chips and cleaned, ready for testing.

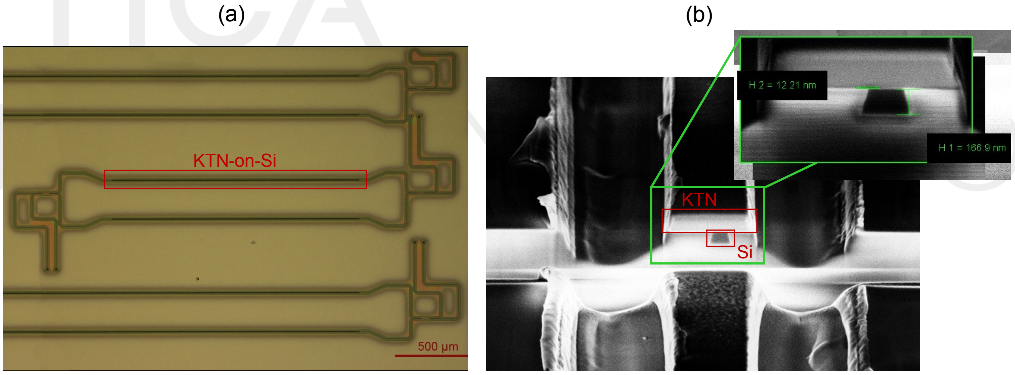

Fig. 2. (a) Microscopic view of MZI test structures. (b) An overview and close-up FIB-SEM images of the tapering section. It shows that the silicon is offset by 12.21nm, and the oxide layer between the two materials is polished away.

3. Result and Discussion

3.1. Passive Characterisation

Devices were characterised by passing light at a wavelength of 1550nm through and measuring the power transmission level. Grating couplers were defined on each waveguide's input and output sides to facilitate light coupling between optical fibers and the silicon chip. The propagation loss within the KTN waveguides and the transition loss of the KTN-to-Si interfaces were investigated. As depicted in Figure 3(a)(b), the propagation loss is approximately 0.45dB mm^{-1} for silicon (Si) and 3.3dB mm^{-1} for KTN. The transition of a mode propagating within a silicon waveguide to and from KTN induces a loss ranging from 0.46 to 0.76dB per transition, as illustrated in Fig.3(c). The higher loss than anticipated from simulation can be attributed to over-polishing and fabrication errors.

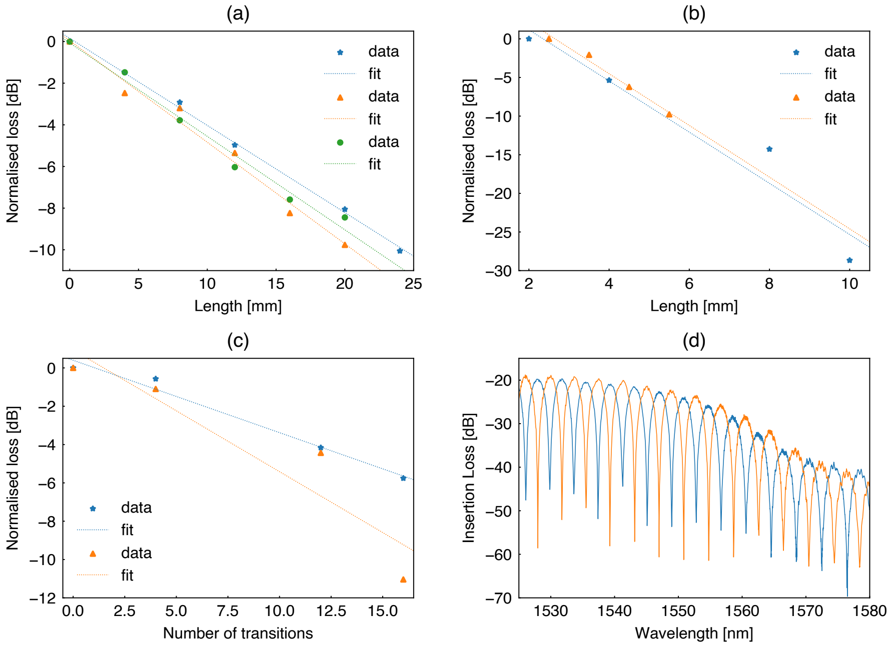

Fig. 3. Experimental results of passive characterisation of different waveguide structures across multiple chips. Normalised loss to the shortest length of (a) Si and (b) KTN. (c) Normalised loss to the smallest number of Si-KTN transitions. (d) Transmission spectrum of imbalanced MZI with KTN integrated into both arms.

Examination of Fig.2(c) reveals a lateral offset of the silicon within the transition region as well as overpolishing during the CMP process, resulting in complete removal of the 100nm oxide between the KTN and silicon layer, and a thinning of the silicon layer to 170nm. Additionally, the absence of top cladding on the chips makes the structures susceptible to loss from particles gathering on the surface during the preparation, dicing, and measurement stages.

The impact of the imperfections was examined by simulating a reference device using parameters of those observed in the fabricated devices, followed by simulating deviations in the device parameters from this reference. The baseline simulation featured a silicon waveguide with a width of 450nm and height of 170nm. The silicon taper region spans 150µm, with a starting width of 450nm leading to a tip width of 202nm. A KTN waveguide, with a width of 1.5µm, and a height of 360nm, was defined directly on top of the silicon waveguide without the 100nm oxide layer.

From Fig. 4, it can be seen that the baseline loss is within the range of the measured experimental loss (grey shading), showing that our simulated and experimental results largely agree. The impact of the variation of the different design parameters can also be observed. Compared to the initially targeted thickness of 220nm, the fabricated thickness of 170nm results in an increase in loss of 0.26dB. The graph shows that decreasing the thickness and width of the KTN material, as well as decreasing the width of the silicon tip, leads to an increase in optical output. The graph indicates an almost linear relationship between the KTN thickness, silicon tip width, and the loss, having a similar gradient of approximately -0.0012dB/nm. Lateral offsets between the positions of the KTN waveguide and the silicon waveguide have minimal impact on the power output, indicating the structure is resilient to such misalignments. These insights offer a preliminary guide for optimizing the geometry of Si-KTN waveguides, providing valuable

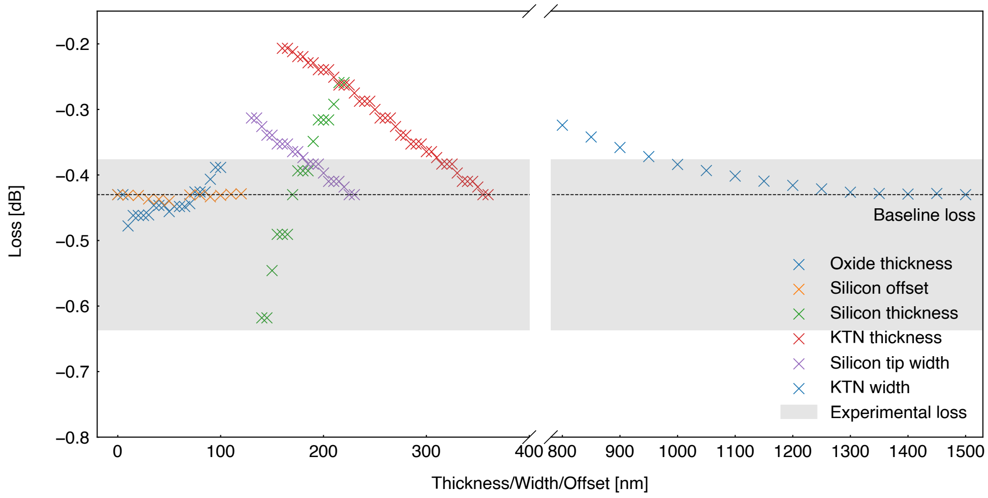

Fig. 4. Analysis of Si-KTN transition loss with various geometrical parameter variation around the baseline fabricated structure.

direction to reduce the loss.

The transmission spectrum of an imbalanced MZI with integrated KTN waveguides on both arms is illustrated in Figure 3(e). The extinction ratio (ER) exceeds 20dB, while the minimum insertion loss (IL_{min}) is approximately 20dB. The high ER of the MZI, coupled with a large electro-optic coefficient of KTN, allows for a reduction in the required modulator driving voltage, thereby enhancing the overall modulation efficiency.

4. Conclusion

This study provided a first insight into the feasibility of wafer-scale integration of KTN waveguides onto a silicon photonics platform and lays the initial groundwork for realising high-speed and efficient optical modulators. Despite passive KTN waveguides exhibiting a loss around an order of magnitude higher than their passive silicon counterparts, they remain comparable to the doped silicon waveguides required to form a modulator. Furthermore, the high electro-optic coefficients surpass those of most other materials, meaning that the propagation length required can be short and, therefore, lower the overall loss. As an initial step in Si-KTN integration, the propagation loss of 3.7dB mm^{-1} in KTN is similar to that reported in BTO at 4dB mm^{-1} without optimisation [17]. Previous research [19] has demonstrated a considerable loss reduction in BTO to around 0.6dB mm^{-1} with loss source identification. Such research conducted on KTN can yield reductions in losses in a similar manner to that reported in BTO. In addition, the Si-KTN integration reported in this work has yet to undergo geometry and fabrication optimisation.

Despite KTN's potential as an alternative modulator material, certain challenges persist. Improving fabrication quality and tackling issues related to the high dielectric constant remain a priority. The latter poses challenges, such as the need for higher driving currents and increased time constants [4,20]. Nonetheless, with ongoing progress in fabrication technology, we anticipate a rising interest in exploring Si-KTN-based modulators.

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Disclosures. The authors declare no conflicts of interest.

Data Availability Statement. Data underlying the results presented in this paper are available in Ref. [21].

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