Bias-Stress Effects in PE-ALD Poly-Crystalline ZnO-TFTs

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Abstract— We report on the impact of fixed bias-stress on the electrical characteristics of polycrystalline ZnO thin-film transistors (TFT). Positive and negative bias-stress is typically explored in amorphous metal-oxide TFTs, often at a single fixed bias point. In this work, we examine bias-stress effects in ZnO-TFTs with multiple fixed gate-source voltages ($V_{GS(fixed)}$), across a 24-hour period for each voltage point. Threshold voltage (V_{th}) is used to assess changes in ZnO-TFT electrical characteristics, with a stretched-exponential fit to model temporal trends in V_{th}. This method provides an insight into long-term charge carrier migration between polycrystalline ZnO channel and dielectric materials.

Introduction— ZnO thin-film transistors (ZnO-TFTs) have attracted significant research in recent years due to applications in display technologies, memory arrays, and heterogeneous integration. Poly-crystalline ZnO thin-films promise high electron-mobility up to 110 cm^2/(V·s) promoting fast switching and high on-current [1] , ultra-low off-current below 100 fA due to the wide bandgap of 3.4 eV [2], and low-temperature (<200℃) processing techniques such as remote plasma-enhanced atomic layer deposition (PE-ALD) promoting 2D and 3D heterogeneous integration [3]. These applications rely on the ZnO-TFT withstanding prolonged periods of fixed bias-stress

Experimental Procedure— ZnO-TFTs are fabricated on Si wafers with a 100 nm SiO_2 isolation layer with fabrication details in [4]. The cross-sectional schematic of the TFT stack-up is in Fig. 1(a) and a cross-sectional SEM image of a fabricated ZnO-TFT in Fig. 1(b). All measured TFTs have confirmed channel width of 50 µm and gate length 995 nm. Core-level O1s X-ray photoelectron spectroscopy (XPS) of ZnO is shown in Fig. 2(a) which, combined with Zn2p spectra (not shown), confirms stoichiometry of $Zn_{0.53}O_{0.47}$. X-ray diffraction (XRD) data for 40 nm ZnO on 30 nm Al_2O_3, both deposited by PE-ALD, are given in Fig. 2(b), indicating poly-crystallinity in the ZnO thin-film.

Electrical characterisation across 24-hour periods of both positive bias-stress (PBS) and negative bias-stress (NBS) is performed out to assess changes in TFT performance due to fixed bias-stress over time. V_{DS} is fixed at +10 V throughout. I_D-V_{GS} before and after 24-hours of PBS at $V_{GS(PBS)} = +8$ V are in Figs. 3(a) and 3(c), and 24-hours of NBS at $V_{GS(NBS)} = -8$ V are in Figs. 3(b) and 3(d). The temporal trend of ΔV_{th} is presented in Fig. 4(a), including dotted lines indicating stretched-exponential fit using Eqn. (1) from [5], where $V_{th(\infty)}$ is V_{th} at infinite time, τ is characteristic trapping time and β is a fitting term. Fitted $V_{th(\infty)}$ against $V_{GS(fixed)}$ is in Fig. 4(b).

$$(1) \quad \Delta V_{th}(t) = V_{th(\infty)}\left[1 - e^{-(t/\tau)^{\beta}}\right]$$

Conclusions— The observed shift in V_{th} under both positive bias-stress is likely caused by trapping of charge carriers in the dielectric under PBS, and de-trapping under NBS, illustrated in Fig. 1(a). Further measurements, fitting and parameter extraction will aim to clarify the electrical performance changes over time and support understanding of the precise mechanism for variation due to bias-stress on poly-crystalline ZnO-TFTs.

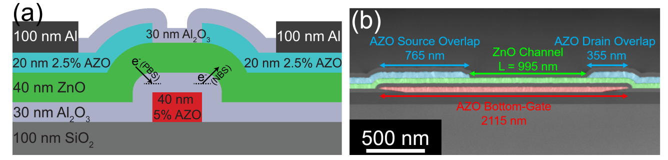

Fig. 1(a) ZnO-TFT cross-section schematic. (b) ZnO-TFT cross-section SEM with source-drain overlap.

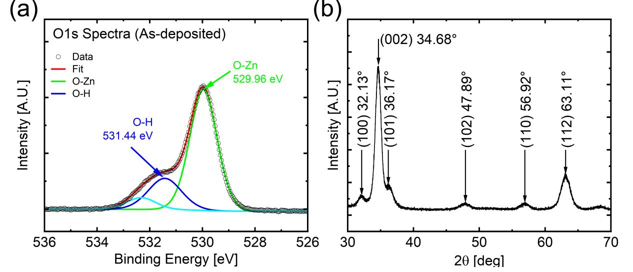

Fig. 2(a) XPS data for O1s of as-deposited ZnO thin-film. (b) XRD scan for as-deposited ZnO (40 nm) on Al_2O_3 (30 nm).

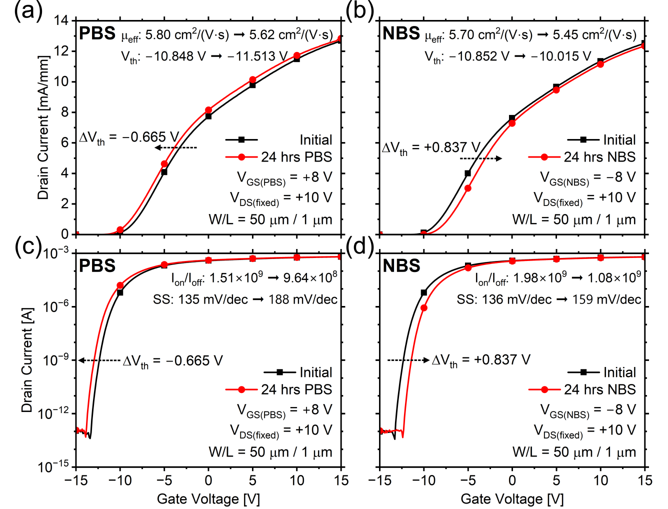

Fig. 3(a) Linear I_D-V_{GS} for ZnO-TFT under 24 hr PBS (V_{GS} = +8 V). (b) Linear I_D-V_{GS} for ZnO-TFT under 24 hr NBS (V_{GS} = −8 V). (c) Semi-log I_D-V_{GS} (PBS). (d) Semi-log I_D-V_{GS} (NBS).

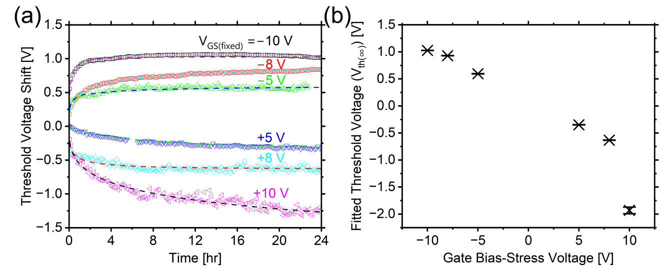

Fig. 4(a) ΔV_{th} against time at various V_{GS} with stretched-exponential fit in dotted lines. (b) Fitted $V_{th(\infty)}$ against $V_{GS(fixed)}$

References

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