Atomic Layer Deposition of Al-Doped ZnO Contacts for ZnO Thin-Film Transistors

Ben D. Rowlinson, Jiale Zeng, Joshua D. Akrofi, Christian Patzig, Martin Ebert, and Harold M.H. Chong

***Abstract*— We report on the fabrication of zinc oxide thin film transistors (ZnO-TFTs) with Al-doped ZnO (AZO) source-drain contacts with a range of different Al dopant concentrations. The source-drain contacts are deposited by thermal atomic layer deposition (ALD) with the Al:Zn atomic ratio varied between 1% and 5%, with an additional sample without AZO contacts. The ZnO channel and Al_2O_3 dielectric material are deposited by plasma-enhanced ALD. The physical properties of the as-deposited AZO thin films are measured by transmission electron microscopy, energy dispersive x-ray spectroscopy, atomic force microscopy, and spectroscopic ellipsometry. The AZO layers are measured electrically using linear transfer-length measurement structures and as the source-drain regions of ZnO-TFTs. We determine that Al:Zn ratios between 1.5% and 3.0% yield functioning transistors with switching characteristics. The fabricated ZnO-TFTs with 2.5% AZO contacts exhibit a contact resistance of 140 Ω/μm, steep sub-threshold swing of 130 mV/dec, on/off-current ratio of 1.9×10^9, threshold voltage of −6.81 V, low threshold voltage hysteresis of 10 mV, and field-effect mobility of 44.8 $cm^2/(V\cdot s)$.**

***Index Terms*— Zinc Oxide, Al-doped Zinc Oxide, Atomic Layer Deposition, Thin-Film Transistors, Source-Drain Contacts.**

I. Introduction

ZnO-based thin-film transistors (ZnO-TFTs) offer three significant benefits towards driving the future of display technologies, memory arrays, and heterogeneous integration: high electron-mobility up to 110 $cm^2/(V\cdot s)$ in TFTs promoting fast switching and high on-current [1], ultra-low off-current below 100 fA due to the wide bandgap of 3.4 eV [2], and low-temperature processing techniques (<200℃) promoting 2D and 3D integration compatibility of heterogeneous materials [3]. Methods for low-temperature deposition of ZnO include spin-coating, solution-based processing, pulsed laser deposition (PLD) and sputtering, however many of these techniques require a thermal annealing step to yield a functional transistor [4]. Furthermore, ZnO-TFTs can suffer from degraded electrical performance due to high top-surface roughness [5], voids in the thin-film [6], and the presence of trapped charges at the dielectric interface due to ambient exposure [7]. To improve the electrical performance of the TFT, high-quality ZnO material without these defects is required, ideally at temperatures below 200℃ to promote compatibility with heterogeneous integration of electronic devices [8]. The availability of high-quality ZnO thin-films by plasma-enhanced atomic layer deposition (PE-ALD) at temperatures below 200℃, coupled with low-damage and selective wet-etching techniques for patterning, makes these ZnO thin-films highly suitable for TFTs in heterogeneous integration with a wide array of existing and future, devices and substrates.

A well-known challenge for metal-oxide TFTs is obtaining a reliable source-drain contact method, which minimises contact resistance and maximises on/off-current ratio, particularly as gate length is scaled [9, 10]. Conductive Al-doped ZnO (AZO) contacts for ZnO and ZnO-based semiconductors have been demonstrated in previous works with fixed Al:Zn atomic ratio by sputtering [11, 12], ALD [13-15] and PLD [16, 17], with Al:Zn ratios up to 5%. Regardless of deposition method, the Al impurity acts as a shallow donor in ZnO [18]. AZO contacts act to reduce overall contact resistance by lowering the potential barrier formed at the semiconductor-metal interface, while matching well in terms of lattice constants [19, 20]. When considering those ZnO-TFTs with AZO contacts by a sputtering or PLD technique, sub-threshold swing above 400 mV/dec, on/off-current ratio in the 10^6 range, and electron mobility on the order of 10 $cm^2/(Vs)$ are observed. Additionally, typical values of contact resistance are on the order of 100-200 Ω/μm for ZnO-TFTs, with a minimum reported value of 84 Ω/μm when using Ar plasma treatment to improve the contact quality [21].

Despite the advances made using AZO as an intermediary contact material, the effect of Al:Zn ratio on both the contact resistance and TFT operation remains unclear. Therefore, we propose a fabrication process primarily using ALD for ZnO-TFTs by which the Al:Zn atomic ratio of AZO source-drain contact material is directly modulated using the ratio of Zn-based and Al-based ALD cycles. The AZO material is characterised using transmission electron microscopy (TEM), energy-dispersive x-ray spectroscopy (EDS), spectroscopic ellipsometry (SE), and atomic force microscopy (AFM). The AZO thin-films, of varying Al:Zn ratio, are electrically characterised using linear transfer-length method (TLM)

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measurement structures and ZnO-TFTs with AZO source-drain contact material. It is found that there is a finite range of Al:Zn atomic ratios (1.5% to 3.0%) for which the ZnO-TFTs exhibit switching characteristics.

II. Experimental Process

Three sets of linear TLM samples are prepared on Si chips with a 100 nm thermal oxide. These comprise of a sample with ZnO/Al contacts, ZnO/AZO(2.5%)/Al contacts, and ZnO/AZO(5.0%)/Al contacts. The ZnO semiconductor material is prepared by PE-ALD at 190℃ for a thickness of 40 nm, then wet etched by 1:1000 HCl:H_2O, before being passivated by a 30 nm layer of Al_2O_3 at 150℃ by PE-ALD. Contact vias are opened by a tetramethyl ammonium hydroxide (TMAH) wet-etch, and thermal-ALD is used to deposit the AZO contacts with a range of Al:Zn ratios. Trimethylaluminium (TMA) is used as the Al precursor and diethylzinc (DEZ) is used as the Zn precursor. H_2O is used as the reactant source for the thermal-ALD of AZO, and O_2 plasma is used in PE-ALD steps for Al_2O_3 dielectric and ZnO channel material. Finally, 100 nm Al metal is lifted-off to form the TLM structure. The TLM lengths (L_{TLM}) are between 10 µm and 50 µm in 10 µm increments, and the TLM width (W_{TLM}) is 150 µm.

These fabrication steps match what is later used in the fabrication of the ZnO-TFTs. Based on the TLM analysis, ZnO-TFTs are fabricated with a range of Al:Zn ratios. The cross-sectional schematic of the bottom-gate staggered ZnO-TFT is shown in Fig. 1(a). ZnO-TFTs are fabricated on a 150 mm Si wafer with a 100 nm thermal oxide. A 45 nm 5% Al-doped ZnO (AZO) thin-film is deposited by thermal-ALD at 175℃ to act as the gate electrode, and patterned by contact photolithography with an HCl wet-etch [22]. A 30 nm Al_2O_3 gate insulator and 40 nm ZnO channel layer are deposited using a contiguous PE-ALD process, using TMA at 150℃, and DEZ at 190℃, respectively [23, 24]. The PE-ALD ZnO channel has been tuned for FET operation in previous work [25]. The ZnO layer is patterned by HCl wet-etching, and a further 30 nm Al_2O_3 is deposited by PE-ALD at 150℃ to act as a passivation layer. Contact vias are selectively wet-etched by TMAH through Al_2O_3 layers to contact the AZO bottom-gate electrode and ZnO channel layer [26]. The wafer is cut with a diamond scribe tip and cleaved into seven identical chips. Each chip has a different ratio of Al:Zn for the AZO source and drain contacts, deposited by thermal-ALD using TMA and DEZ precursors and H_2O reactant at 175℃. The Al:Zn ratios used are 1.0%, 1.5%, 2.0%, 2.5%, 3.0%, 5.0%, and one sample with no AZO intermediate contact. These ratios are achieved using an even distribution of TMA and DEZ monolayers for a total of 200 thermal-ALD cycles. A layer of 100 nm Al by electron-beam evaporation is lifted-off to form metal probing pads.

III. Characterisation and Analysis

The fabricated TFTs have channel width W = 50 µm, and gate length L = 3 µm, verified by optical microscopy as per Fig. 1(b). All material thicknesses in the TLM and TFT structures are verified by SE (M2000-DI, J.A. Woollam) and surface profiling (DektakXT, Bruker). TEM (C_s-corrected ThermoFisher Titan 80-300 S/TEM), and EDS (SuperX, Bruker) are used to inspect cross-sectional lamellae with as-deposited thin-films of un-doped ZnO by PE-ALD, and 2.0% and 5.0% AZO by thermal-ALD. Each of the thin-films is deposited on a layer of PE-ALD Al_2O_3. The TEM images are shown in Fig. 2(a), 2(b), and 2(c) for un-doped ZnO, 2.0% AZO, and 5.0% AZO, respectively. Poly-crystalline structure is observed in all samples with crystal grains that extend the full thickness of the film. A fast Fourier transform (FFT) is applied to the TEM micrographs yielding c-axis lattice constants of 0.530 nm, 0.516 nm, and 0.521 nm for un-doped ZnO, 2.0% AZO, and 5.0% AZO, respectively, in close agreement with the theoretical value of 0.5207 [18]. EDS measurements for each of the material samples are made in an area of size 20 nm by 150 nm, and are shown in Fig. 2(d), with an inset figure showing a zoomed view of the $Al_K\alpha$ line. The Al:Zn atomic ratio is extracted based on the ratio of counts per second (CPS) at the characteristic energies of 1.012 keV for the $Zn_L\alpha$ line and 1.486 keV for the $Al_K\alpha$ line, taking into account the noise floor and background Al readings from the chamber. Al:Zn atomic ratios of 1.38% and 4.75% are measured for the 2.0% AZO and 5.0% AZO samples, respectively. There is a 31% and 5% discrepancy between the measured and intended Al:Zn ratio. Tapping mode AFM (XE7, Park Systems) measurements of a 1.0 µm × 1.0 µm area are shown in Fig. 3(a), Fig. 3(b), and Fig. 3(c), confirming the top-surface RMS roughness to be 0.837 nm, 0.866 nm, and 0.674 nm for as-deposited ZnO, 2.0% AZO, and 5.0% AZO, respectively. The samples used for AFM are deposited on Si substrate with 100 nm of thermal SiO_2 and a 30 nm layer of PE-ALD Al_2O_3. Table I summarises the findings from the TEM, EDS and AFM measurements, using samples of ZnO, 2.0% AZO and 5.0% AZO.

Electrical characterisation of both the linear TLM and the ZnO-TFTs is performed using a dual-channel source-meter unit (2636B, Keithley Instruments). The TLM resistance values (R_{TLM}) are calculated by sweeping the applied voltage between −10.0 V and +10.0 V in 100 mV increments and back three times and averaging the gradient of the I_{TLM}-V_{TLM} graph across those sweeps for each TLM length (L_{TLM}) interval. The R_{TLM}-L_{TLM} graph in Fig. 3(d) shows the extracted normalised contact resistance (R_{con}) values of the ZnO/Al, ZnO/AZO(2%)/Al, and ZnO/AZO(5%)/Al contact stacks and the linear regression model used to calculate R_{con} for each sample. The extracted R_{con} values are presented in Table II. Of these three contacts, 2.5% AZO is leading with an R_{con} of 140 Ω/µm.

To specify the suitable Al:Zn ratio range for AZO contacts, 7 different Al:Zn atomic ratios in the source-drain contacts are fabricated to gain insight into the dependency of the switching characteristics on AZO contact doping. Fig. 4(a) shows drain current (I_D) against drain-source voltage (V_{DS}), as a function of gate-source voltage (V_{GS}), for an example 2.5% AZO TFT with 100 mV increments in V_{DS} and 5 V increments in V_{GS}. These data indicate a saturation drain voltage ($V_{DS(sat)}$) of between 8.6 V and 9.5 V as V_{GS} is increased from −5.0 V to +15.0 V. Below the $V_{DS(sat)}$ point the TFT exhibits linear operation, demonstrating electrostatic control of the channel by the gate electrode. The V_{GS} is then swept between −15.0 V and +15.0 V in 100 mV increments for the forward I_D-V_{GS} sweep, and from +15.0 V back to -15.0 V for the reverse I_D-

V_{GS} sweep. A fixed V_{DS} of +1.0 V is used. Fig. 4(b) shows the linear plots and Fig. 4(c) shows semi-logarithmic plots of I_D-V_{GS}, with forward and reverse V_{GS} sweeps indicated by full and dashed lines, respectively. The threshold voltage (V_{th}), field-effect mobility (μ_{FE}), on-current to off-current ratio (I_{on}/I_{off}), and sub-threshold swing (*SS*) are extracted from I_D-V_{GS} graphs in Fig. 4(b) and 4(c) and are listed against Al:Zn ratio in Table III.

Four of the seven Al:Zn ratios (1.5%, 2.0%, 2.5%, and 3.0%) exhibit transistor switching, with the remaining ratios (un-doped ZnO, 1.0% and 5.0%) showing no transistor switching in the measured V_{GS} range. The lack of switching coupled with low I_D in the case of no AZO contacts and 1.0% AZO contacts indicates a high potential barrier at the contacts, attributed to poor Fermi energy level matching [27]. For the 5.0% Al:Zn sample, there is no transistor switching though the I_D is higher than for the un-doped ZnO and 1.0% AZO, suggesting Al incorporation into the channel material [28]. Incorporation of Al increases charge carrier density and shifts V_{th} to a more negative value, as illustrated by the comparable magnitude of I_D to the working TFTs, versus the un-doped ZnO and 1.0% AZO samples. The measured V_{th} values shows stability under high gate bias with low V_{th} hysteresis (ΔV_{th}) of −70 mV, +100 mV, −10 mV, and +300 mV, for 1.5%, 2.0%, 2.5% and 3.0% Al:Zn, respectively. This low V_{th} hysteresis can be attributed to low surface damage of the ZnO channel due to the use of wet-etching and low defect density at the dielectric interface [29]. Negative values of V_{th} can be understood by fixed negative charge in PEALD Al_2O_3 dielectric and passivation material [30]. Extracted values of μ_{FE} for working TFTs lie in a range between 37 $cm^2/(V{\cdot}s)$ and 48 $cm^2/(V{\cdot}s)$, with good agreement between forward and reverse sweeps. This mobility is indicative of high-quality ZnO channel material and low surface roughness at the dielectric-semiconductor interface, justifying the ALD fabrication approach for ZnO-TFTs. The ZnO-TFTs show switching characteristics with steep *SS* below 130 mV/dec for 1.5% to 2.5% Al:Zn, with a minimum value of 115 mV/dec for 1.5%. Steep *SS* is evidence of high-quality dielectric interface with minimal contamination and low trap-charge density [31]. An I_{on}/I_{off} above 10^9 is measured for 1.5%, 2.0% and 2.5% Al:Zn, with the maximum I_{on}/I_{off} being 1.9×10^9 for 2.5% Al:Zn. I_{on} above 100 μA, at V_{DS} of +1.0 V indicates good quality of the metal-semiconductor contact. Furthermore, ultra-low I_{off} below 100 fA is consistently measured between 1.5% and 3.0% AZO contacts. This is a result of both fully depleting the ZnO channel of carriers and low current leakage through high quality PE-ALD Al_2O_3 dielectric material. These two factors combine to give an overall I_{on}/I_{off} that is above 10^9 at a V_{DS} of +1.0 V. Overall electrical performance is optimal when using AZO source-drain contacts with Al:Zn ratios between 1.5% and 3.0%.

IV. Conclusions

This work has demonstrated the importance of high-quality ohmic contacts for ZnO-TFTs that can be achieved by low-temperature ALD of AZO intermediary contact layers. An R_{con} value of 140 Ω/μm for 2.5% AZO is reported and a method by which source-drain contacts can be optimised using low-temperature ALD to tune the material is demonstrated for metal-oxide TFTs. Considering the recent works in contact materials and methods for improving the contact in ZnO-TFTs, the measured electrical figures of merit are comparable to leading ZnO-TFT devices. The ZnO-TFTs with 2.5% AZO intermediary contacts are characterised by high μ_{FE} of 44.8 $cm^2/(V{\cdot}s)$, steep *SS* of 130 mV/dec, high I_{on}/I_{off} of 1.9×10^9, V_{th} of -6.81 V and ΔV_{th} of 10 mV, at V_{DS} of 1.0 V, demonstrating the benefits of low-temperature ALD AZO as intermediary contact layers for ZnO-TFTs.

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***Index Terms*— Zinc Oxide, Al-doped Zinc Oxide, Atomic Layer Deposition, Thin-Film Transistors, Source-Drain Contacts.**

I. Introduction

NO-based thin-film transistors (ZnO-TFTs) offer three significant benefits towards driving the future of display technologies, memory arrays, and heterogeneous integration: high electron-mobility up to 110 $cm^2/(V\cdot s)$ in TFTs promoting fast switching and high on-current [1], ultra-low off-current below 100 fA due to the wide bandgap of 3.4 eV [2], and low-temperature processing techniques (<200℃) promoting 2D and 3D integration compatibility of heterogeneous materials [3]. Methods for low-temperature deposition of ZnO include spin-coating, solution-based processing, pulsed laser deposition (PLD) and sputtering, however many of these techniques require a thermal annealing step to yield a functional transistor [4]. Furthermore, ZnO-TFTs can suffer from degraded electrical performance due to high top-surface roughness [5], voids in the thin-film [6], and the presence of trapped charges at the dielectric interface due to ambient exposure [7]. To improve the electrical performance of the TFT, high-quality ZnO material without these defects is required, ideally at temperatures below 200℃ to promote compatibility with heterogeneous integration of electronic devices [8]. The availability of high-quality ZnO thin-films by plasma-enhanced atomic layer deposition (PE-ALD) at temperatures below 200℃, coupled with low-damage and selective wet-etching techniques for patterning, makes these ZnO thin-films highly suitable for TFTs in heterogeneous integration with a wide array of existing and future, devices and substrates.

A well-known challenge for metal-oxide TFTs is obtaining a reliable source-drain contact method, which minimises contact resistance and maximises on/off-current ratio, particularly as gate length is scaled [9, 10]. Conductive Al-doped ZnO (AZO) contacts for ZnO and ZnO-based semiconductors have been demonstrated in previous works with fixed Al:Zn atomic ratio by sputtering [11, 12], ALD [13-15] and PLD [16, 17], with Al:Zn ratios up to 5%. Regardless of deposition method, the Al impurity acts as a shallow donor in ZnO [18]. AZO contacts act to reduce overall contact resistance by lowering the potential barrier formed at the

semiconductor-metal interface, while matching well in terms of lattice constants [19, 20]. When considering those ZnO-TFTs with AZO contacts by a sputtering or PLD technique, sub-threshold swing above 400 mV/dec, on/off-current ratio in the 10^6 range, and electron mobility on the order of 10 $cm^2/(Vs)$ are observed. Additionally, typical values of contact resistance are on the order of 100-200 Ω/μm for ZnO-TFTs, with a minimum reported value of 84 Ω/μm when using Ar plasma treatment to improve the contact quality [21].

Despite the advances made using AZO as an intermediary contact material, the effect of Al:Zn ratio on both the contact resistance and TFT operation remains unclear. Therefore, we propose a fabrication process primarily using ALD for ZnO-TFTs by which the Al:Zn atomic ratio of AZO source-drain contact material is directly modulated using the ratio of Zn-based and Al-based ALD cycles. The AZO material is characterised using transmission electron microscopy (TEM), energy-dispersive x-ray spectroscopy (EDS), spectroscopic ellipsometry (SE), and atomic force microscopy (AFM). The AZO thin-films, of varying Al:Zn ratio, are electrically characterised using linear transfer-length method (TLM) measurement structures and ZnO-TFTs with AZO source-drain contact material. It is found that there is a finite range of Al:Zn atomic ratios (1.5% to 3.0%) for which the ZnO-TFTs exhibit switching characteristics.

II. Experimental Process

Three sets of linear TLM samples are prepared on Si chips with a 100 nm thermal oxide. These comprise of a sample with ZnO/Al contacts, ZnO/AZO(2.5%)/Al contacts, and ZnO/AZO(5.0%)/Al contacts. The ZnO semiconductor material is prepared by PE-ALD at 190℃ for a thickness of 40 nm, then wet etched by 1:1000 $HCl:H_2O$, before being passivated by a 30 nm layer of Al_2O_3 at 150℃ by PE-ALD. Contact vias are opened by a tetramethyl ammonium hydroxide (TMAH) wet-etch, and thermal-ALD is used to deposit the AZO contacts with a range of Al:Zn ratios. Trimethylaluminium (TMA) is used as the Al precursor and diethylzinc (DEZ) is used as the Zn precursor. H_2O is used as the reactant source for the thermal-ALD of AZO, and O_2 plasma is used in PE-ALD steps for Al_2O_3 dielectric and ZnO channel material. Finally, 100 nm Al metal is lifted-off to form the TLM structure. The TLM lengths (L_{TLM}) are between 10 μm and 50 μm in 10 μm increments, and the TLM width (W_{TLM}) is 150 μm.

These fabrication steps match what is later used in the fabrication of the ZnO-TFTs. Based on the TLM analysis, ZnO-TFTs are fabricated with a range of Al:Zn ratios. The cross-sectional schematic of the bottom-gate staggered ZnO-TFT is shown in Fig. 1(a). ZnO-TFTs are fabricated on a 150 mm Si wafer with a 100 nm thermal oxide. A 45 nm 5% Al-doped ZnO (AZO) thin-film is deposited by thermal-ALD at 175℃ to act as the gate electrode, and patterned by contact photolithography with an HCl wet-etch [22]. A 30 nm Al_2O_3 gate insulator and 40 nm ZnO channel layer are deposited using a contiguous PE-ALD process, using TMA at 150℃, and DEZ at 190℃, respectively [23, 24]. The PE-ALD ZnO channel has been tuned for FET operation in previous work [25]. The ZnO layer is patterned by HCl wet-etching, and a further 30 nm Al_2O_3 is deposited by PE-ALD at 150℃ to act as a passivation layer. Contact vias are selectively wet-etched by TMAH through Al_2O_3 layers to contact the AZO bottom-gate electrode and ZnO channel layer [26]. The wafer is cut with a diamond scribe tip and cleaved into seven identical chips. Each chip has a different ratio of Al:Zn for the AZO source and drain contacts, deposited by thermal-ALD using TMA and DEZ precursors and H_2O reactant at 175℃. The Al:Zn ratios used are 1.0%, 1.5%, 2.0%, 2.5%, 3.0%, 5.0%, and one sample with no AZO intermediate contact. These ratios are achieved using an even distribution of TMA and DEZ monolayers for a total of 200 thermal-ALD cycles. A layer of 100 nm Al by electron-beam evaporation is lifted-off to form metal probing pads.

III. Characterisation and Analysis

The fabricated TFTs have channel width W = 50 μm, and gate length L = 3 μm, verified by optical microscopy as per Fig. 1(b). All material thicknesses in the TLM and TFT structures are verified by SE (M2000-DI, J.A. Woollam) and surface profiling (DektakXT, Bruker). TEM (C_s-corrected ThermoFisher Titan 80-300 S/TEM), and EDS (SuperX, Bruker) are used to inspect cross-sectional lamellae with as-deposited thin-films of un-doped ZnO by PE-ALD, and 2.0% and 5.0% AZO by thermal-ALD. Each of the thin-films is deposited on a layer of PE-ALD Al_2O_3. The TEM images are shown in Fig. 2(a), 2(b), and 2(c) for un-doped ZnO, 2.0% AZO, and 5.0% AZO, respectively. Poly-crystalline structure is observed in all samples with crystal grains that extend the full thickness of the film. A fast Fourier transform (FFT) is applied to the TEM micrographs yielding c-axis lattice constants of 0.530 nm, 0.516 nm, and 0.521 nm for un-doped ZnO, 2.0% AZO, and 5.0% AZO, respectively, in close agreement with the theoretical value of 0.5207 [18]. EDS measurements for each of the material samples are made in an area of size 20 nm by 150 nm, and are shown in Fig. 2(d), with an inset figure showing a zoomed view of the $Al_K\alpha$ line. The Al:Zn atomic ratio is extracted based on the ratio of counts per second (CPS) at the characteristic energies of 1.012 keV for the $Zn_L\alpha$ line and 1.486 keV for the $Al_K\alpha$ line, taking into account the noise floor and background Al readings from the chamber. Al:Zn atomic ratios of 1.38% and 4.75% are measured for the 2.0% AZO and 5.0% AZO samples, respectively. There is a 31% and 5% discrepancy between the measured and intended Al:Zn ratio. Tapping mode AFM (XE7, Park Systems) measurements of a 1.0 μm × 1.0 μm area are shown in Fig. 3(a), Fig. 3(b), and Fig. 3(c), confirming the top-surface RMS roughness to be 0.837 nm, 0.866 nm, and 0.674 nm for as-deposited ZnO, 2.0% AZO, and 5.0% AZO, respectively. The samples used for AFM are deposited on Si substrate with 100 nm of thermal SiO_2 and a 30 nm layer of PE-ALD Al_2O_3. Table I summarises the findings from the TEM, EDS and AFM measurements, using samples of ZnO, 2.0% AZO and 5.0% AZO.

Electrical characterisation of both the linear TLM and the ZnO-TFTs is performed using a dual-channel source-meter unit (2636B, Keithley Instruments). The TLM resistance values (R_{TLM}) are calculated by sweeping the applied voltage between −10.0 V and +10.0 V in 100 mV increments and back three

times and averaging the gradient of the I_{TLM}-V_{TLM} graph across those sweeps for each TLM length (L_{TLM}) interval. The R_{TLM}-L_{TLM} graph in Fig. 3(d) shows the extracted normalised contact resistance (R_{con}) values of the ZnO/Al, ZnO/AZO(2%)/Al, and ZnO/AZO(5%)/Al contact stacks and the linear regression model used to calculate R_{con} for each sample. The extracted R_{con} values are presented in Table II. Of these three contacts, 2.5% AZO is leading with an R_{con} of 140 Ω/μm.

To specify the suitable Al:Zn ratio range for AZO contacts, 7 different Al:Zn atomic ratios in the source-drain contacts are fabricated to gain insight into the dependency of the switching characteristics on AZO contact doping. Fig. 4(a) shows drain current (I_D) against drain-source voltage (V_{DS}), as a function of gate-source voltage (V_{GS}), for an example 2.5% AZO TFT with 100 mV increments in V_{DS} and 5 V increments in V_{GS}. These data indicate a saturation drain voltage ($V_{DS(sat)}$) of between 8.6 V and 9.5 V as V_{GS} is increased from −5.0 V to +15.0 V. Below the $V_{DS(sat)}$ point the TFT exhibits linear operation, demonstrating electrostatic control of the channel by the gate electrode. The V_{GS} is then swept between −15.0 V and +15.0 V in 100 mV increments for the forward I_D-V_{GS} sweep, and from +15.0 V back to -15.0 V for the reverse I_D-V_{GS} sweep. A fixed V_{DS} of +1.0 V is used. Fig. 4(b) shows the linear plots and Fig. 4(c) shows semi-logarithmic plots of I_D-V_{GS}, with forward and reverse V_{GS} sweeps indicated by full and dashed lines, respectively. The threshold voltage (V_{th}), field-effect mobility (μ_{FE}), on-current to off-current ratio (I_{on}/I_{off}), and sub-threshold swing (*SS*) are extracted from I_D-V_{GS} graphs in Fig. 4(b) and 4(c) and are listed against Al:Zn ratio in Table III.

Four of the seven Al:Zn ratios (1.5%, 2.0%, 2.5%, and 3.0%) exhibit transistor switching, with the remaining ratios (un-doped ZnO, 1.0% and 5.0%) showing no transistor switching in the measured V_{GS} range. The lack of switching coupled with low I_D in the case of no AZO contacts and 1.0% AZO contacts indicates a high potential barrier at the contacts, attributed to poor Fermi energy level matching [27]. For the 5.0% Al:Zn sample, there is no transistor switching though the I_D is higher than for the un-doped ZnO and 1.0% AZO, suggesting Al incorporation into the channel material [28]. Incorporation of Al increases charge carrier density and shifts V_{th} to a more negative value, as illustrated by the comparable magnitude of I_D to the working TFTs, versus the un-doped ZnO and 1.0% AZO samples. The measured V_{th} values shows stability under high gate bias with low V_{th} hysteresis (ΔV_{th}) of −70 mV, +100 mV, −10 mV, and +300 mV, for 1.5%, 2.0%, 2.5% and 3.0% Al:Zn, respectively. This low V_{th} hysteresis can be attributed to low surface damage of the ZnO channel due to the use of wet-etching and low defect density at the dielectric interface [29]. Negative values of V_{th} can be understood by fixed negative charge in PEALD Al_2O_3 dielectric and passivation material [30]. Extracted values of μ_{FE} for working TFTs lie in a range between 37 $cm^2/(V \cdot s)$ and 48 $cm^2/(V \cdot s)$, with good agreement between forward and reverse sweeps. This mobility is indicative of high-quality ZnO channel material and low surface roughness at the dielectric-semiconductor interface, justifying the ALD fabrication approach for ZnO-TFTs. The ZnO-TFTs show switching characteristics with steep *SS* below 130 mV/dec for 1.5% to 2.5% Al:Zn, with a minimum value of 115 mV/dec for 1.5%. Steep *SS* is evidence of high-quality dielectric interface with minimal contamination and low trap-charge density [31]. An I_{on}/I_{off} above 10^9 is measured for 1.5%, 2.0% and 2.5% Al:Zn, with the maximum I_{on}/I_{off} being 1.9×10^9 for 2.5% Al:Zn. I_{on} above 100 μA, at V_{DS} of +1.0 V indicates good quality of the metal-semiconductor contact. Furthermore, ultra-low I_{off} below 100 fA is consistently measured between 1.5% and 3.0% AZO contacts. This is a result of both fully depleting the ZnO channel of carriers and low current leakage through high quality PE-ALD Al_2O_3 dielectric material. These two factors combine to give an overall I_{on}/I_{off} that is above 10^9 at a V_{DS} of +1.0 V. Overall electrical performance is optimal when using AZO source-drain contacts with Al:Zn ratios between 1.5% and 3.0%.

IV. Conclusions

This work has demonstrated the importance of high-quality ohmic contacts for ZnO-TFTs that can be achieved by low-temperature ALD of AZO intermediary contact layers. An R_{con} value of 140 Ω/μm for 2.5% AZO is reported and a method by which source-drain contacts can be optimised using low-temperature ALD to tune the material is demonstrated for metal-oxide TFTs. Considering the recent works in contact materials and methods for improving the contact in ZnO-TFTs, the measured electrical figures of merit are comparable to leading ZnO-TFT devices. The ZnO-TFTs with 2.5% AZO intermediary contacts are characterised by high μ_{FE} of 44.8 $cm^2/(V \cdot s)$, steep *SS* of 130 mV/dec, high I_{on}/I_{off} of 1.9×10^9, V_{th} of -6.81 V and ΔV_{th} of 10 mV, at V_{DS} of 1.0 V, demonstrating the benefits of low-temperature ALD AZO as intermediary contact layers for ZnO-TFTs.

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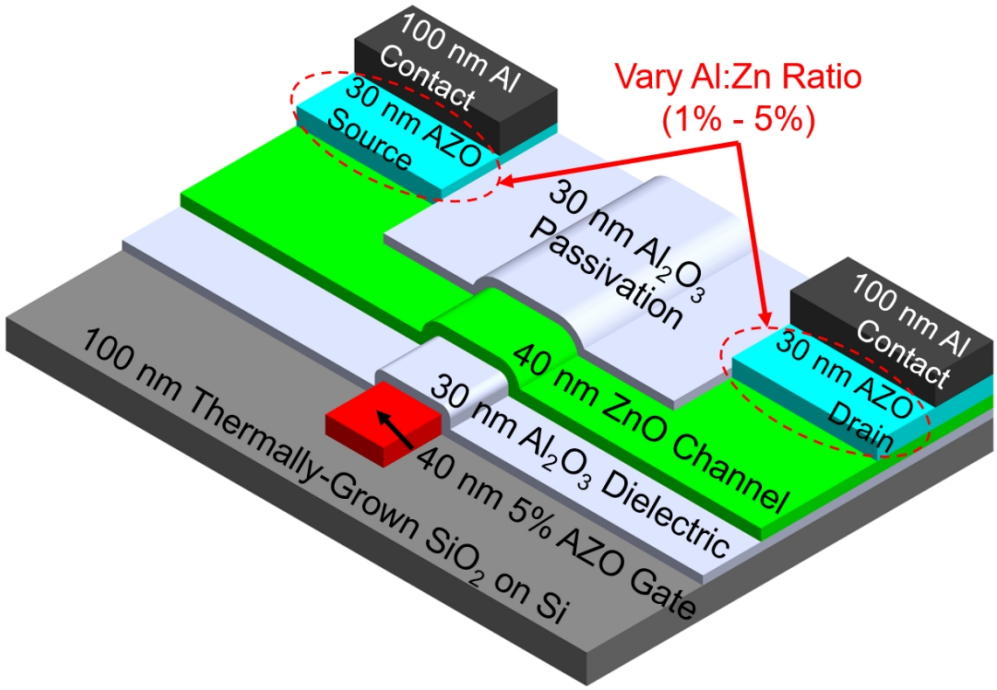

Fig. 1(a) Exploded cross-section schematic view of the fabricated ZnO-TFT.

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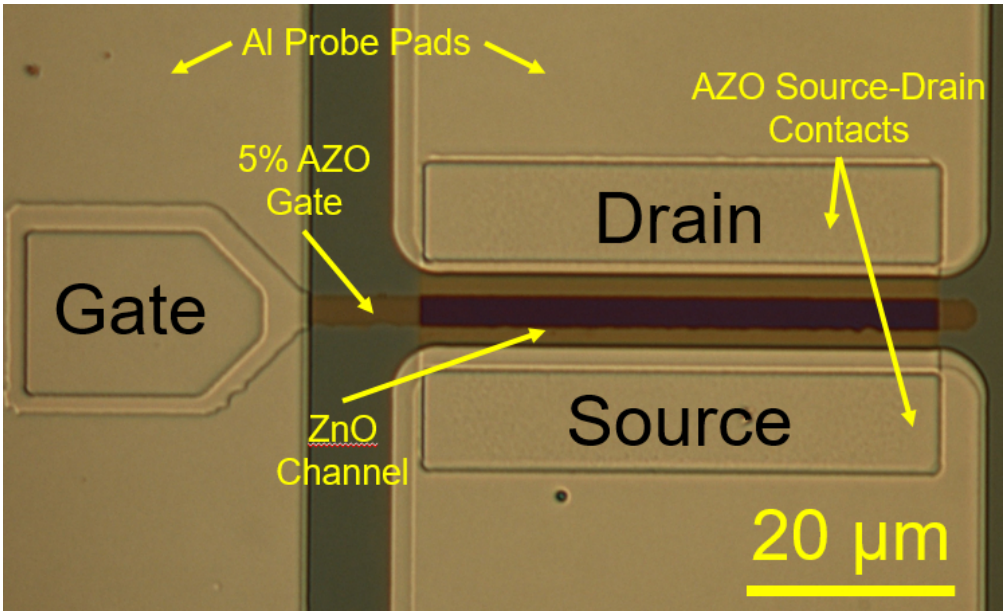

Fig. 1(b) Top-view micrograph of a fabricated ZnO-TFT with 2.5% AZO contacts. Channel size W/L = 50 μm/3 μm.

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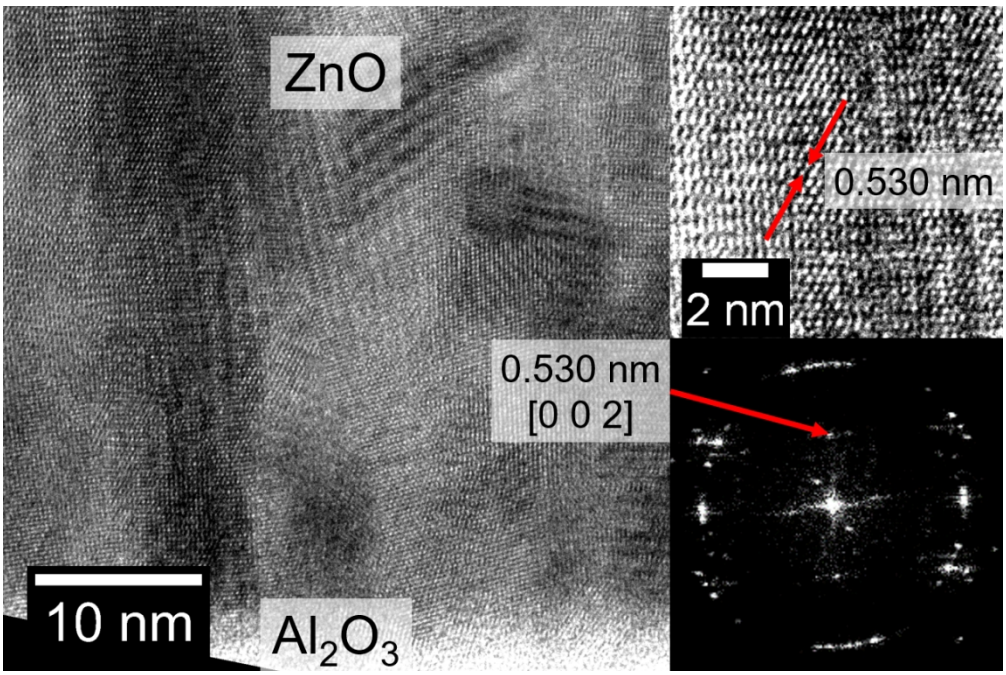

Fig. 2(a) TEM at 300 kV of un-doped ZnO (×295k, left), zoomed-in view (top right), and an FFT (bottom left).

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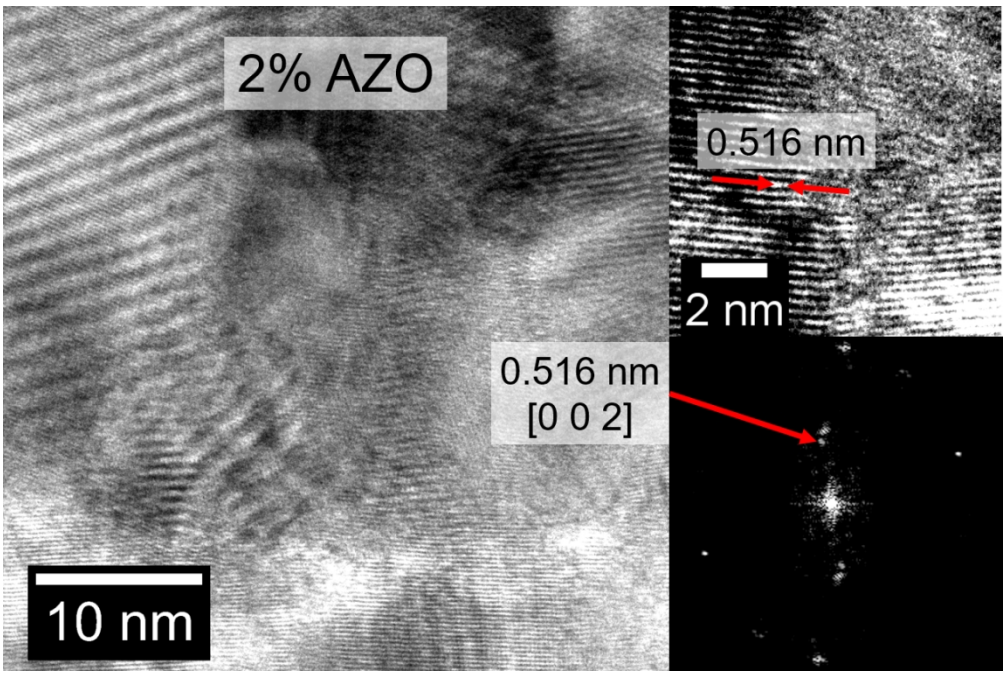

Fig. 2(b) TEM at 300 kV of 2.0% AZO (×295k, left), zoomed-in view (top right), and an FFT (bottom left).

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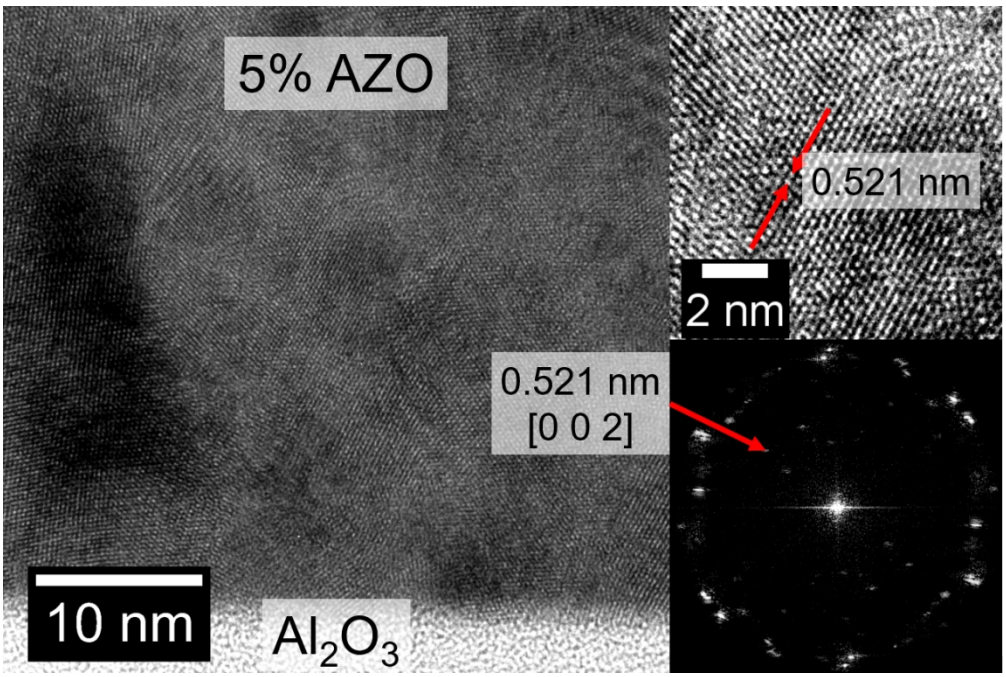

Fig. 2(c) TEM at 300 kV of 5.0% AZO (×295k, left), zoomed-in view (top right), and an FFT (bottom left).

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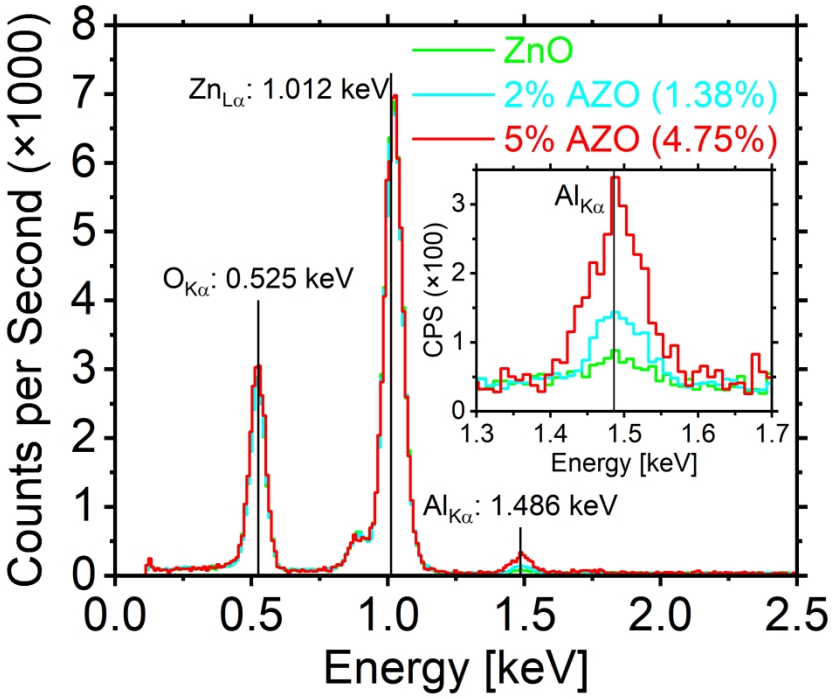


Fig. 2(d) EDS of un-doped ZnO (in green), 2.0% AZO (in blue), and 5.0% AZO (in red). Spectral lines for $O_{K\alpha}$, $Zn_{L\alpha}$, and $Al_{K\alpha}$ are labelled. Inset: Zoomed-in view of $Al_{K\alpha}$ line.

692x529mm (118 x 118 DPI)

Material	TEM c-axis Length [nm]	EDS Al:Zn Ratio [%]	AFM RMS Surface Roughness [nm]
ZnO	0.530	-	0.837
2.0% AZO	0.516	1.38 %	0.866
5.0% AZO	0.521	4.75 %	0.674

Table Ⅰ) Summary of TEM, EDS, and AFM material characterisation for ZnO, 2.0% AZO and 5.0% AZO.

316x104mm (38 x 38 DPI)

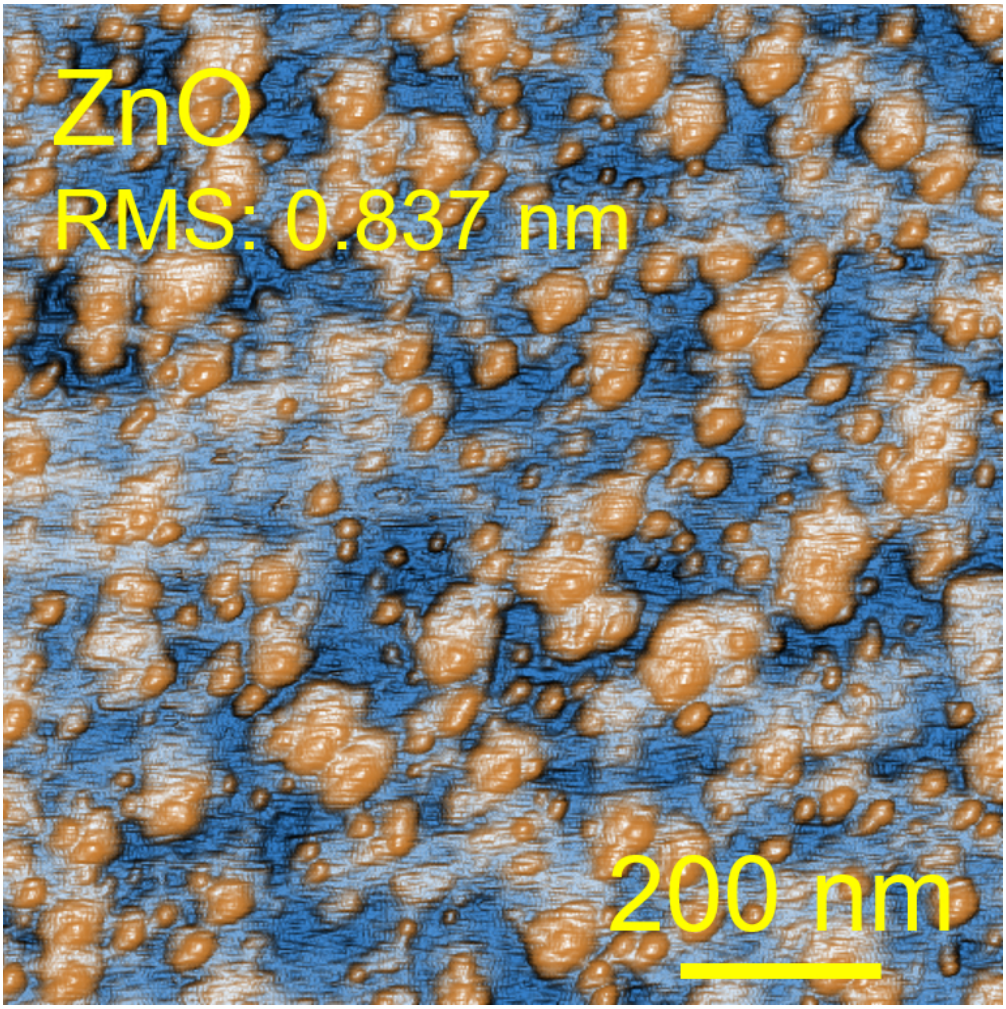


Fig. 3(a) AFM image of as-deposited ZnO on Al_20_3. RMS roughness is 0.837 nm.

512x512mm (38 x 38 DPI)

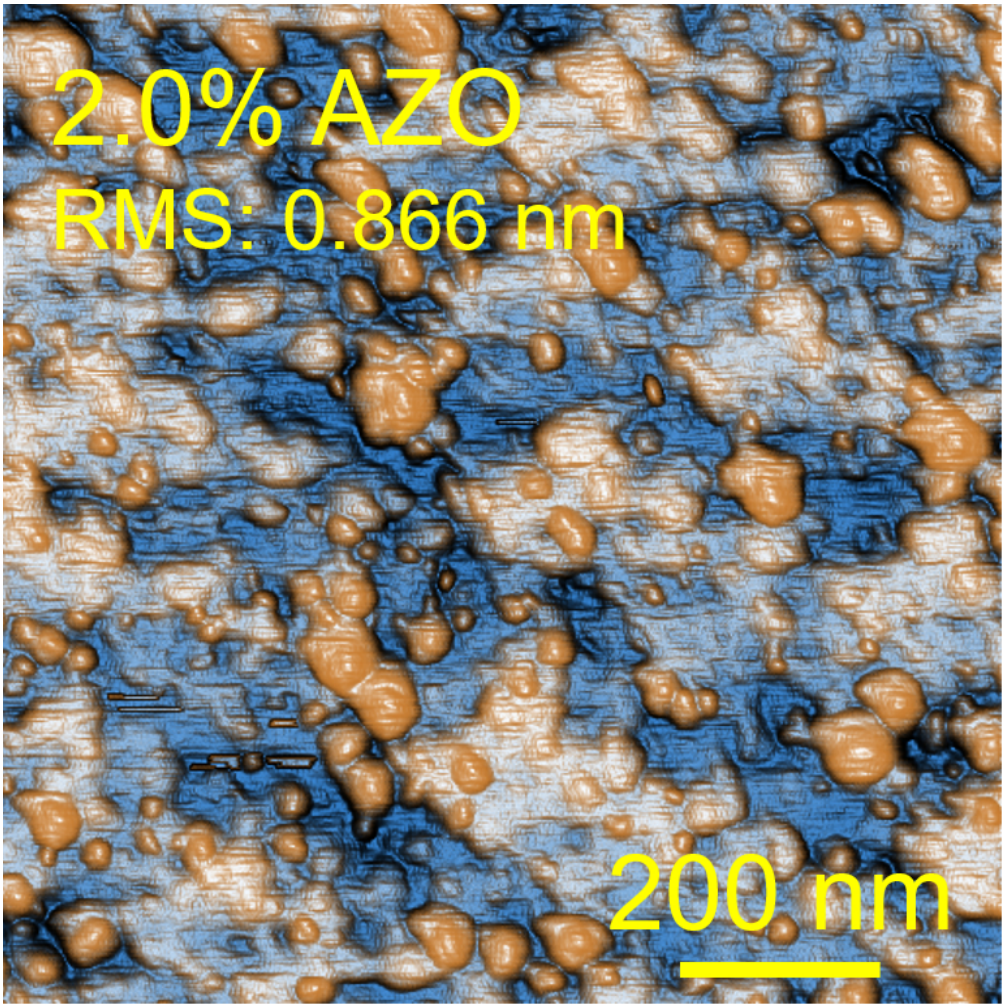


Fig. 3(b) AFM image of as-deposited 2.0% AZO on Al_20_3. RMS roughness is 0.866 nm.

513x513mm (38 x 38 DPI)

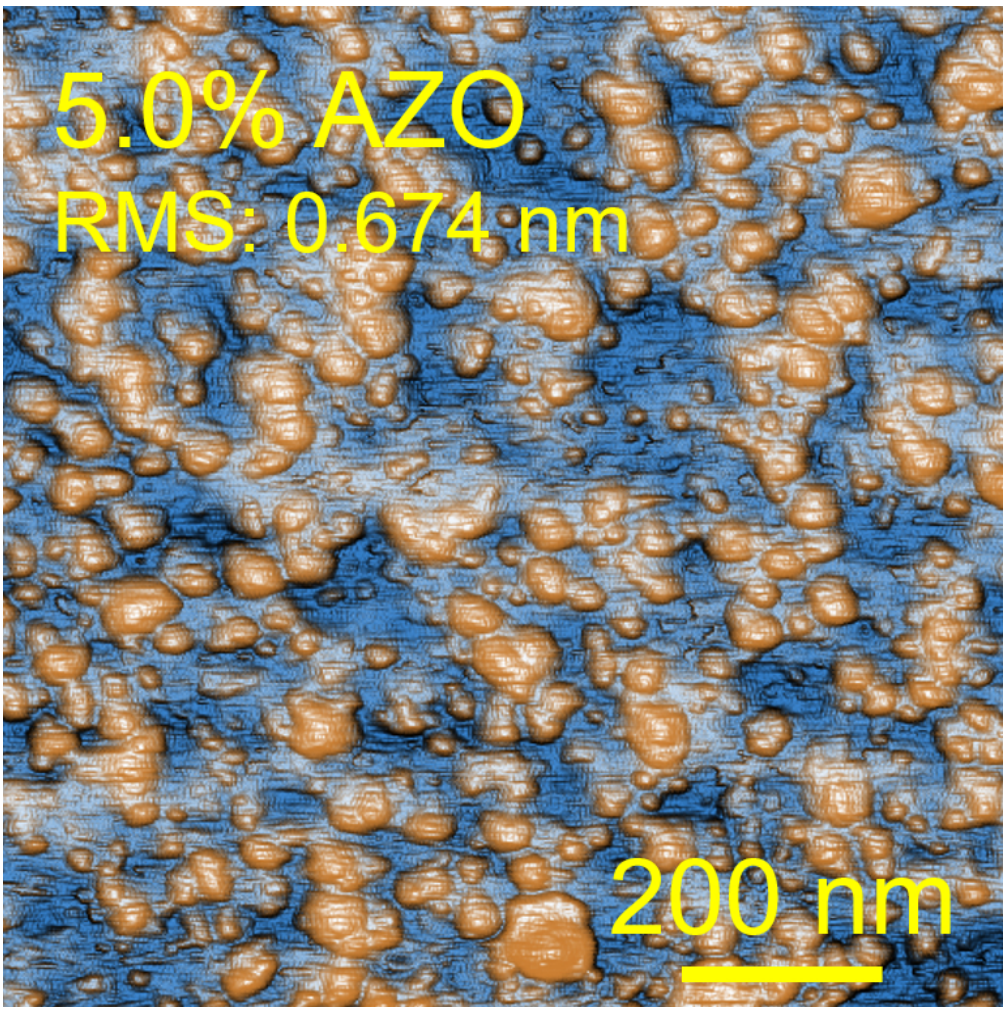


Fig. 3(c) AFM image of as-deposited 2.0% AZO on Al_20_3. RMS roughness is 0.674 nm.

512x512mm (38 x 38 DPI)

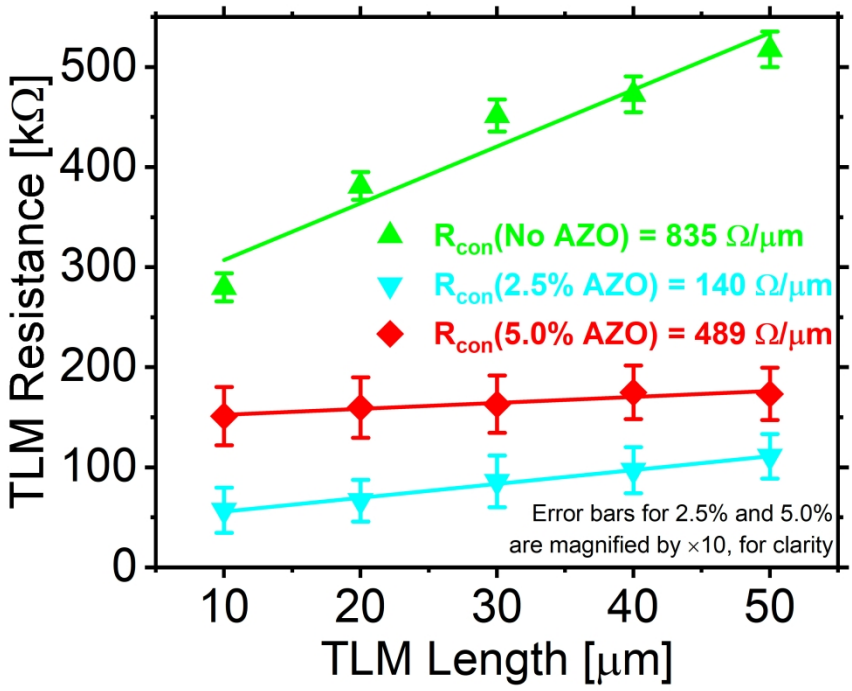


Fig. 3(d) TLM Measurements of R_{TLM}-L_{TLM} for direct Al contact (in green), 2.5% AZO contacts (in blue) and 5.0% AZO contacts (in red).

692x529mm (118 x 118 DPI)

Contact Material	R_{con} [Ω/μm]
No AZO	835
2.5% AZO	140
5.0% AZO	489

Table Ⅰ Ⅰ) Summary of TLM measurements.

118x88mm (38 x 38 DPI)

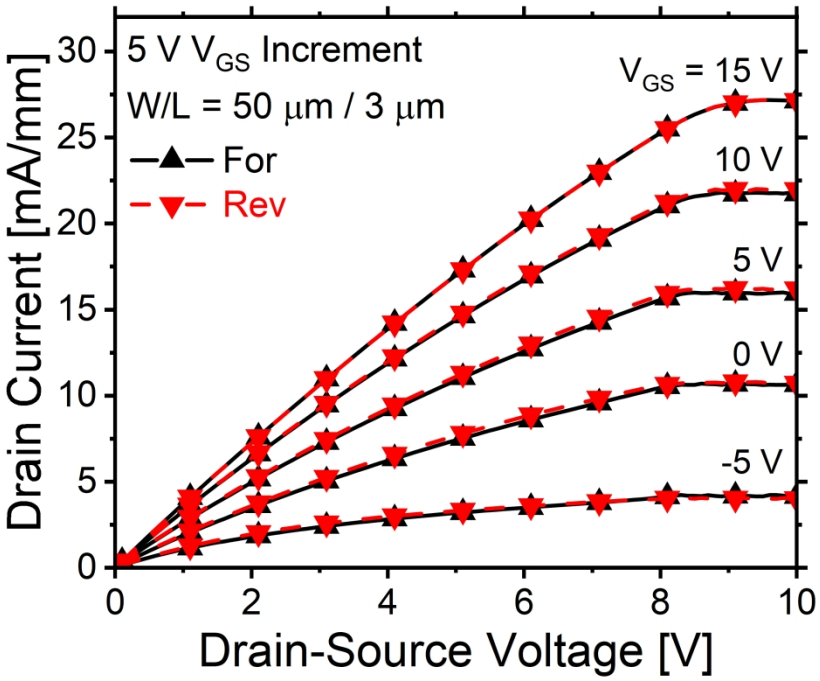


Fig. 4(a) I_D-V_{DS} with increasing V_{GS} (2.5% AZO contacts).

692x529mm (118 x 118 DPI)

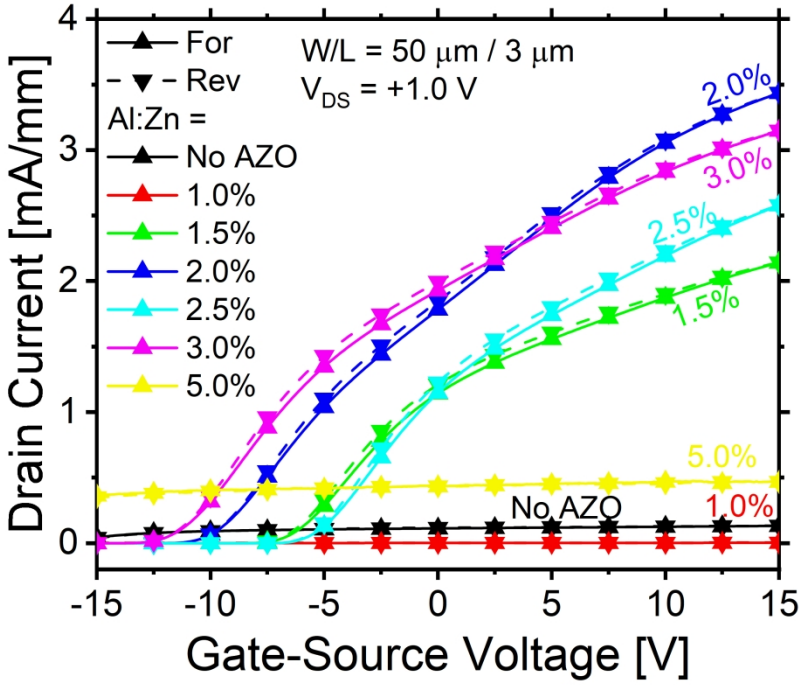


Fig. 4(b) Linear plot of I_D-V_{GS} with varying Al:Zn ratios of AZO contacts.

692x529mm (118 x 118 DPI)

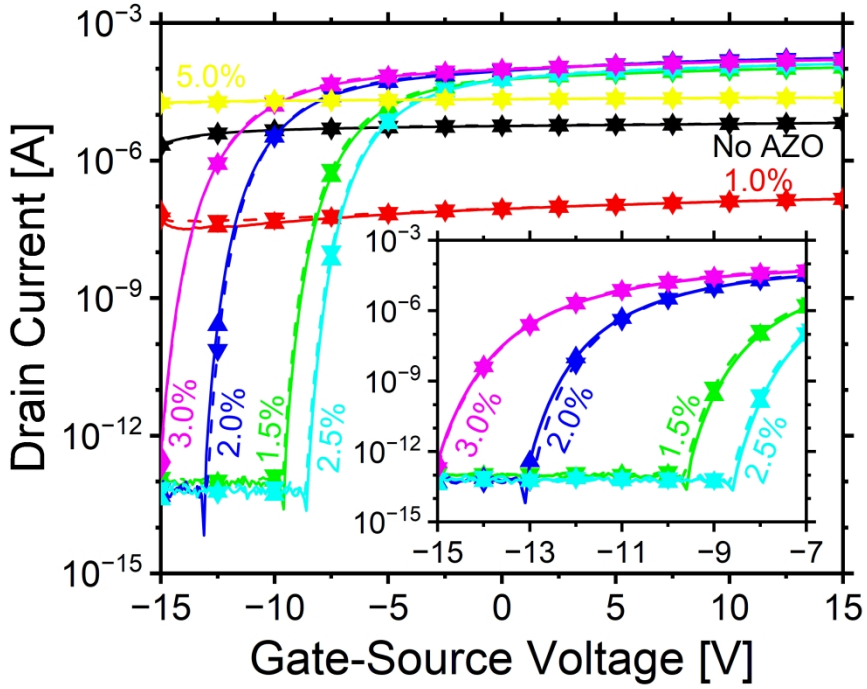


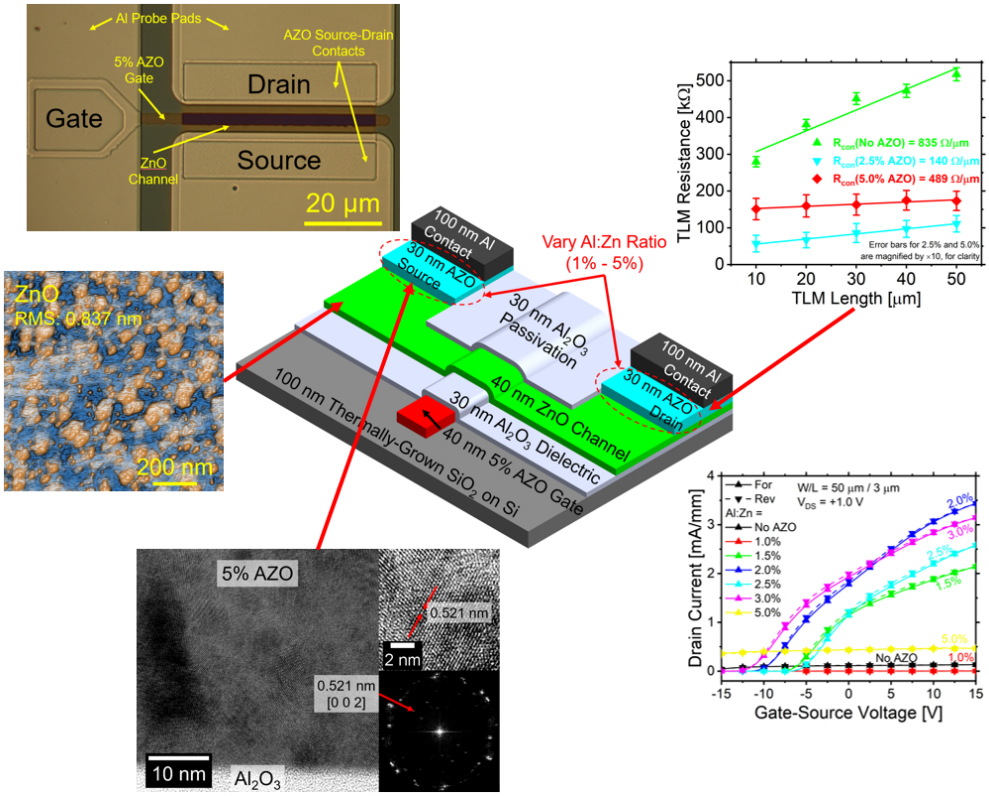
Fig. 4(c) Semi-log plot of I_D-V_{GS} with varying Al:Zn ratios of AZO. Line colour is the same as for Fig. 4(b). Inset: Zoomed-in view of sub-threshold characteristics.

692x529mm (118 x 118 DPI)

Contact Material	V_{GS} Sweep Direction	μ_{FE} [$cm^2/(Vs)$]	V_{th} [V]	ΔV_{th} [V]	SS [mV/dec]	I_{on}/I_{off}
1.5% AZO	Forward	37.6	-7.82	-0.07	101	1.1×10^9
	Reverse	42.2	-7.89		132	9.8×10^8
2.0% AZO	Forward	38.2	-11.3	+0.10	119	2.2×10^9
	Reverse	44.3	-11.2		130	2.5×10^9
2.5% AZO	Forward	41.9	-6.81	-0.01	121	2.1×10^9
	Reverse	47.5	-6.82		138	1.7×10^9
3.0% AZO	Forward	35.9	-13.3	+0.30	245	2.2×10^8
	Reverse	44.5	-13.0		142	3.0×10^8

Table Ⅰ Ⅰ Ⅰ) Measured electrical figures of merit against Al:Zn ratio of AZO contacts.

352x129mm (38 x 38 DPI)



675x539mm (38 x 38 DPI)