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Impact of bias stress and endurance switching on electrical characteristics of polycrystalline ZnO-TFTs with Al_2O_3 gate dielectric

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Abstract

This study experimentally investigates electrical characteristics and degradation phenomena in polycrystalline zinc oxide thin-film transistors (ZnO-TFTs). ZnO-TFTs with Al_2O_3 gate dielectric, Al-doped ZnO (AZO) source–drain contacts, and AZO gate electrode are fabricated using remote plasma-enhanced atomic layer deposition at a maximum process temperature of 190 °C. We employ positive bias stress (PBS), negative bias stress (NBS), and endurance cycling measurements to evaluate the ZnO-TFT performance and examine carrier dynamics at the channel-dielectric interface and at grain boundaries in the polycrystalline channel. DC transfer measurements yield a threshold voltage of −5.95 V, a field-effect mobility of 53.5 $cm^2/(V{\cdot}s)$, a subthreshold swing of 136 mV dec^{-1}, and an on-/off-current ratio above 10^9. PBS and NBS measurements, analysed using stretched-exponential fitting, reveal the dynamics of carrier trapping and de-trapping between the channel layer and the gate insulator. Carrier de-trapping time is 88 s under NBS at −15 V, compared to 1856 s trapping time under PBS at +15 V. Endurance tests across 10^9 cycles assess switching characteristics and temporal changes in ZnO-TFTs, focusing on threshold voltage and field-effect mobility. The threshold voltage shift observed during endurance cycling is similar to that of NBS due to the contrast in carrier trapping/de-trapping time. A measured mobility hysteresis of 19% between the forward and reverse measurement directions suggests grain boundary effects mediated by the applied gate bias. These findings underscore the electrical resilience of polycrystalline ZnO-TFTs and the aptitude for 3D heterogeneous integration applications.

Supplementary material for this article is available online

Keywords: zinc oxide, thin-film transistors, atomic layer deposition, bias stress, switching endurance

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1. Introduction

Three-dimensional (3D) heterogeneous integration represents the next leap in semiconductor technology, enabling the monolithic assembly of new electronic layers for More-than-Moore development [1]. However, integrating additional semiconductor layers presents a set of complex challenges. These include a stringent temperature constraint (<400 °C), a limited range of compatible semiconductor materials, and a requirement for robust nanofabrication processes. Metal–oxide thin-film transistors (TFTs) meet these specifications by leveraging low-temperature techniques, such as atomic layer deposition (ALD), sputtering and chemical vapour deposition for high-quality semiconductor thin films. Alongside well-established applications in backplane display drivers, research and development of metal–oxide TFTs is increasingly motivated by applications in 3D monolithic heterogeneous integration technologies [2]. For example, metal–oxide TFTs can integrate between heterogeneous functionalities on-chip, such as memory, logic, optoelectronics, and sensors [3–5], enabled by low-temperature, low-damage and highly compatible nanofabrication steps.

In particular, ZnO-based TFTs have come to the fore in metal–oxide TFTs research due to the ability to deposit high-quality polycrystalline thin-films at temperatures below 400 °C [6, 7]. Furthermore, the wide-bandgap of ZnO (3.37 eV) facilitates sub-1 fA/μm off-current [8], and electron mobility up to 110 $cm^2/(V{\cdot}s)$ in thin-films enables significantly faster switching than comparable a-Si TFTs [9]. Oxide-based TFTs with amorphous material are finding specific applications in display active matrices [10, 11], logic circuits [12], memory drivers [13], flexible electronics [14, 15], and low-power RFID circuitry [16]. However, the effects of fixed bias stress, endurance cycling, and grain boundary scattering on the electrical performance and switching of polycrystalline ZnO-TFTs are rarely reported. Prolonged bias stress, whether it be positive or negative, can promote migration of metal atoms and ion impurities into the channel region of ZnO-TFTs, acting to increase current leakage by introduction of defect states in the semiconductor bandgap, reducing on-/off-current ratio [17, 18]. Degradation in the electrical stability and hysteresis effects have been observed in metal–oxide TFTs during periods of high drain bias due to charge-trapping effects in the dielectric [19–21]. Dielectric breakdown due to excessive gate bias is a frequent issue in metal–oxide TFTs [22]. Dielectric breakdown can be mitigated using thicker insulator layers, however this compromises electrostatic control of the channel [23]. Furthermore, metal–oxide TFTs frequently suffer from electrical degradation and breakdown effects under prolonged bias stress conditions due to self-heating effects [24–26]. Regions of high thermal and electrical resistance suffer in particular from self-heating breakdown which can be mitigated by use of properly matched source–drain contacts [27].

Identifying the phase and crystal structure of the channel material is critical to understanding the switching characteristics of metal–oxide TFTs. Charge carriers in a-Si and poly-Si TFTs arises from impurity doping, however conduction in ZnO typically arises from Oxygen vacancies and ubiquitous Hydrogen [28]. Carrier scattering dynamics at the channel-insulator interface are material and phase-dependent therefore warrant independent investigation into the degradation and stress effects specific to polycrystalline metal–oxide TFTs.

Channels with a polycrystalline phase contain a number of crystal grain boundaries with either well-defined or random crystal growth direction, depending on the deposition conditions. Each of these crystal grain boundaries acts as a gate-dependent potential barrier in the channel [29]. Since planar TFT architectures utilise lateral current flow perpendicular to the crystal growth orientation, potential barriers at grain boundaries are critical to understanding carrier conduction. There is increasing interest in more complex TFT architectures, such as vertical-TFTs, to mitigate grain boundary effects [30, 31], though these encounter difficulties in scalability and planarisation for 3D integration.

To enable 3D heterogeneous integration, the maximum fabrication temperature of functional layers is kept strictly below 400 °C. Low-temperature techniques for ZnO thin-films include spin-coating [32], solution-based processing [33], and sputtering [34], however thin films produced by these techniques require a thermal annealing step to yield a functional transistor [35, 36]. Even with the annealing step, the TFTs fabricated by these methods frequently suffer from poor electrical performance due to high interface roughness [37], voids in the thin film [38], and trapped species at the dielectric interface due to atmospheric exposure [39]. To improve the electrical properties of the TFT, high-quality ZnO semiconductor material without such defects must be used [40]. The availability of high-quality ZnO and Al_2O_3 thin-films by ALD [41, 42], coupled with low-damage and highly selective wet-etching techniques for patterning, makes these ZnO-TFTs suitable for integration with a wide array of existing devices and substrates.

Experimental data on metal–oxide TFTs with a fixed bias stress are typically collected over durations between 60 s to 10 h [43–54]. Extrapolation is frequently used to determine TFT lifetime, often at a single fixed bias value. A more comprehensive view of ZnO-based TFTs is desirable to understand carrier dynamics and charge-trapping effects. To address the shortfall in long-term characterisation of ZnO-TFTs, this work uses 24 h durations of bias stress and a wide range of stress voltages, between −15 V and +15 V. The threshold voltage shift over time under fixed bias stress is fitted using a stretched-exponential model, yielding the projected threshold voltage shift and characteristic trapping/de-trapping time of charge carriers. Similarly, thermal stress is frequently utilised as an important method of accelerated aging testing [55]. However, this work assesses the charge carrier dynamics in the channel due to bias stress. Published works on metal–oxide TFT longevity and stability focus on fixed gate and drain bias stress conditions without considering the impact of switching the TFT channel repeatedly ‘on’ and ‘off’. Such cycling measurements are an effective emulation of the working conditions

of ZnO-TFTs in power switching, control systems, and logic circuits. Endurance cycling across 10^9 cycles is used in this study to examine electrical resilience, underlying degradation mechanisms, and grain-boundary scattering effects, thereby providing an effective emulation of switching conditions for applications in level shifting, memory control, and logic circuitry.

2. Experimental methods

ZnO-TFTs are fabricated using on a 150 mm Si wafer with a 100 nm thermal oxide isolation layer. A schematic of the TFT layers is shown in figure 1(a). A 35 nm layer of Al-doped ZnO (AZO) is deposited by thermal-ALD at 175 °C for the bottom-gate electrode. Trimethylaluminium (TMA) and diethylzinc (DEZ) precursors are used as Al and Zn sources respectively, with a H_2O pulse as the reactant for the AZO layers. A 1:20 ratio between TMA cycles and DEZ cycles is used to achieve Al doping of 5% in the AZO. The AZO gate electrode is patterned by contact photolithography using S1813 positive photoresist and is wet-etched by a 1:1000 dilution of 37% HCl in de-ionised water. A 30 nm layer of Al_2O_3 gate dielectric is deposited at 150 °C using plasma-enhanced ALD (PE-ALD) (Oxford Instruments, FlexAL), with a TMA precursor, followed by a 40 nm ZnO thin-film for the channel layer using the DEZ precursor at 190 °C, without breaking vacuum between the two depositions [56, 57]. Tapping mode atomic-force microscopy (AFM) confirms the root-mean squared top surface roughness of the as-deposited ZnO thin-film on Al_2O_3 to be 0.559 nm, with the AFM data shown in the supplementary material. The ZnO channel material is patterned by the same combination of S1813 photoresist and 1:1000 HCl wet-etch as for the AZO bottom-gate, thereby avoiding ion-bombardment and plasma-induced roughness to the active ZnO channel material [58, 59]. A 30 nm layer of Al_2O_3 is deposited by PE-ALD at 150 °C to passivate the channel material. AZ2020 negative photoresist is used to lift-off 30 nm AZO (2.5% Al:Zn) deposited by thermal-ALD. Contact vias are selectively wet-etched by a 1:100 dilution of 25% tetramethyl ammonium hydroxide in de-ionised water through the Al_2O_3 layers to contact the bottom-gate and channel layers simultaneously, with the AZO layers acting as an etch-stop layer. The gate, source and drain contact pads are patterned using AZ2020 and a 100 nm layer of Al metal is deposited by long-throw electron-beam evaporation and lifted-off. A false-colour scanning transmission electron microscopy (STEM) image of the cross-section in presented in figure 1(b) to illustrate the overlap of source–drain contacts. The 5.0% AZO bottom-gate is shown in red, the 2.5% AZO source–drain regions in blue, and the ZnO channel in green. The observed mismatch of the source and drain regions is attributed to unintentional alignment errors during optical lithography steps. The TFTs have a confirmed channel width $W = 50$ μm and effective gate length $L = 995$ nm. Figure 1(c) shows a summary of the fabrication steps. Material thicknesses are measured by spectroscopic ellipsometry (J.A. Woollam M2000-DI) and surface profiling (Bruker DektakXT).

Figure 2(a) shows a (TEM, C_s-corrected ThermoFisher Titan 80–300) cross-section of a ZnO-TFT alongside the energy dispersive x-ray spectroscopy (EDS, Bruker SuperX) elemental map of Si, C, O, Al, and Zn. Figures 2(b) and (c) illustrate the vertical grain boundary structure of the ZnO channel, with a Fourier transform plot in figure 2(d). X-ray photoelectron spectroscopy (XPS, Thermo Scientific Theta Probe) data for the ZnO channel material are shown for a survey spectrum, O1s region and Zn2p region are shown in figures 3(a)–(c), respectively, and are used to confirm a stoichiometry of $Zn_{0.57}O_{0.43}$. Grazing incidence x-ray diffraction (GI-XRD, Rigaku SmartLab) is used to confirm the polycrystalline ZnO thin film in figure 3(d). The full details of the experimental methods used in this study and interpretation of the EDS, TEM, XPS, and GI-XRD data can be found in Sections S1, S2 and S3 of the supplementary material, which detail Device Imaging, Material Characterisation and Electrical Characterisation, respectively.

3. Electrical results and discussion

3.1. DC ZnO-TFT characterisation

Figure 4(a) shows the I_D–V_{DS} plot, with upward-pointing triangles and solid lines indicating the forward sweep and downward triangles and dotted lines indicating the reverse sweep. These data confirm electrostatic control of the semiconductor channel by the gate, and indicate I_D saturation at a V_{DS} of 9 V. Figure 4(b) shows the linear I_D–V_{GS} data. V_{DS} is increased from 1 V to 8 V in 1 V increments, as indicated by an arrow. The negative values of V_{th} (-5.95 V and -6.02 V for forward and reverse sweeps, respectively, at 8 V V_{DS}), are attributed to fixed negative charge contribution from PE-ALD Al_2O_3 dielectric [60]. Low V_{th} hysteresis of -70 mV is observed. The values of μ_{FE} between 9.8 cm^2/(V·s) and 10.5 cm^2/(V·s) at 1 V V_{DS}, and 53.5 cm^2/(V·s) and 56.4 cm^2/(V·s) at 8 V V_{DS}, are indicative of high-density polycrystalline ZnO channel material with low surface roughness of 0.559 nm at the dielectric-semiconductor interface. Minimal interface roughness is enabled by avoiding breaking chamber vacuum during the contiguous growth of PE-ALD ZnO and Al_2O_3 thin films. Figure 4(c) presents these same I_D–V_{GS} data in a semi-logarithmic plot, similarly with an arrow indicating direction of increasing V_{DS}. A high I_{on}/I_{off}, above 10^{10} at 8 V V_{DS}, is achieved by maximising I_{on} using well-matched AZO/Al bilayer contacts [61], and minimising I_{off} using PE-ALD Al_2O_3 to reduce gate current leakage and fully depleting the ZnO channel of carriers in the subthreshold region. Figure 4(d) shows a zoomed-in view of the sub-threshold region of the semi-logarithmic plot of I_D–V_{GS}, to demonstrate *S.S.* between 136 mV dec^{-1} and 158 mV dec^{-1} at 8 V V_{DS}. This steep *S.S.* can be understood by low trap density at the semiconductor-insulator interface [62]. Using C_{ox} and *S.S.* measurements, the trap density is calculated to be 4.87×10^{12} cm^{-2}eV^{-1} for the

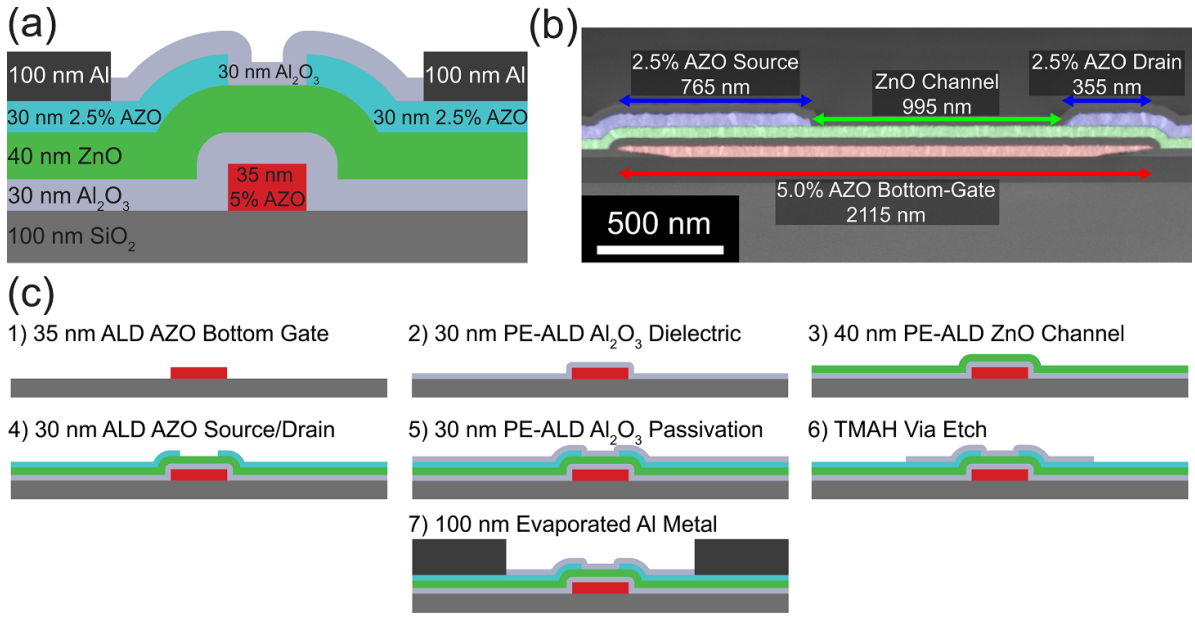

Figure 1. (a) Cross-section schematic of the fabricated ZnO-TFT. (b) False colour cross-sectional S-TEM of ZnO-TFT with effective channel length of 995 nm. (c) Schematic sequence of fabrication steps for ZnO-TFTs, starting from a Si wafer with 100 nm thermal oxide.

forward V_{GS} sweep and 6.28×10^{12} cm^{-2}eV^{-1} for the reverse sweep. Table 1 summarises the extracted values of V_{th}, μ_{FE}, *S.S.*, and I_{on}/I_{off} values at a V_{DS} of 1 V and 8 V.

3.2. Positive and negative bias stress (PBS and NBS)

PBS and NBS DC characterisation are performed over a period of 24 h, using multiple different bias stress voltages applied to the gate ($V_{GS(PBS)}$ and $V_{GS(NBS)}$, respectively). V_{DS} is fixed throughout the PBS and NBS measurements at +10 V to put the TFT in the saturation regime and apply high current stresses to the channel. Current stresses in the channel lead to Joule heating and promote electron injection into the insulator layer by thermionic emission [53]. Joule heating effects would be experienced during operation of a ZnO-TFT in many applications. To avoid the impact of non-volatile trapped charge effects and enable a fair comparison between biasing conditions, a fresh ZnO-TFT located in the same region of the substrate is used for each value of $V_{GS(PBS)}$ and $V_{GS(NBS)}$. This ensures that each PBS and NBS measurement of the ZnO-TFTs is unaffected by any previous charging or degradation of the TFT. The maximum value of $V_{GS(PBS)}$ and $V_{GS(NBS)}$ is +15 V and −15 V, respectively. At greater V_{GS}, the Al_2O_3 insulator material suffers dielectric breakdown. At low bias, V_{th} shift is minimal therefore these additional data shown in the supplementary material.

A set of I_D–V_{GS} plots for ZnO-TFTs with PBS and NBS applied are presented in figure 5. The black line denotes the initial measurement of I_-–V_{GS}, with the red line representing the shift after 24 h of PBS or NBS. The $V_{GS(PBS)}$ is fixed at +15 V for 24 h of PBS measurements in figures 5(a) and (b), which are the linear and semi-logarithmic plots, respectively. Similarly, figures 5(c) and (d) present the evolution of I_D–V_{GS} after 24 h of $V_{GS(NBS)}$ at −15 V. In the case of PBS, there is a shift of V_{th} in the *x*-direction by −2.09 V. In contrast, the I_D–V_{GS} characteristics shift under NBS in the *x*-direction by +1.64 V. The TFT parameters of V_{th}, μ_{FE}, *S.S.*, and I_{on}/I_{off} are extracted from figure 5 and presented in table 2. After 24 h of PBS at +15 V, μ_{FE} reduces by 8.7% from 71.1 cm^2(V·s)$^{-1}$ to 64.9 cm^2(V·s)$^{-1}$, *S.S.* increases by 28% from 145 mV dec^{-1} to 186 mV dec^{-1}, and I_{on}/I_{off} decreases by 10% from 7.76×10^9–6.98×10^9. These data show that PBS does not significantly affect carrier mobility or switching characteristics over 24 h of continuous electrical stress. However, I_{off} is increased by the presence of additional trapped charge carriers in the gate dielectric and at the channel-dielectric interface.

After 24 h of NBS at −15 V, μ_{FE} reduces by 7.8% from 70.9 cm^2(V·s)$^{-1}$ to 65.4 cm^2(V·s)$^{-1}$, *S.S.* increases by 24% from 144 mV dec^{-1} to 178 mV dec^{-1}, and I_{on}/I_{off} increases by 2.8% from 7.24×10^9–7.44×10^9. These data show that NBS does not significantly affect carrier mobility over 24 h of continuous electrical stress. However, subthreshold characteristics are severely impacted leading to markedly degraded *S.S.* and increased I_{off}, due to the presence of trapped charges at the channel-dielectric interface.

Figures 6(a) and (b) present the extracted ΔV_{th} shift against time under 24 h of PBS with an applied $V_{GS(PBS)}$ ranging from +2 V to +15 V, using linear and logarithmic time scales, respectively. Figures 6(c) and (d) present the ΔV_{th} shift against time under 24 h of NBS with an applied $V_{GS(PBS)}$ ranging from −2 V to −15 V, using linear and logarithmic time scales, respectively. Below ±2 V, there is a very small shift in V_{th}, <100 mV. Such a small shift is challenging to fit using the stretched exponential function, therefore the ±2 V to ±15 V range is used.

The mathematical expression for V_{th} in a TFT is given in equation (1) [63]. φ_{ms} is the Fermi-level difference between

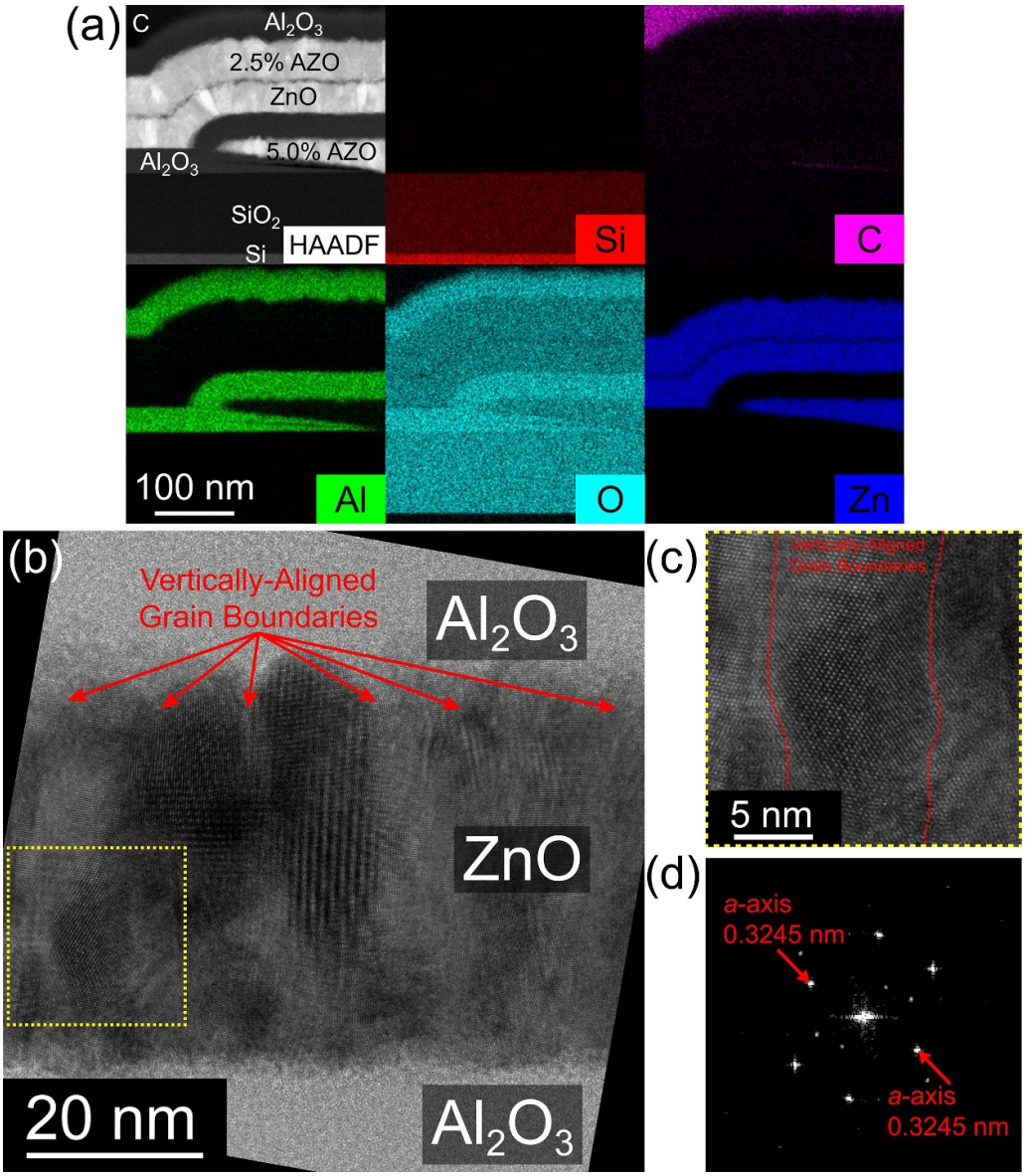

Figure 2. (a) HAADF S-TEM image of ZnO-TFT cross-section with EDS mapping for Si, C, Al, O and Zn. (b) TEM of ZnO channel material with lower layer of Al_2O_3 insulator and upper layer of Al_2O_3 passivation. Red dotted lines indicate the distribution of vertically-aligned grain boundaries. (c) Zoomed-in view of figure 2(b) region with dotted yellow outline showing a crystalline region of the polycrystalline film. (d) FFT of TEM image in figure 2(c) indicating *a*-axis length of 0.3245 nm.

the gate electrode and semiconductor channel material. Q_f is the fixed surface charge, Q_m the mobile ionic charge, Q_{ot} the dielectric trapped charge, and C_{ox} the capacitance, each quantity is expressed per unit area. q is the elementary charge, N_D is the fixed donor concentration, ε_{ZnO} is the permittivity of ZnO, and ψ_B is the difference between Fermi level and intrinsic Fermi level of ZnO, used to define the fully depleted condition,

$$V_{th} = \left[\varphi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_{ox}}\right] + \frac{\sqrt{2qN_D\varepsilon_{ZnO}(2\psi_B)}}{C_{ox}} + 2\psi_B. \quad (1)$$

The mechanism of V_{th} shift under PBS/NBS conditions implies at least one quantity in equation (1) is time-dependent. The parameters φ_{ms}, ε_{ZnO}, Q_f, $N_{D,}$ and C_{ox} are determined by the constant material properties and device structure. Under bias-stress conditions, the applied V_{GS} and Fermi energy level of the ZnO does not vary over time, implying ψ_B is fixed. Therefore, the time-dependent variables to consider are Q_m and Q_{ot}. Under bias stress conditions, charge carriers are trapped and de-trapped based on the sign of $V_{GS(fixed)}$, modulating Q_m and Q_{ot}, and shifting V_{th} accordingly. Under PBS, electrons in the channel are injected into the gate dielectric, increasing Q_m and Q_{ot}, and shifting V_{th} in the negative direction. This effect is illustrated in figure 7(a) showing the PBS condition whereby hot carriers are injected into the dielectric [25]. Similarly, under NBS conditions electrons are de-trapped from the dielectric material, decreasing Q_m and Q_{ot} and shifting V_{th} in the positive direction. The de-trapping mechanism

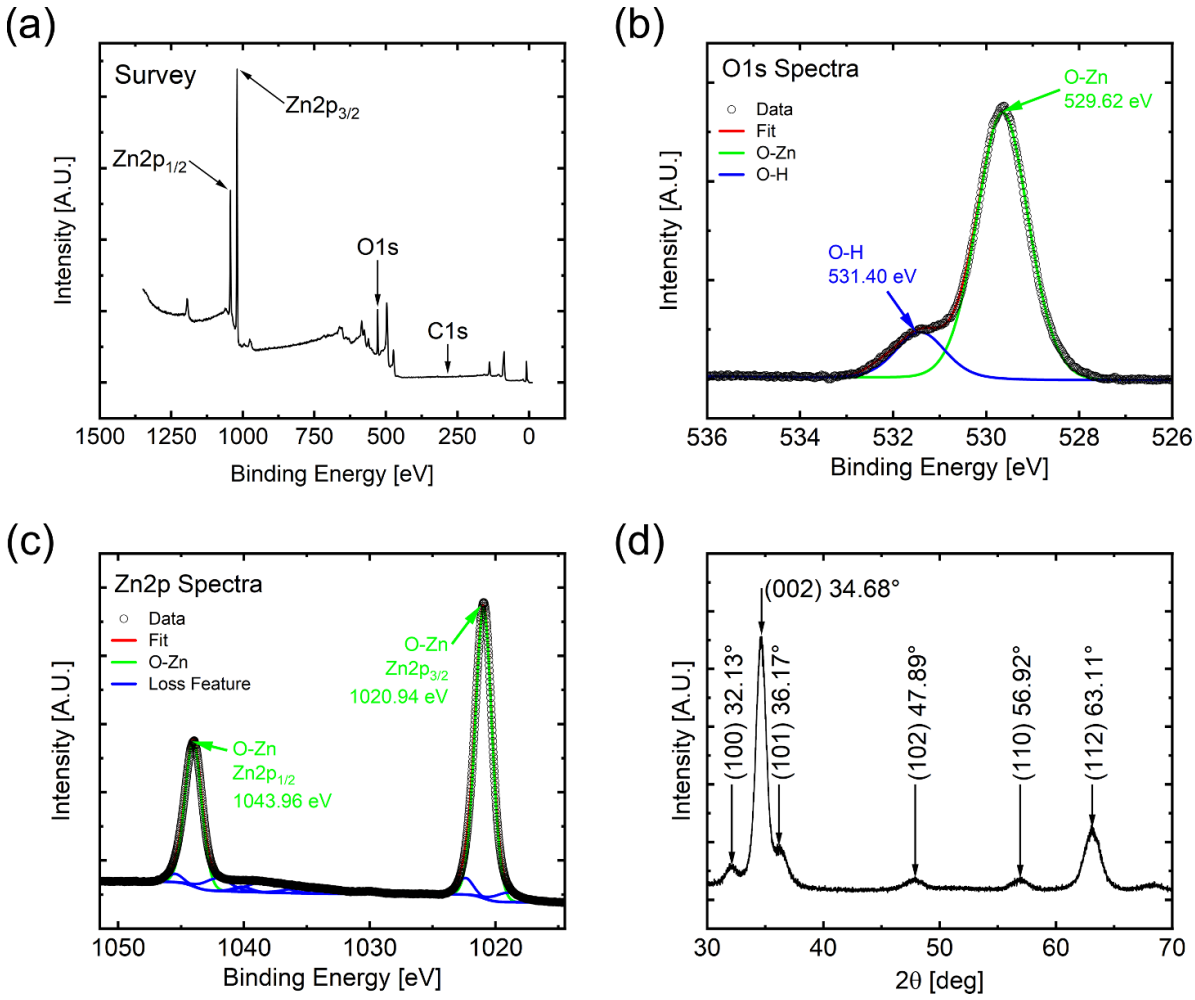

Figure 3. (a) XPS survey of as-deposited ZnO thin-film with peaks of interest labelled. (b) Core-level O1s XPS spectrum with de-convoluted peaks for O–Zn bond and O–H bond. (c) Zn2p XPS spectrum with de-convoluted peaks for O–Zn bond. (d) GI-XRD spectrum for as-deposited ZnO thin-film on Al_2O_3 with peaks assigned using JCPDS Card No. 79–0205.

is shown in figure 7(b). The rate of this trapping/de-trapping mechanism is modelled by the stretched-exponential function in equation (2) [64], and is used to fit the bias stress data in figure 6. The stretched-exponential model is given in equation (2), where ΔV_{th} is the threshold voltage shift as a function of time, $V_{\text{th}(\infty)}$ is the projected threshold voltage after an infinite time, t is the time elapsed from the application of fixed bias stress, τ is the characteristic trapping time of charge carriers, and β is the stretched-exponential fitting parameter. The stretched-exponential fittings are shown as solid lines in figure 6,

$$\Delta V_{\text{th}}(t) = V_{\text{th}(\infty)}\left[1 - \exp\left(-(t/\tau)^{\beta}\right)\right]. \tag{2}$$

The stretched-exponential function is fitted iteratively using the Levenberg–Marquardt algorithm for each dataset at a specific $V_{\text{GS(fixed)}}$. The extracted parameters of $V_{\text{th}(\infty)}$, τ, and β are plotted against $V_{\text{GS(fixed)}}$ in figures 8(a)–(c), respectively. All fitting for each value of $V_{\text{GS(fixed)}}$ use the same initial state for $V_{\text{th}(\infty)}$, τ, and β (0, 10^4, and 0.5, respectively).

The trend of $V_{\text{th}(\infty)}$ against $V_{\text{GS(fixed)}}$ is shown in figure 8(a). These data demonstrate that the degree of V_{th} shift is linearly correlated to the applied $V_{\text{GS(fixed)}}$ in this range of $V_{\text{GS(fixed)}}$. Furthermore, the sign of $V_{\text{GS(fixed)}}$ relates directly to the direction of V_{th} shift, whereby a positive $V_{\text{GS(fixed)}}$ leads to a V_{th} in the negative direction and a negative $V_{\text{GS(fixed)}}$ leads to a positive shift in V_{th}.

The relation between τ and $V_{\text{GS(fixed)}}$ in figure 8(b) is dependent on the use of PBS versus NBS. In the PBS regime, τ is consistent between 1800 s and 2900 s for $V_{\text{GS(fixed)}}$ between +5 V and +15 V. There is one outlier at +2 V, for which τ is 6800 s, likely due to a lower electron injection rate at this lower field strength. In contrast, in the NBS regime there is a significant reduction in τ from 1970 s at −2 V to 88 s at −15 V, indicating electron de-trapping time is dependent on the applied $V_{\text{GS(fixed)}}$. As $V_{\text{GS(fixed)}}$ becomes more negative the electron de-trapping time significantly reduces, due to increased Coulomb repulsion. The de-trapping process continues until an equilibrium point is reached for a particular $V_{\text{GS(fixed)}}$, and V_{th} plateaus at a stable, positively-shifted value, as evidenced in figure 6(c).

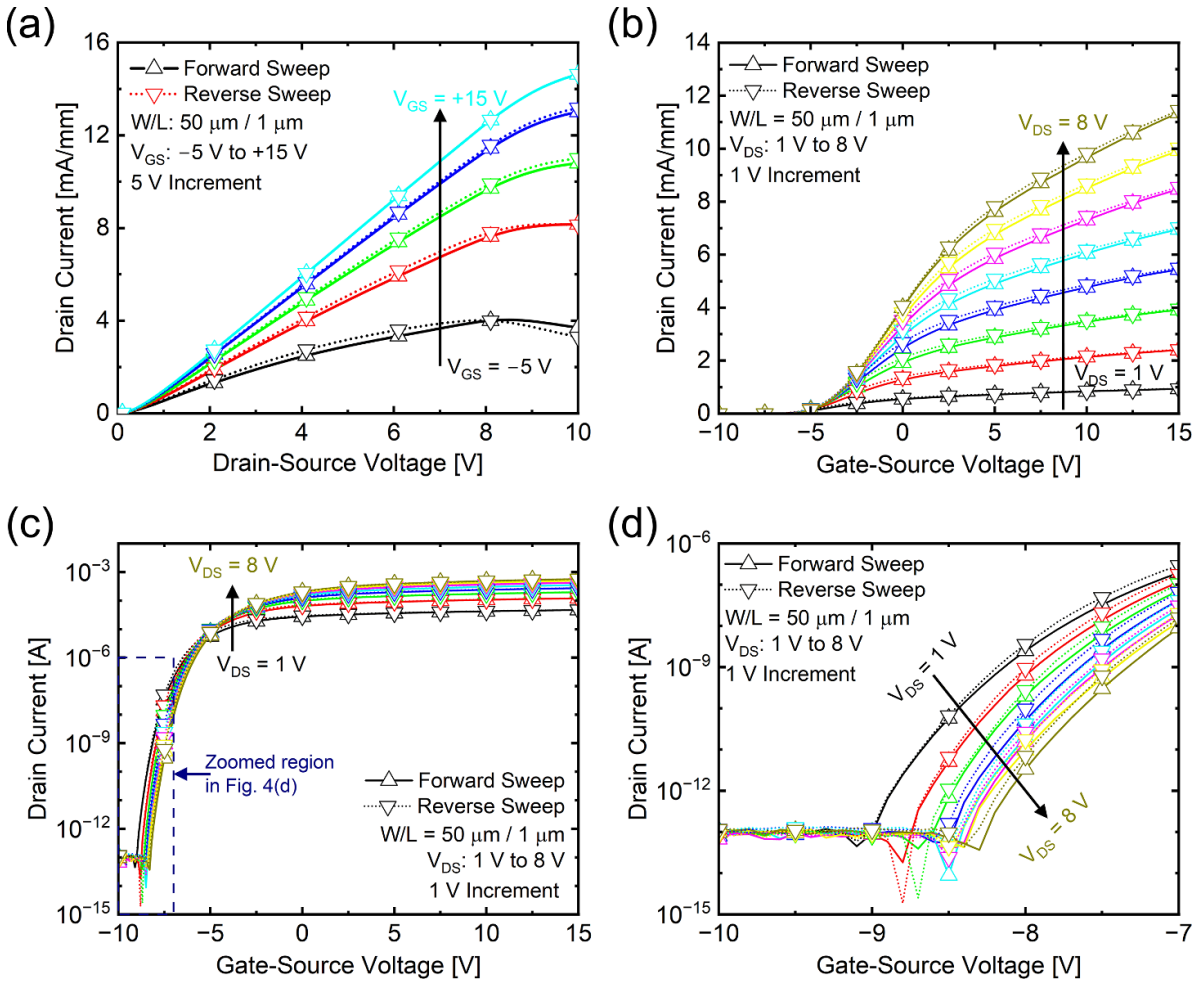

Figure 4. (a) I_D–V_{DS} characteristics of ZnO-TFTs with V_{GS} between −5 V and +15 V. (b) Linear plot of I_D–V_{GS} characteristics with V_{DS} between 1 V and 8 V. (c) Semi-logarithmic plot of I_D–V_{GS} characteristics with V_{DS} between 1 V and 8 V. (d) Zoomed-in view of the semi-logarithmic plot of I_D–V_{GS}, focusing on the sub-threshold region.

Table 1. Extracted values of threshold voltage, field-effect mobility, subthreshold swing, and on-/off-current ratio at $V_{DS} = 1$ V and $V_{DS} = 8$ V. $W/L = 50$ μm/1 μm.

Test Condition		V_{th} (V)	μ_{FE} (cm^2/(V·s))	*S.S.* (mV dec^{-1})	I_{on}/I_{off} (A/A)
$V_{DS} = 1$ V	Forward Sweep	−7.21	9.8	141	1.10×10^8
	Reverse Sweep	−7.32	10.5	147	8.32×10^7
$V_{DS} = 8$ V	Forward Sweep	−5.95	53.5	136	1.70×10^9
	Reverse Sweep	−6.02	56.4	158	1.42×10^9

The β fitting parameter is presented in figure 8(c) with a range between 0.31 and 0.59. With the exception of ±2 V, the greater the magnitude of $V_{GS(fixed)}$, the greater the value of β, although this is not a robust trend.

The fitting error is evaluated using the reduced chi-squared metric (χ^2), and coefficient of determination (R^2) goodness-of-fit tests. These tests are presented in figure 8(d) with χ^2 on the left axis, in black crosses, and R^2 on the right axis, in red circles. χ^2 is minimised during the fitting procedure, until the change in χ^2 between iterations is $< 10^{-9}$. R^2 measures the goodness of the fit, and is lower when there is a significant spread in the data, such as the plots for +12 V and +15 V in figure 6(a).

A comparison to recently reported works on bias stressing of TFTs using *n*-type metal–oxide semiconductors in table 3 demonstrates that the measured V_{th} shifts in this work are comparable to existing publications. Furthermore, fresh insights into ZnO-TFT behaviour are yielded by use of V_{GS}-dependent extraction of trapping/de-trapping time. The choice of V_{DS} varies markedly between different works, though can be broadly categorised as low V_{DS} (0.1 V to 1.0 V) and high V_{DS} (5.0 V to 20.0 V). This work primarily uses a fixed V_{DS}

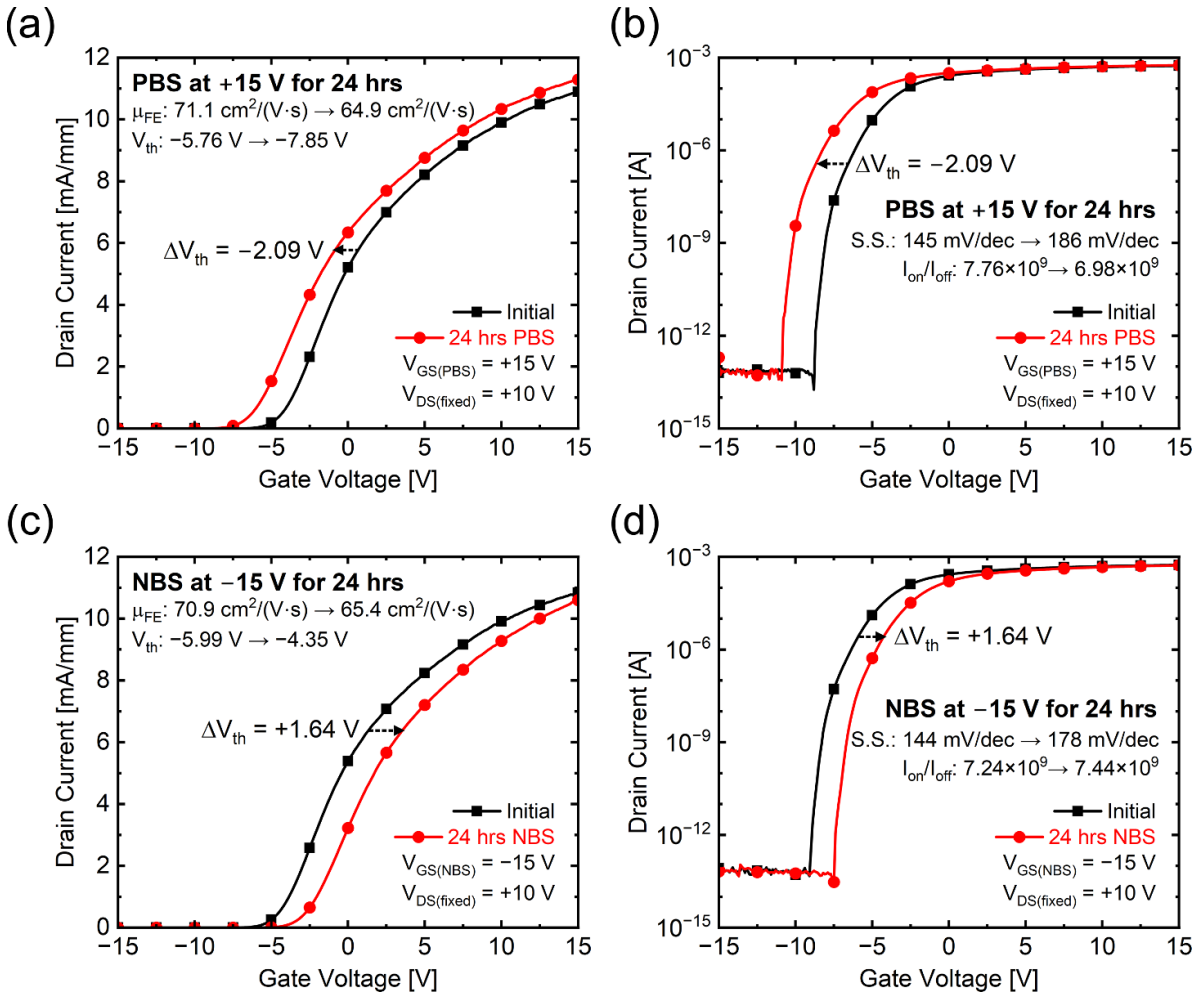

Figure 5. Transfer characteristics of ZnO-TFT ($W/L = 50\ \mu$m/1 μm), under positive and negative bias stress conditions. V_{DS} is 10 V for all plots. (a) Linear plot of I_D–V_{GS} before and after positive bias stress of +15 V for 24 h. (b) Semi-logarithmic plot of I_D–V_{GS} before and after positive bias stress of +15 V for 24 h. (c) Linear plot of I_D–V_{GS} before and after negative bias stress of −15 V for 24 h. (d) Semi-logarithmic plot of I_D–V_{GS} before and after negative bias stress of −15 V for 24 h.

Table 2. Values of threshold voltage, field-effect mobility, subthreshold swing, and on-/off-current ratio under PBS and NBS conditions for 24 h. V_{DS} is 10 V and $W/L = 50\ \mu$m/1 μm.

Test Condition		V_{th} (V)	ΔV_{th} (V)	μ_{FE} (cm^2/(V·s))	$S.S.$ (mV dec^{-1})	I_{on}/I_{off} (A/A)
PBS ($V_{GS(fixed)} = +15$ V)	Initial	−5.76	−2.09	71.1	144	7.76×10^9
	After 24 h	−7.85		64.9	186	6.98×10^9
NBS ($V_{GS(fixed)} = -15$ V)	Initial	−5.99	+1.64	70.9	145	7.24×10^9
	After 24 h	−4.35		65.4	178	7.44×10^9

of 10 V to emulate future 3D heterogeneous integration operation, placing it in the high V_{DS} category. The degree of V_{th} shift is comparable for similar $V_{GS(fixed)}$ and V_{DS}, however this work uses extended bias times compared to many works in bias stressing of metal oxide TFTs.

3.3. Endurance cycling

After making the DC and PBS/NBS I_D–V_{GS} measurements, endurance cycling measurements are made using 10^9 square-wave cycles between a V_{GS} of −15 V and +15 V, applied at 1 kHz. This voltage range switches the channel fully on and off. A snap-shot I_D measurement is performed every 2000 cycles, at $V_{GS} = 0$ V and $V_{DS} = 10$ V, yielding 500 000 total snap-shot I_D measurements, as a separate dataset to the 1000 I_D–V_{GS} plots. I_D–V_{GS} is measured every 10^6 cycles using the initial characterisation conditions ($V_{DS} = 10$ V, V_{GS} between −15 V and +15 V). A further 10^6 on-off cycles are applied and so this measurement procedure is repeated 1000 times, yielding 1000 I_D–V_{GS} graphs. The overall measurement procedure is summarised in the supplementary material. This set of 1000 I_D–V_{GS} plots are used to extract V_{th}, μ_{FE}, $S.S.$, and I_{on}/I_{off}

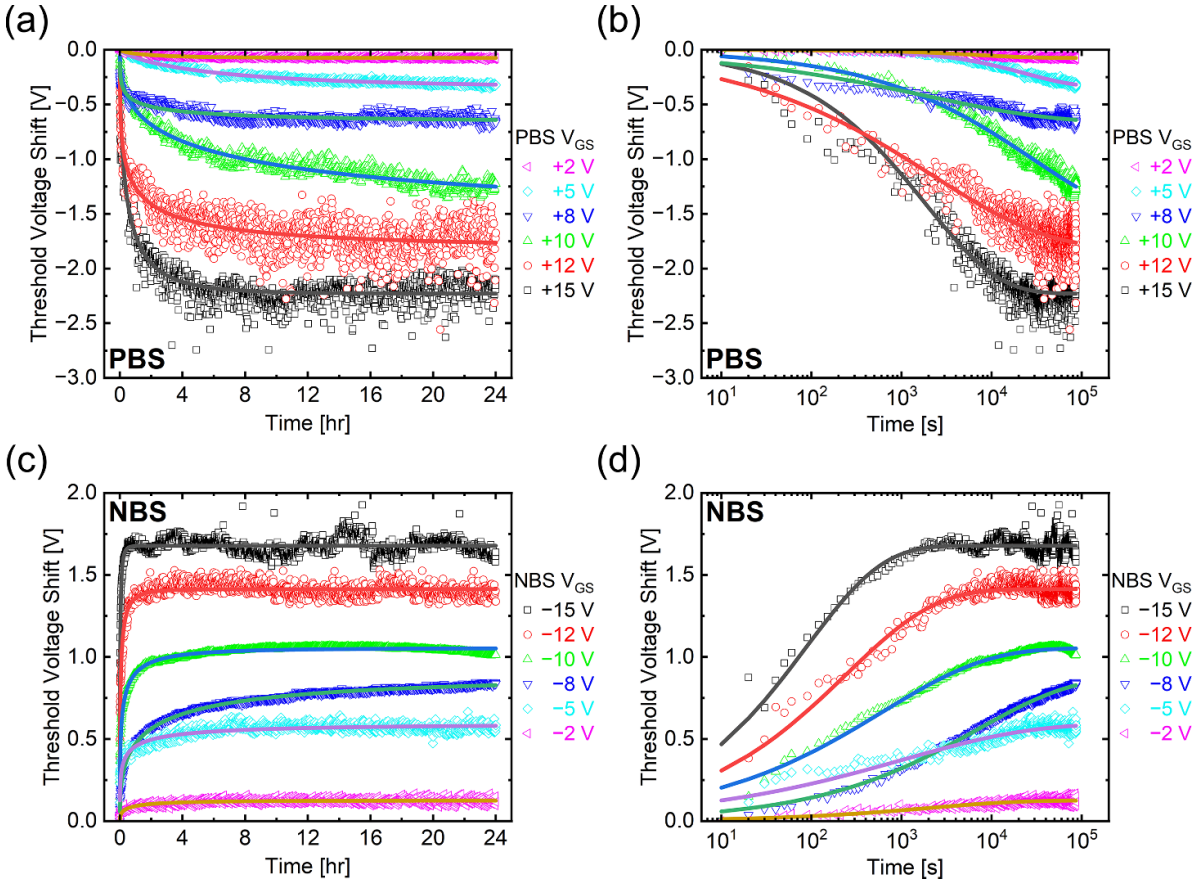

Figure 6. Threshold voltage against time with stretched-exponential fitting (solid line), (a) Linear V_{th}-time with a fixed V_{GS} positive-bias stress for 24 h. (b) Semi-logarithmic V_{th}-time with a fixed V_{GS} positive-bias stress for 24 h. (c) Linear V_{th}-time with a fixed V_{GS} negative-bias stress for 24 h. (d) Semi-logarithmic V_{th}-time with a fixed V_{GS} negative-bias stress for 24 h.

against the number of on-off cycles, enabling time-evolution and statistical analysis of TFT characteristics under endurance testing. The overall measurement time is 22 d.

Figure 9(a) presents the change in V_{th} against the number of on-off cycles. There is an overall positive shift in V_{th}, similar to the NBS trends in figure 6(c). The endurance cycling indicates a steep shift between 0 and 1×10^8 cycles, before levelling off and rising gradually for the remainder of the experiment. As V_{GS} input cycles are applied with 50% duty cycle, there is equal time at −15 V (NBS condition) and at +15 V (PBS condition). Therefore, the positive shift in V_{th} can be ascribed to the difference in characteristic trapping time of charge carriers under PBS versus NBS conditions, as noted in figure 8(b). Under the −15 V NBS condition the characteristic trapping time of charges into the insulator material is 88 s, as compared to a 1860 s de-trapping time with +15 V PBS, representing a factor of 21 difference in carrier trapping time. Across the endurance cycling test period, the faster NBS trapping mechanism dominates the PBS effect leading to a positive V_{th} shift that is similar to the NBS tests in figures 6(c) and (d). V_{th} hysteresis is shown as the blue plot on the right-axis with an initial counter-clockwise hysteresis pattern at −710 mV, which gradually shifts towards 0 mV at 5×10^8 cycles, before shifting to a clockwise hysteresis pattern and plateauing at +180 mV.

Figure 9(b) shows the change in μ_{FE} against the number of on-off cycles, measured both in the forward and reverse V_{GS} sweeps. Between 0 and around 4×10^8 cycles, μ_{FE} is stable around 47 cm2 $(V{\cdot}s)^{-1}$ and 56 cm2 $(V{\cdot}s)^{-1}$ in the forward and reverse directions, respectively. Then both forward and reverse directions increase gradually to a peak of 63 cm2 $(V{\cdot}s)^{-1}$ in the forward direction and 77 cm2 $(V{\cdot}s)^{-1}$ in the reverse direction at 8×10^8 cycles, before falling and stabilising to 53 $cm^2/(V{\cdot}s)$ and 64 $cm^2/(V{\cdot}s)$, respectively. The cause of this combined μ_{FE} shift over time is not immediately clear, however variations in temperature or humidity are a likely mechanism [65]. Hysteresis in μ_{FE} between the forward and reverse direction sweep is notable with values of μ_{FE} measured in the reverse direction being 19% greater than the forward direction. This disparity can be understood by assessing the role of grain boundaries in limiting carrier mobility. Grain boundaries in polycrystalline ZnO act as localised charge-traps in the channel, presenting double-Schottky potential barriers at each boundary [29, 66]. The barrier height is modulated by V_{GS}, as trapped charges at the grain boundaries are trapped and de-trapped. When V_{GS} is increased, the potential barrier height at each grain boundary decreases [29]. Correspondingly, when V_{GS} is reduced the potential barrier height at grain boundaries increases. The potential barrier height relates to the mean free path of charge carriers in the channel [29], with a greater

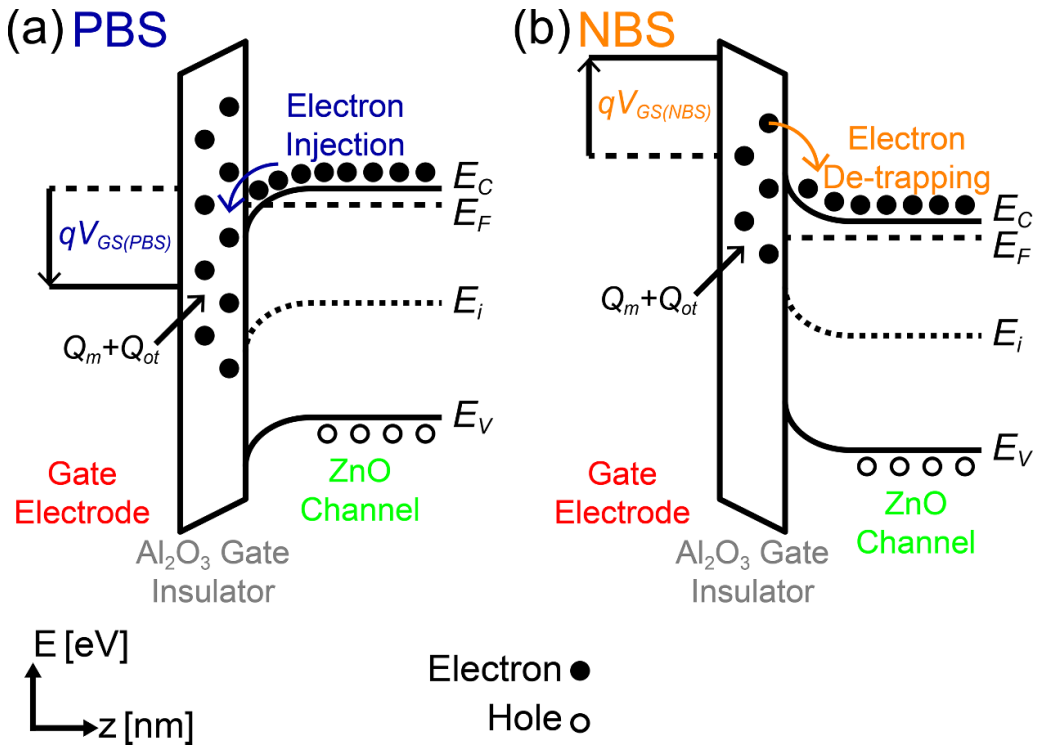

Figure 7. Band-energy diagrams of the threshold voltage shift mechanism with (a) positive bias stress inducing electron injection into the gate insulator and (b) negative bias stress leading to de-trapping of electrons from the gate insulator. Electrons that contribute to mobile (Q_m) and trapped oxide (Q_{ot}) charges in the gate insulator are labelled.

barrier height reducing the mean free path and carrier mobility, per Matthiessen's rule. Figure 9(c) illustrates the μ_{FE} hysteresis mechanism as a cycle of rising and lowering double-Schottky potential barriers in the conduction band (E_C) located at grain boundaries in the channel. When V_{GS} is at a minimum value the grain boundary potential barriers are at a maximum (figure 9(c)(i)). As V_{GS} increases for the forward sweep (in black), this potential barrier reduces as carriers are de-trapped (figure 9(c)(ii)), reaching minimum barrier height when V_{GS} is at a maximum value (figure 9(c)(iii)). Finally, as V_{GS} reduces back to the minimum value for the reverse sweep (in red), the potential barrier increases back to its maximum height (figure 9(c)(iv)). The observed mobility hysteresis is suggestive of a longer trapping than de-trapping time at double-Schottky potential barriers induced by grain boundary interfaces.

4. Conclusions

The long-term electrical characteristics of polycrystalline ZnO-TFTs fabricated by a low-temperature PE-ALD process have been examined using bias-stress and endurance cycling techniques. The as-fabricated ZnO-TFTs show reasonable TFT performance immediately after fabrication with a typical threshold voltage of −6.0 V, minimal hysteresis of −70 mV, mobility of 55 cm2 $(V{\cdot}s)^{-1}$, steep subthreshold swing of 136 mV dec^{-1}, and on-/off-current ratio of 1.70×10^9. Having established the baseline performance of the ZnO-TFTs, the long-term reliability and resilience are examined by use of PBS and NBS tests and endurance cycling. These results compare favourably to existing works on bias-stress in metal–oxide TFTs, with overall V_{th} shift of −2.09 in the PBS regime at +15 V and +1.64 in the NBS regime at −15 V. However, in this work ZnO-TFTs are studied using a greater range of voltages, with thorough analysis providing a critical insight into carrier dynamics in the channel material and trapping effects in the gate insulator. There is a notable discrepancy between the characteristic trapping and de-trapping time between PBS and NBS conditions, with a trapping time of 88 s using PBS and 1860 s using NBS. This phenomenon is further examined using endurance cycling measurements. Leveraging endurance cycling between −15 V and +15 V there is an overall V_{th} shift in the positive direction, similar to NBS conditions. The effect appears to arise from a factor of 21 difference between electron trapping and de-trapping time in the gate insulator. Furthermore, a mobility hysteresis effect is revealed using endurance cycling which is described by a grain boundary model for a polycrystalline ZnO channel under changing gate bias. The outcomes of this study point towards the need for a more thorough approach for metal–oxide TFT reliability analysis which is relevant for amorphous and polycrystalline TFTs. Charge carrier dynamics have been revealed which are critical for understanding the long-term behaviour of polycrystalline ZnO-TFTs for back-end-of-line heterogeneous integration applications.

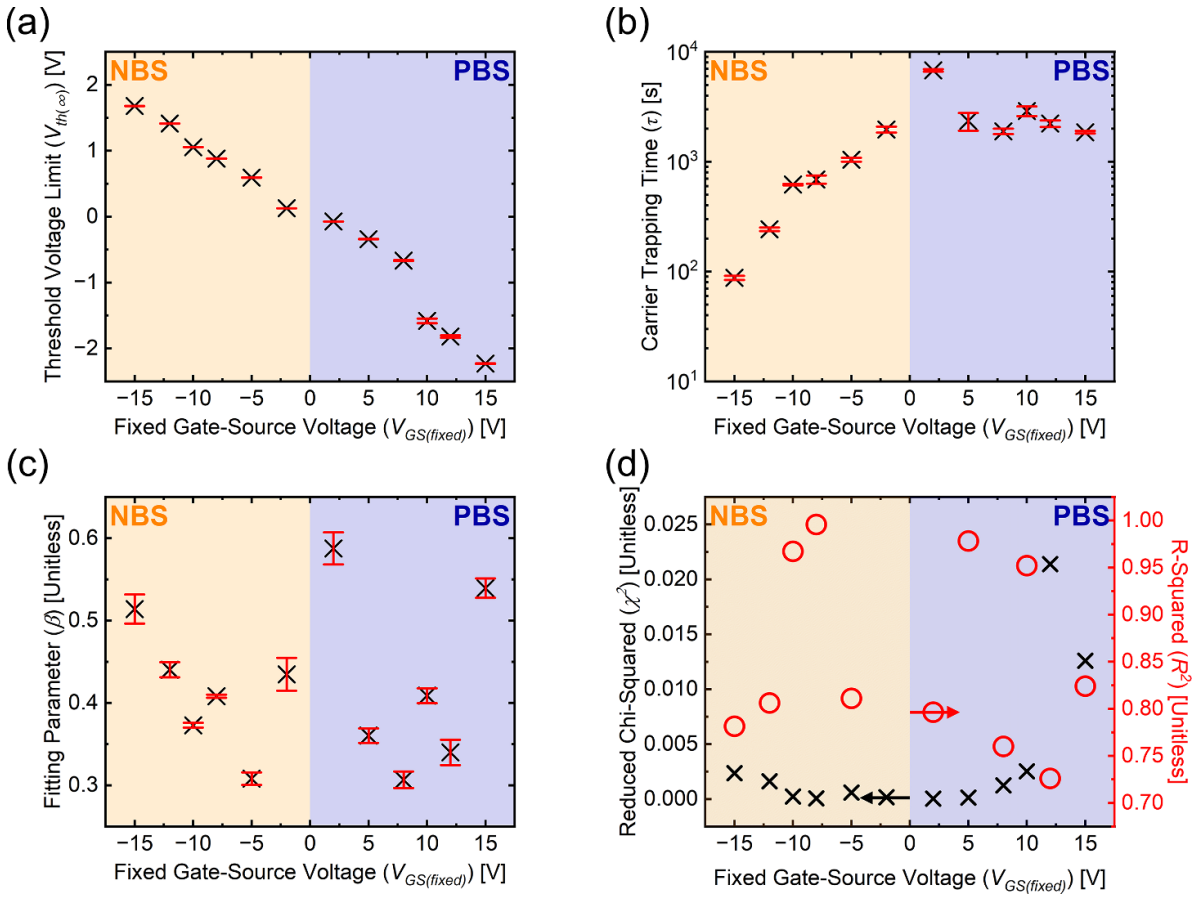

Figure 8. (a) Fitted value of V_{th} at infinite time against fixed V_{GS} under PBS and NBS conditions. (b) Characteristic trapping time of charge carriers against fixed V_{GS} under PBS and NBS conditions. (c) Stretched-exponential fitting parameter against fixed V_{GS} under PBS and NBS conditions. (d) Reduced chi-squared (χ^2) goodness-of-fit test against fixed V_{GS} (left axis in black), and coefficient of determination (R^2) goodness-of-fit test against fixed V_{GS} (right axis in red).

Table 3. Comparison of related works on *n*-type metal–oxide TFTs with bias stress testing.

Channel material	Gate bias stress [V]	Drain bias during PBS [V]	Duration [s]	V_{th} Shift [V]	References
Thermal ALD ZnO	+10	1.0	3600	+1.24	[42]
Sputtered a-IGZO	+20	20	30 000	−3	[43]
Sputtered a-IGZO	+30	7.0	30 000	−17	[43]
PE-ALD ZnO	+6	0.1	1800	+0.33	[44]
PE-ALD ZnO	−6	0.1	1800	+0.28	[44]
VLS ZnO	+9	0.5	4000	+6	[45]
ZnON (1:19 N:O)	+10	1.0	3600	+0.21	[46]
PE-ALD a-IGZO	+20	10	3600	+0.4	[47]
Thermal ALD AZO	+30	10	7200	+0.5	[48]
Thermal ALD AZO	−30	10	7200	−0.3	[48]
Thermal ALD ZnO	+20	0.1	3600	+1.24	[49]
Thermal ALD ZnO	−20	0.1	3600	−1.28	[49]
Sputtered a-IGZO	+7.5	0.1	300	+0.9	[50]
Sputtered ZnO	−20	0.1	1000	+2.52	[51]
Sputtered a-IGZO	+12	10	5000	−0.4	[52]
Sputtered a-IGZO	+40	1.0	3600	−3.2	[53]
PE-ALD ZnO	**+15**	**10**	**86 400**	**−2.09**	**This work**
PE-ALD ZnO	**−15**	**10**	**86 400**	**+1.64**	**This work**

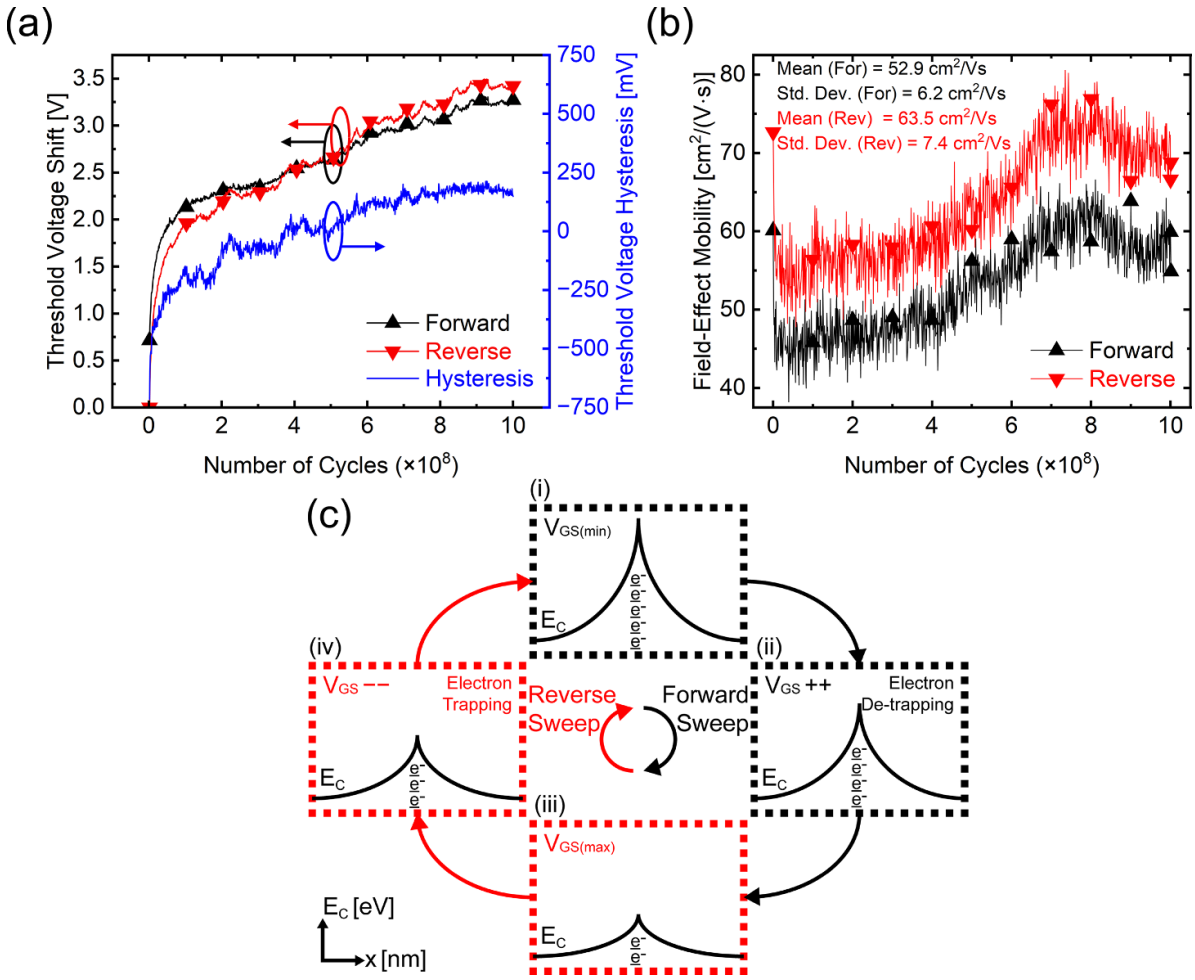

Figure 9. (a) Threshold voltage in forward and reverse sweep direction in black and red, respectively, against number of endurance cycles, measured every 10^6 cycles (left-axis).Threshold voltage hysteresis against number of endurance cycles in blue (right-axis). (b) Field-effect mobility against number of endurance cycles measured every 10^6 cycles. (c) Energy level diagram of conduction band, E_C, at double-Schottky grain boundary potential barriers in polycrystalline ZnO-TFTs. Electron (e^- trapping and de-trapping rates vary as gate bias (V_{GS}) is modulated.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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Conflict of interest

The authors declare no conflict of interest.

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