Energy Consumption in Micro and Nanoelectromechanical Relays

Qi Tang, Elliott Worsey, Mukesh K. Kulsreshath, Yue Fan, Yingying Li, Simon Bleiker, Harold Chong, Frank Niklaus and Dinesh Pamunuwa *Senior Member,IEEE*

***Abstract*— Electrostatically operated micro and nano electromechanical (MEM/NEM) relays have been proposed as digital switches to replace transistors due to their sharp turn-on/off transient, zero leakage current between drain and source in the off state, and capability to operate at far higher temperatures and radiation levels than CMOS. However, the different components associated with energy consumption in MEM/NEM relays, including the dynamic energy associated with charging the gate capacitance and static energy lost through substrate leakage, have not been investigated to date. Here, we present a detailed analysis of the energy consumption of NEM/MEM relays starting from first principles and compare against measurements carried out on silicon MEM relay prototypes. The dynamic energy consumed by a transistor in a binary switching transfer is accurately captured by $0.5CV^2$. This expression, which has also been used for relays, is only valid under the approximation of an unvarying capacitance C. However, the gate capacitance of a MEM/NEM relay varies as a function of the gate voltage, as it is determined by the airgap between the gate electrode and the moving beam. We show how including this effect adds an extra term to the dynamic energy consumption expression. Furthermore, we investigate different current leakage mechanisms and devise a new method to estimate the substrate leakage current based on utilising the switching hysteresis of relays. The models, analyses and measurement methodologies presented here constitute a set of essential techniques for accurate estimation of the energy consumption of MEM/NEM relays in ultra-low power circuit applications.**

***Index Terms*— Leakage energy, microelectromechanical, nanoelectromechanical, nanomechanical computing, relay, switching energy**

I. Introduction

Due to an abrupt turn-off transient, zero leakage current [1] and the ability to work at temperatures up to 300 °C [2], micro and nano-electromechanical (MEM/NEM) relays have the potential to replace transistors in applications that require high-temperature capability with ultra-low power consumption [2], [3], [4]. Such applications are common in the industrial IoT, aerospace, downhole and defence sectors for example. To date, many works have reported different modelling approaches to estimate the energy consumption of MEM/NEM relays, including finite-element model (FEM) simulations [5]–[7], reduced order modelling [8], [9], and numerical [10], analytical [11], [12] and circuit-level models [13], [14]. However, experimental verification of the energy consumption of electromechanical relays is essential to get a full understanding of the opportunities for potential power savings in relay-based circuits. Previously, we reported preliminary work carried out to experimentally extract the dynamic energy consumption of a MEM 3-T relay [15]. However, this work focused solely on dynamic energy without addressing static dissipation, which is critical for ultra-low power applications. We also derive a more accurate analytical model for dynamic energy consumption and provide many more details around the entire methodology.

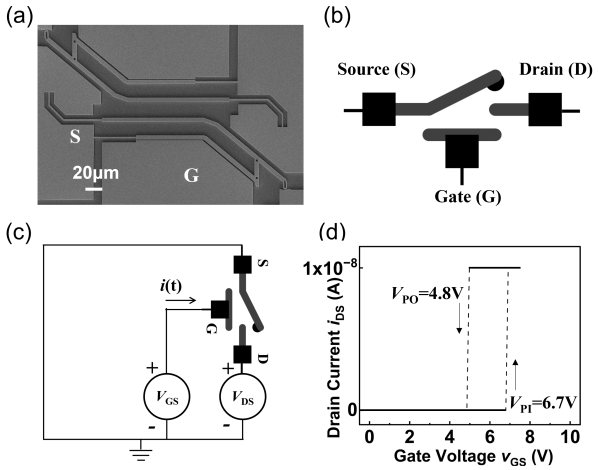

Fig. 1. Actuation of 3-T relay: (a) SEM images of the MEM 3-T Relay with movable dual beam. Voltages and currents are applied and measured at the source (S), drain (D) and gate (G) electrodes to measure the dynamic energy consumption. (b) Circuit symbol of 3-T relay with terminal definitions. (c) Equivalent circuit for actuation where the gate-source voltage V_{GS} is a ramp waveform and the drain is biased at a constant voltage V_{DS}. (d) Measured pull-in and pull-out of relay imaged in (a) showing the sharp turn-on and turn-off transients (relay dimensions correspond to the R1 design in Table I).

II. Relay Prototyping

In this paper we carry out a systematic analysis of the dynamic and static energy consumption of an electrostatically actuated three-terminal (3-T) relay, the closest equivalent to a MOSFET switch, based on experimental measurements. The conventional formulation of the dynamic energy consumption

This work was supported in part by the Royal Academy of Engineering Senior Research Chair Fellowship (RCSRF1920-9-53) awarded to Pamunuwa, the EU H2020 research and innovation programme (grant 871740 ZeroAMP) and the UK Research and Innovation (UKRI) under the Horizon Europe funding guarantee (grant 10063023 i-EDGE).

Authors Tang, Worsey, Kulsreshath, and Pamunuwa are with the School of Electrical, Electronic and Mechanical Engineering, University of Bristol. Authors Fan and Chong are with the School of Electronics and Computer Science, University of Southampton. Authors Li, Bleiker and Niklaus are with the Division of Micro and Nanosystems, Royal Institute of Technology (KTH). Corresponding author is Dinesh Pamunuwa (e-mail: dinesh.pamunuwa@bristol.ac.uk).

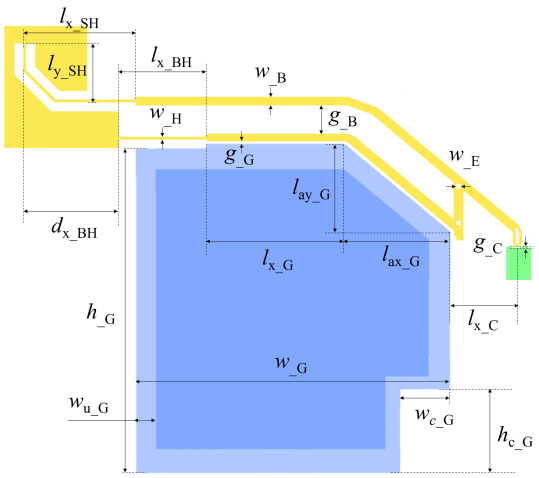

Fig. 2. Sketch of parameterised 3-T MEM relay layout for the two prototypes with key dimensions as symbols. The dimensions for the two relay designs R1 and R2 are given in Table I.

of a binary switching transfer where the output voltage swings from 0 to V is $\int v \cdot i\, dt = \int v \cdot d/dt(c \cdot v)dt$, which simplifies to $0.5CV^2$ for constant C [16]. However, the gate capacitance of a MEM relay varies as a function of the gate voltage, as the instantaneous capacitance is determined by the airgap between the gate electrode and the moving beam. In this work, using first principles, we derive an expression for the energy consumption that takes into account the changing capacitance. We also compute the dynamic energy consumption using current and voltage measurements on a 3-T MEM relay. The accuracy of measurements is verified by comparing extracted capacitance values against FEM simulations. Our results confirm that $0.5CV^2$ can significantly underestimate the dynamic energy consumption in MEM relays. Furthermore, we devised an experimental methodology to measure the static substrate leakage current of MEM relays fabricated on a silicon-on-insulator (SOI) substrate, which has not been considered to date, to provide insight into the efficacy of using MEM relays for ultra-low power applications.

A. Relay Design

We use a 3-T relay design that has an in-plane, angled dual-beam architecture as shown in Fig. 1(a) that we have successfully used in previous work to demonstrate switch cycling using nanocrystalline graphite coatings [17] and to demonstrate a 4-terminal relay with a single contact [18]. The 3-T relay can be depicted by the symbol defined in Fig. 1(b), and is actuated by applying a voltage v_{GS}[1] between the gate (G) and source (S) terminals that causes the movable cantilever to deflect due to the resulting electrostatic force and make contact with the drain (D) electrode. As per the equivalent circuit shown in Fig. 1(c), the current $i(t)$ charges the relay capacitance c_{R}, which is the capacitor defined by the beam (source) and gate acting as electrodes with air as the dielectric. The gate voltage v_{GS} eventually causes the beam to pull in at V_{PI}, defining the on state. Once on, a current i_{DS} flows between the source and drain terminals through the beam, due to the applied bias voltage between the drain and the source, V_{DS}. When the gate voltage is subsequently reduced, the hinges are designed to be stiff enough to overcome the surface adhesion forces at the contact and the beam pulls out at V_{PO}. We have characterised two different relay designs with this same architecture, and the key dimensions of each design are defined in Fig. 2 while the parameters for the two different prototypes as well as the experiment carried out on each are given in Table I. The measured pull-in and pull-out electrical performance for the MEM relay prototype (R1 in Table I) shown in Fig. 1(a) is given in Fig. 1(d).

[1]Our notation uses lowercase and uppercase letters respectively to denote variable and constant parameters, uppercase subscripts to denote terminals such as 'G' for gate, and lowercase subscripts for all other qualifiers such as 'st' for static.

TABLE I
PARAMETERS OF 3-T MEM RELAYS AND GATE ELECTRODE

Devices	**Relay (R1)**	**Relay with Wide Hinge and Gap (R2)**
Experiment	**Dynamic Energy Consumption**	**Static Energy Consumption**
Inner Structure Parameter		
Thickness (SOI substrate device layer thickness) (t)	2 μm	2 μm
Gate airgap (g_G)	0.6 μm	1.6 μm
Contact airgap (g_C)	0.5 μm	1 μm
Hinge width (w_H)	1.8 μm	2.5 μm
Beam width (w_B)	5 μm	5 μm
Dual beams gap (w_B)	15.8 μm	15.8 μm
Etching hole width (w_B)	2.3 μm	2.3 μm
Source beam hinge horizontal length (Lx_{SH})	65 μm	65 μm
Source beam hinge vertical length (Ly_{SH})	34 μm	34 μm
Body beam hinge length (Lx_{BH})	50 μm	50 μm
Beam hinge anchor displacement (dx_{BH})	60 μm	60 μm
Gate flat length (lx_G)	80 μm	80 μm
Gate Electrode Parameter		
Electrode width (w_G)	178.4 μm	
Electrode height (h_G)	187 μm	
Angled height (l_{ay_G})	50 μm	
Angled width (l_{aX_G})	62 μm	
Corner height (h_{c_G})	47.5 μm	
Corner width (w_{c_G})	28.3 μm	
Undercut width after VHF (w_{u_G})	5 μm	

B. Fabrication Process

The MEM relays R1 and R2 were patterned on SOI substrates with a $2\,\mu\mathrm{m}$ thick doped device layer (resistivity $0.02\,\Omega\,\mathrm{cm}$) and a $1\,\mu\mathrm{m}$ thick buried oxide (BOX) layer. A $210\,\mathrm{nm}$ thick SiO_2 layer was deposited as a hard mask using plasma-enhanced chemical vapor deposition (PECVD). The

in-plane switches were defined on the silicon device layer of the SOI substrates by carrying out electron-beam lithography (EBL) on a RAITH VOYAGER system. Next, the hard mask was patterned using reactive ion etching (RIE), and the silicon device layer was etched using inductively coupled plasma (ICP) on an Oxford Instruments Cobra 100 system. Subsequently, the cantilever structures were released by etching the BOX layer with HF vapor at $50\,^{\circ}\mathrm{C}$. A gold layer of 40 to $50\,\mathrm{nm}$ was thermally evaporated on the top of the MEM relays and the sidewalls of the suspended switch as a contact material.

III. Measurement Methodology

A. Energy Consumption of MEM Relay

The dynamic energy consumption of a MEM relay, E_{dy}, is the energy required to charge the relay's gate capacitance to the pull-in voltage, and is given by

$$E_{\mathrm{dy}} = \int_0^T v(t) \cdot i(t)\, dt. \tag{1}$$

For constant C this equation has a simple closed-form solution of $0.5CV^2$, but for the case of a MEM relay, the beam moves closer to the gate under actuation, the dielectric thickness reduces and the relay capacitance increases. The dynamic energy consumption can be accurately calculated by integrating the product of the measured capacitor charging current and the applied voltage over the actuation period T.

The static energy consumption of a MEM relay, E_{st}, caused by leakage currents, has two main components: drain-source leakage and gate leakage, similar to transistors. For our fabricated MEM relays, the current draw at the drain and source terminals before turn on has been observed to be at the noise level of our measurement system, while the turn-on and turn-off transients are as near vertical as can be ascertained. Thus, drain-source leakage is as near zero as is possible to measure. To measure gate leakage, which is difficult to directly monitor due to the very small gate capacitances present in micro scale relays, we utilise the hysteresis between the pull-in and pull-out voltages. After pull-in, the gate voltage is disconnected and the time for the relay to pull out is measured, from which the leakage current can be calculated using the fundamental expression in (2), as the initial voltage is known, the pull-out voltage can be measured by monitoring the drain current, and the gate capacitance can be estimated from finite-element simulations as well as measurements (see section III-C).

$$i = \frac{dQ}{dt} = \frac{d}{dt}\left[c(t) \cdot v(t)\right] \tag{2}$$

B. Measurement Setup

For measuring the relevant parameters of our MEM relays, we used a probe station with six triax channels connected to Keithley 2636B and 2606B source measure units (SMU) for voltage and current provision and monitoring. All measurements were carried out at room temperature under ambient atmosphere. In the experiments the gate voltage is increased linearly as a ramp until it reaches a given maximum, and then maintained at that value for a further period, while the current is logged. The drain is biased at a constant voltage, while the current is logged and monitored for a step change to signify turn on and turn off. To minimise power line-induced AC noise, the number of power line cycles (NPLC) over which the signal is integrated in the instrument for a single measurement was set to 25 [19].

C. Measurement Accuracy Verification

The SMUs have an inherent noise floor for current measurement that is a function of the transient characteristics of the voltage waveform and data logging frequency; the more time the instrument is given to stabilise at a given voltage, the more accurate the measurement. Our use of an NPLC setting of 25, which is the maximum for the instrument, ensures the lowest noise floor, albeit at the cost of a relatively slow ramp rate. For the setup we use, the noise floor is of the order of $0.2\,\mathrm{pA}$.

Additionally, the parasitic capacitors introduced by the measurement system and the SOI wafer have a significant effect. To quantify these effects, first, the current for a given voltage transient for a floating probe was logged, representing the current I_{SMU} drawn by the parasitic capacitance of the measurement system (SMUs and probe station). Second, the probe was connected to a floating pad of the same size as in the relay prototypes to measure the current I_{Ref} drawn to charge the parasitic capacitance of the electrode. Both currents, logged for an identical voltage ramp as used to drive the relays when measuring the dynamic energy, are shown in Fig. 3.

These reference measurements can be compared with theoretical calculations to provide a baseline measure of accuracy. The two currents can be modeled as:

$$I_{\mathrm{SMU}} = \frac{d\left[C_{\mathrm{SMU}} \cdot v_{\mathrm{G}}(t)\right]}{dt} \tag{3}$$

$$I_{\mathrm{Ref}} = \frac{d\left[(C_{\mathrm{SMU}} + C_{\mathrm{Sub}}) \cdot v_{\mathrm{G}}(t)\right]}{dt} \tag{4}$$

Here, $v_{\mathrm{G}}(t)$ is the gate voltage at time t, and C_{SMU} is a constant representing the parasitic capacitance of the measurement system, contributed by the SMU output drive circuits, cables and probes of the probe station. The gate electrode pad and interconnect tracks patterned on the Si device layer and the grounded substrate separated by the BOX layer define a parasitic capacitance structure that can be treated as a constant capacitor C_{sub} (see Table II). Both currents in Fig. 3, I_{SMU} and

TABLE II
CAPACITOR DEFINITIONS

Capacitance	Description
c_{R}	Relay capacitance defined by the gate and beam with air as dielectric; varies as a function of beam deflection.
C_{sub}	Pad capacitance defined by the pad on the device silicon layer and handle substrate with the BOX as dielectric; constant for a given pad geometry.
C_{SMU}	Parasitic capacitance introduced by the SMU, cables and probe station; constant.
C_{G}	Total capacitance seen at the gate electrode comprising C_{sub}, C_{SMU} and c_{R}; approximated as constant given that $C_{\mathrm{sub}} + C_{\mathrm{SMU}} >> c_{\mathrm{R}}$.

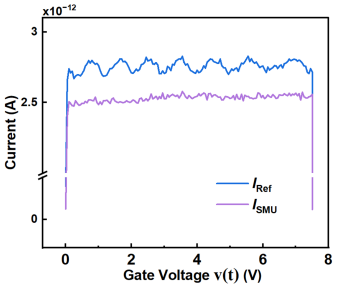

Fig. 3. Currents drawn when driving a pad connected to an interconnect track without a device (I_{G_Ref}), and when the probe pin is left floating without connecting to a pad, (I_{SMU}). The measurement setup used was identical to that used for probing the device.

I_{Ref}, have a sharp increase at the start of the voltage ramping process, indicative of the onrush of current drawn by the initially uncharged parasitic capacitors. Afterwards, the cyclical variation of the current seen can be explained by the fact that the SMU drive stage establishes a ramp waveform through a series of small increments followed by short stabilising periods where the voltage remains approximately constant, rather than an ideal linear increase. Finally, as the voltage reaches its maximum value and remains constant, both charging currents sharply decrease to the noise floor due to dv_G/dt becoming zero.

As I_{Ref} charges both C_{sub} and C_{SMU} (see Table II for definition), which are in parallel, from equations (3) and (4), the total capacitance of the gate electrode C_{Sub} of our MEM relay designs can be calculated as:

$$C_{Sub} = C_{Ref} - C_{SMU} = \frac{\int I_{Ref} dt - \int I_{SMU} dt}{V_{MAX}} = 8.70 \times 10^{-13}\,\mathrm{F}. \tag{5}$$

where the integration in (5) of the two measured currents (shown in Fig. 3) has been performed using a Matlab script. The value of the capacitance defined by the stack formed by the gate electrode pad, BOX layer, and Si substrate can also be calculated theoretically as:

$$\begin{aligned} A_G &= w_G h_G - w_{c\_G} h_{c\_G} - \frac{1}{2} l_{ax\_G} l_{ay\_G} \\ A_S &= 2w_{u\_G}(w_G + h_G) - 4w_{u\_G} \\ C_{Sub\_T} &= \frac{\epsilon_{SiO2}(A_G - A_S) + \epsilon_{air} A_S}{t_{BOX}} = 8.69 \times 10^{-13}\,\mathrm{F}. \end{aligned} \tag{6}$$

where ϵ_{air} =8.854 × 10^{-12} F/m and ϵ_{SiO_2} =3.543 × 10^{-11} F/m are the permittivity values, and A_G =2.98 × 10^{-8} m^2 and A_S = 3.65 × 10^{-9} m^2 are the gate electrode area and undercut area caused by the vapor phase HF etch performed to suspend the beams. Finally, t_{BOX} =1 µm is the BOX layer thickness. The close match between the measured and theoretical values provide validation of our methodology.

IV. Experimental Results

A. Dynamic Energy Consumption

The dynamic energy is measured by recording the voltage across the gate capacitance and the current drawn to charge it over an actuation cycle for relay R1 (shown in Fig. 1(a)), and

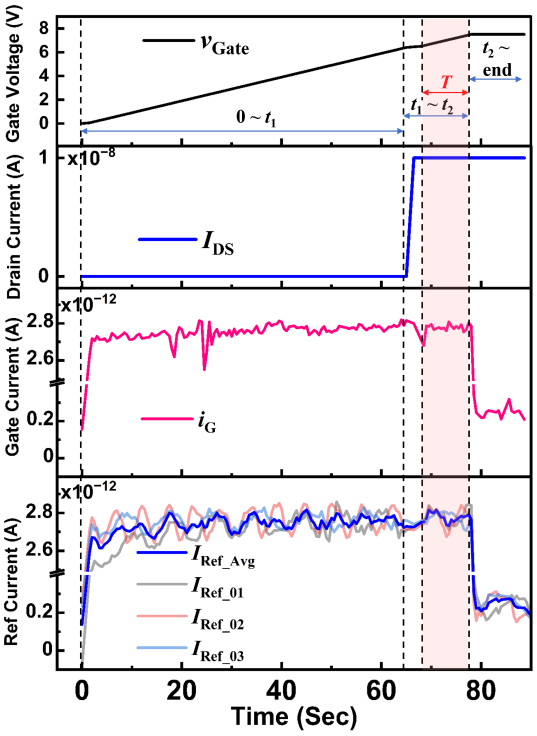

Fig. 4. (a) Applied gate voltage V_{GS}, measured gate current I_G, substrate capacitance charging current I_{G_Ref} and total current drawn by gate electrode i_G, for a single actuation cycle.

performing the integral specified in equation (1). The applied actuation signal, gate voltage v_G, comprised a ramp voltage as shown in Fig. 4. The pull-in event is shown by the sharp increase in drain current i_{DS}. The measured gate current i_G represents the current drawn by the total gate capacitance c_G including the relay capacitance c_R and parasitic capacitance comprising the gate electrode pad capacitance C_{sub} and the total capacitance of the measurement system C_{SMU}:

$$\begin{aligned} i_G(t) &= \frac{d}{dt}\left[(C_{SMU} + C_{Sub} + c_R(t)) \cdot v_G(t)\right] \\ &= I_{ref} + \frac{d}{dt}\left[(c_R(t)) v_G(t)\right] \end{aligned} \tag{7}$$

The switching of the relay can be separated into three phases, (1) $0 \le t \le\ t_1$, (2) $t_1 \le t \le\ t_2$, and (3) $t > t_2$ where t_1 and t_2 are the times taken for the gate voltage to reach the pull-in voltage V_{PI} and the maximum value V_M, which represents the gate overdrive. In the first phase, where $0 \le t \le\ t_1$, the beam deflects towards the gate with increasing gate voltage with pull-in occurring at V_{PI} =6.4 V. As the beam deflects, the beam-to-gate airgap decreases and the relay capacitance increases. At the beginning of phase 2, where $t_1 \le t \le\ t_2$, the beam of the 3-T relay makes contact with the drain electrode after pull in. Thereafter, the beam behaves mechanically as a beam that's fixed at both ends, and the relay capacitance can be approximated as constant due to the relatively small beam deflection that occurs as v_G increases from V_{PI} to V_M. Therefore, in this phase, the gate current i_G charges three constant capacitors, comprising the parasitic capacitances presented by the SMU and SOI substrate, and the maximum

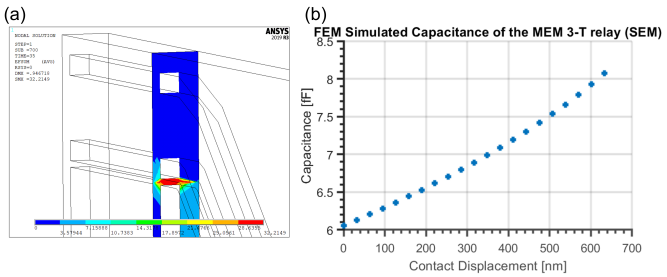

Fig. 5. Results from FEM simulation of relay R1: (a) the field distribution across the gate and beam, showing the concentration in the actuation air gap and fringing components. (b) The gate-to-beam capacitance as a function of the beam tip position for dimensions extracted from the SEM of the fabricated relay. The closed position corresponds to a contact displacement (i.e. airgap between the beam tip and gate) of $650\,\mathrm{nm}$, and a gate-to-beam capacitance of $8.2\,\mathrm{fF}$.

capacitance of the relay C_R in the closed state. It can be seen that after pull in, the voltage between the gate and beam v_G has a distinctly different ramp rate for a short period, until $t = t_2 - T$. We believe this is caused by the beam voltage changing from $0\,\mathrm{V}$ (due to the grounding at the source end) before pull in, to a voltage distribution determined by the bias voltage at the drain ($5\,\mathrm{V}$) and the on resistance R_on of the beam (comprising tip contact resistance of $\approx 10^5\,\Omega$ and silicon beam resistance of $\approx 10^3\,\Omega$) after pull in. This, in turn, causes a sudden change in the impedance seen by the instrument at the gate. Once the transient effects of this have died down, the ramp rate stabilises. Therefore, we use the period T, shown in Fig. 4, to estimate the closed-state relay capacitance as:

$$\begin{aligned} C_\mathrm{R} &= C_\mathrm{G} - C_\mathrm{Ref} \\ &= \frac{\int^T i_\mathrm{G} dt - \int^T I_\mathrm{Ref\_Avg} dt}{\Delta V_\mathrm{T}} = 9.73\,\mathrm{fF}. \end{aligned} \tag{8}$$

We carried out an FEM simulation of the actuation of relay R1, based on dimensions extracted from the SEM, shown in Fig. 1(a). Fig. 5(a) shows the electric field distribution in a slice orthogonal to the beams, showing its concentration in the actuation air gap, and the fringing around the outside. The capacitance of the relay has been extracted as a function of the tip displacement, and is $8.2\,\mathrm{fF}$ in the closed state. Thus, the measured value of $9.73\,\mathrm{fF}$ varies from the FEM extracted value by 18.6%, likely due to disregarding beam deflection and the resulting capacitance change due to gate overdrive, as well as measurement limitations. Nevertheless, the values are close enough to provide confidence in our measurement methodology.

Now, the dynamic energy consumption of the relay can be calculated based on measurements by using the relation (1):

$$\begin{aligned} E_\mathrm{dy} &= \int_0^{t_1} v_\mathrm{G}(t) i_\mathrm{G}(t) dt - \int_0^{t_1} v_\mathrm{G}(t) I_\mathrm{Ref}(t) dt \\ &= \frac{V_\mathrm{PI}}{2} \int_0^{t_1} \frac{d}{dt} \left[c_\mathrm{R}(t) \cdot v_\mathrm{G}(t) \right] dt \\ &= \frac{V_\mathrm{PI}}{2} \int_0^{t_1} \frac{dQ_\mathrm{R}(t)}{dt} dt = 2.59 \times 10^{-13}\,\mathrm{J}. \end{aligned} \tag{9}$$

For an analytical formulation, the expression for E_dy in eq.

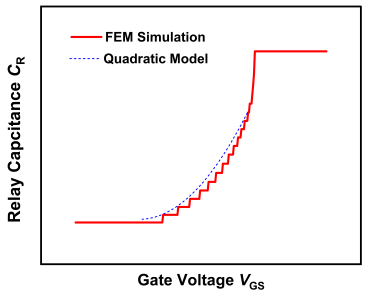

Fig. 6. Variation of the relay capacitance c_R as a function of the gate voltage V_GS extracted from ANSYS FEM simulations and quadratic model result for relay R1.

(1) can be combined with eq. (2) to yield

$$\begin{aligned} E_\mathrm{dy} &= \int_0^T v(t) \frac{d}{dt} \left[c(t) \cdot v(t) \right] dt \\ &= \int_0^T v(t) \left[c(t) \frac{dv(t)}{dt} + v(t) \frac{dc(t)}{dt} \right] dt \\ &= \int_0^{V_\mathrm{pi}} v \cdot c\, dv + \int_{C_\mathrm{R\_o}}^{C_\mathrm{R\_o}} v^2 dc \end{aligned} \tag{10}$$

In order to perform this integration, the capacitance c needs to be defined as a function of voltage v. The variation of the capacitance c_R with gate voltage V_GS for relay R1 is shown in Fig. 6. These values have been extracted from FEM simulations carried out in ANSYS and shows classic pull-in behaviour. The capacitance curve can be closely approximated by a quadratic function of the gate voltage, fitted using the capacitance and voltage values at the open state, closed state, and midpoint of the capacitance as boundary conditions (see Fig. 6):

$$c_\mathrm{R} = C_\mathrm{R\_o} + \frac{\lambda (C_\mathrm{R\_c} - C_\mathrm{R\_o})}{V_\mathrm{PI}} V + \frac{(1-\lambda)(C_\mathrm{R\_c} - C_\mathrm{R\_o})}{V_\mathrm{PI}^2} V^2. \tag{11}$$

Here, λ is a constant related to the voltage ratio n between the gate voltage corresponding to the midpoint capacitance $\frac{C_\mathrm{R\_c} + C_\mathrm{R\_o}}{2}$ and the pull-in voltage V_pi. The value of λ can be expressed in terms of n as $\lambda = \frac{2n^2-1}{2n^2-2n}$.

By substituting eq. (11) in eq. (10), an analytic expression can be obtained for the dynamic energy consumption under the assumption of a quadratic variation of the relay capacitance with gate voltage:

$$\begin{aligned} E_\mathrm{dy} = 1/2 C_\mathrm{R\_o} V_\mathrm{pi}^2 + 2/3 \lambda (C_\mathrm{R\_c} - C_\mathrm{R\_o}) V_\mathrm{pi}^2 \\ + 3/4 (1-\lambda)(C_\mathrm{R\_c} - C_\mathrm{R\_o}) V_\mathrm{pi}^2. \end{aligned} \tag{12}$$

In our previous work [15] we used a linear assumption for the capacitance, which can be obtained by setting $\lambda = 1$ in eq. (12), when the dynamic energy expression simplifies to

$$E_\mathrm{dy} = 1/2 C_\mathrm{R\_o} V_\mathrm{pi}^2 + 2/3 (C_\mathrm{R\_c} - C_\mathrm{R\_o}) V_\mathrm{pi}^2. \tag{13}$$

The relation in (12) yields a dynamic energy consumption of $2.10 \times 10^{-13}\,\mathrm{J}$, which is a 19% deviation from the measured value in our fabricated MEM relay, an improvement over the value of $1.80 \times 10^{-13}\,\mathrm{J}$ produced by the linear assumption [15]. Under the assumption of a constant capacitance

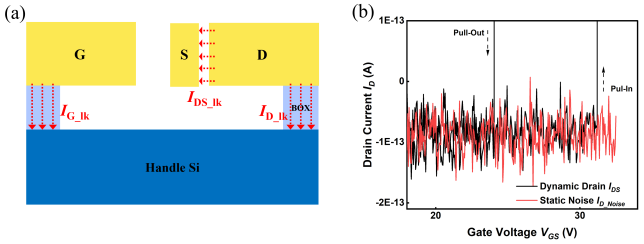

Fig. 7. (a) Possible leakage current mechanisms in a 3-T relay: source-drain leakage I_{DS_lk}, and leakage to substrate at gate I_{G_lk} and drain I_{G_lk} electrodes. (b) Measured drain current I_{DS} as a function of applied gate voltage V_{GS} for a single switching cycle. The turn-on and turn-off transients are as near vertical as can be measured, while the current before pull in and after pull out is indistinguishable from the noise floor.

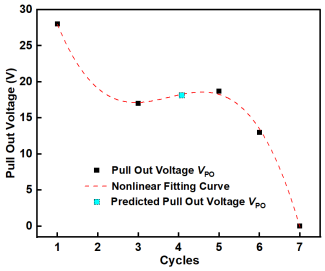

Fig. 8. Pull out points V_{PO} of relay R2 for consecutive switching cycles. Measurements in black, pull-out for cycle 4 is estimated by curve fitting.

$C_{R\_o} = C_{R\_c}$ the expression (12) simplifies to $0.5CV^2$. The use of a single representative value, for example the average of the open-state and measured closed-state capacitance C_{R_avg} =7.9 fF, gives a value of 1.62×10^{-13} J, which is 37% lower than the actual energy consumption for the particular actuation waveform used here. In general, the energy consumption is a function of the open-state and closed-state capacitance values, in turn determined by the relay design, especially the actuation and contact airgaps (our previous work gives details of the effects of the relay geometry on the electromechanical behaviour of the relay architecture used in this work [18]). The quadratic model for the relay capacitance provides a simple and accurate means of including the effect of the changing capacitance, and provides valuable insight. For example, the dynamic energy consumption of a MEM relay can be reduced by minimising the difference between the open-state and closed-state capacitances, which can in turn be accomplished by making the contact airgap smaller than the actuation (gate) airgap, so that the beam tip makes contact before it traverses the full length of the gate airgap.

B. Static Energy Dissipation

The static energy dissipation E_{st} of a MEM relay is defined as the energy consumed outside the switching transient, which can be due to a combination of leakage current at the drain and gate as sketched in Fig. 7(a). For MEM relays, the leakage current i_{DS_lk} between drain and source in the off state is zero due to the physical air gap between the tip of the beam and the drain. Furthermore, the slope of the drain current turnoff transient is only limited by tunneling currents which occur within very small air gaps [11], compared to the 60 mV per decade subthreshold slope in CMOS. The sharp turn-on/off transient is evident in the *I-V* plot shown in Fig. 7(b). Insofar as possible to determine within the capability of our measurement equipment, both turn-on and turn-off transients appear vertical. Fig. 7(b) shows i_{DS} during the switching process (when v_{GS} is applied) and the noise current i_{DS_n} without an actuation voltage and only the bias voltage V_{DS} applied. As evident, i_{DS} before pull-in and after pull-out is indistinguishable from i_{DS_n}.

The second potential source of static energy dissipation is leakage currents to the substrate from electrodes that are biased at non-zero voltages. All pads (gate, drain and source) form parasitic capacitors defined by the Si device layer and the handle substrate with the BOX acting as a dielectric. The pad size and characteristics of the SOI substrate determine this type of static energy consumption, including the dopant concentration in the Si device and Si handle layers, and the thickness and quality of the BOX layer. Due to the very small currents involved, direct measurement is impractical. Therefore, we characterized leakage from the gate electrode by utilising the hysteresis window between pull-in and pull-out (the pull-out voltage V_{PO} is always lower than the pull-in voltage V_{PI}, due to the surface adhesion forces at the contact and differences in the closed-state and open-state beam-to-gate air gaps [4]). After initially actuating the relay by grounding the source and driving the gate, the gate electrode was electrically floated, and the time taken for the relay tip to disengage from the drain was recorded (a similar methodology has been used for MEMs energy harvesters [20], [21]). The average gate-to-substrate leakage current i_{GS_lk} can be calculated as

$$I_{G\_lk} = C_{Sub}\frac{V_{PI} - V_{po}}{t_{PO}} = 1.16 \times 10^{-15}\,\text{A} \qquad (14)$$

This experiment was carried out using relay R2 (see Table I). While the relay consistently pulled in at 31.2 V, demonstrating the mechanical stability of our monocrystalline silicon relays, the pull-out voltage varied from cycle to cycle as shown in Fig. 8. This is due to the changing nature of the contact surface with cycling, exacerbated by our choice of Au as a contact material (chosen for easy prototyping). First, the relay was cycled twice, then the leakage experiment was performed, and afterwards the relay was cycled twice more. As the gate voltage could not be monitored during the experiment (to avoid loading of the electrode), we estimated the pull-out voltage based on the measured pull-out voltages in the cycles before and after the experiment, as shown in Fig. 8. While an estimate, in our experience, Au coated relays show reasonably consistent pull-out behaviour for a few cycles after the first, before the Au contact surface starts to degrade. In equation (14), V_{PI}(=31.2 V), the pull-in voltage, is also the initial voltage on the relay gate when the gate drive is removed, and V_{PO}(=18 V), the pull-out voltage, occurs at t_{PO} =165 min. The same current leakage is seen at the drain electrode (which has the same pad size). Now, the static energy consumption E_{st} corresponding to maintaining the charge on the electrode pad can be calculated as in equation (15). vspace-2mm

$$E_{st} = I_{G\_lk}T\frac{(V_{PI} - V_{PO})}{2} = 7.58 \times 10^{-11}\,\text{J} \qquad (15)$$

Given that $i_{DS\_lk} = 0$, and the pad capacitance $C_{sub} >> c_R$ the relay capacitance, with over two orders of magnitude

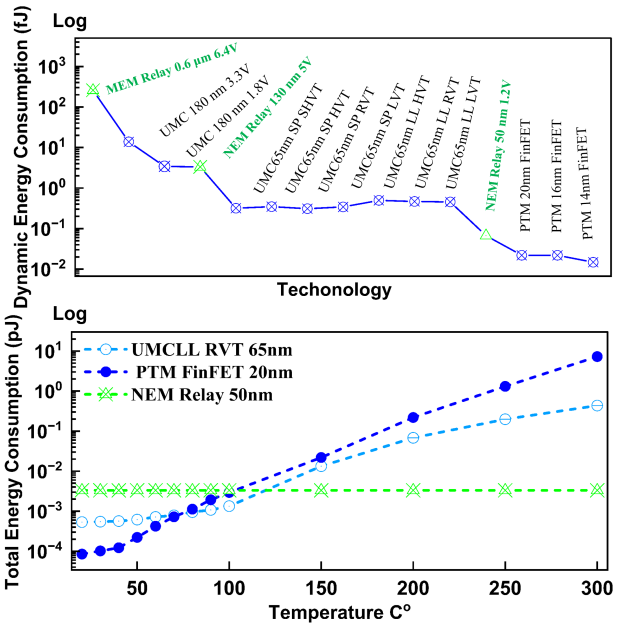

Fig. 9. Comparison of energy consumption in NEM/MEM relays and CMOS. (a) Dynamic energy consumed in a binary switching transfer; the relays comprise the R1 prototype with measured energy, a 130 nm relay with a measured $\boldsymbol{V}_{\rm pi}$, and a 50 nm relay where the $\boldsymbol{V}_{\rm pi}$ was estimated from FEM. The CMOS processes include the UMC 180 nm process with two transistor variants (1.8 and 3.3 V), the UMC 65 nm standard process with four transistor variants, and the UMC 65 nm low leakage process with three transistor variants. Abbreviations SP and LL stand for Standard Process and Low Leakage. Suffixes SHVT (super high), HVT (high), RVT (regular), and LVT (low) refer to devices within the same technology that have different threshold voltages. The BSIM-CMG 14 nm, 16 nm, and 20 nm FinFET processes [22] are also included. (b) Total energy estimated as the sum of dynamic energy consumed for a single switching event and the static dissipation over a 1 μs period for the 50 nm relay and selected low-leakage processes, the UMC 65 nm LL RVT, and the PTM 20 nm FinFET, with increasing temperature.

difference, this static energy is determined by the SOI substrate characteristics and pad geometry.

V. Comparison with CMOS

To gain insight into the potential savings offered by NEM and MEM relay technology, we compared the energy consumption of relays with 12 different CMOS technologies based on a study that estimated the energy consumed in a binary switching transfer of an inverter [22], [23]. In addition to the experimentally characterised relay R1, two scaled relays were considered, with a gate gap $g_{\rm G}$ =130 nm and a measured $V_{\rm pi}$ of 5 V, and $g_{\rm G}$ =50 nm with $V_{\rm pi}$ estimated to be 1.2 V from an FEM simulation, see Table III. For both scaled designs, the open-state and closed-state capacitances $C_{\rm op}$ and $C_{\rm cl}$ were calculated using $g_{\rm G}$ and contact airgap $g_{\rm C}$, using an empirical expression reported by Leus and Elata to account for the fringing fields typically seen in microscale structures [24], which makes the actual capacitance up to 2× the parallel-plate capacitance. The dynamic energy, calculated using eq. (12), is also shown in Table III. The dynamic energy component reported for CMOS in [22], [23] was halved to ensure the output capacitance corresponds to the parasitic capacitance of a single device. As illustrated in Fig. 9(a), the dynamic energy consumption of the 50 nm NEM relay is comparable to the UMC 180 nm CMOS technology.

TABLE III
Parameters of NEM Relays with Fringing Effect.

Parameter	NEM 130nm	NEM 50nm
Pull-in Voltage $V_{\rm pi}$ (V)	5.0	1.2
Gate flat length (lx_G) (μm)	5.00	1.25
Thickness $t_{\rm Si}$ (μm)	0.24	0.15
Gate airgap (g_G) (μm)	0.13	0.05
Contact airgap (g_C) (μm)	0.05	0.02
Hinge width w_H (μm)	0.20	0.05
Open-state Cap. $C_{\rm op}$ (fF)	0.16	0.05
Closed-state Cap. $C_{\rm cl}$ (fF)	0.21	0.07

Next, the total energy consumption - comprising the dynamic and static components - of the low-leakage UMC 65 nm transistor, the PTM 20 nm FinFET (which provides better control of carriers), was compared with the 50 nm NEM relay across a temperature range from 20 °C to 300 °C, simulating the demands of high-temperature edge computing [25], [26]. The static energy component we measured in the MEM technology is caused by substrate leakage and not related to the relay characteristics, rather the pad dimensions and properties of the substrate used. As this would be present in both types of technologies and was not considered in the CMOS energy consumption calculations [23], this component was disregarded for comparison. This is distinct from the subthreshold drain-to-source conduction that is the origin of the static energy consumption in CMOS [22], [23], which is not present in NEM/MEM technology as we verified. Thus, the total energy dissipation in the UMC 65 nm and PTM 20 nm processes increases with rising temperature due to the increase in leakage current [23], [27], [28], [29], whereas the energy consumption of the NEM relay is constant. The total energy consumption in the UMC 65 nm and PTM 20 nm processes exceeds that of the NEM relay at around 109 °C and 99 °C respectively. The PTM processes has more severe leakage, even with the FinFET structure, revealing the inherent static energy dissipation challenges within CMOS technologies.

VI. Conclusions

This work is the first to verify the dynamic and static energy consumption of a MEM relay through characterisation, and derive an expression for the dynamic energy consumption that considers the variation of relay capacitance as a quadratic function of the applied gate voltage. A comparison study with CMOS shows that the dynamic energy consumption of a NEM relay with a footprint of ≈120 × 290 μm^2 is comparable to that of a 180 nm CMOS process. Furthermore, as NEM relays do not have subthreshold conduction, the total energy consumption is unvarying with increasing temperature. By contrast, CMOS has a static energy consumption that increases exponentially with temperature. Therefore, NEM and MEM technologies present significant opportunities for energy savings over CMOS even in applications with moderately high temperatures, such as commonly found in edge computing applications.

REFERENCES

[1] H. Kam, T.-J. K. Liu, V. Stojanović, D. Marković, and E. Alon, "Design, optimization, and scaling of MEM relays for ultra-low-power digital logic," *IEEE Trans. Electron. Devices*, vol. 58, no. 1, pp. 236–250, 2010.

[2] T.-H. Lee, S. Bhunia, and M. Mehregany, "Electromechanical computing at 500 °C with silicon carbide," *Science*, vol. 329, no. 5997, pp. 1316–1318, 2010.

[3] R. Li and H. Fariborzi, "MEM relay for the Internet of Things applications," in *Proc. IEEE Symp. Microelectronics Technol. (SBMICRO)*, 2022, pp. 1–4.

[4] S. Rana, J. Mouro, S. J. Bleiker, J. D. Reynolds, H. M. Chong, F. Niklaus, and D. Pamunuwa, "Nanoelectromechanical relay without pull-in instability for high-temperature non-volatile memory," *Nat. Commun.*, vol. 11, no. 1, p. 1181, 2020.

[5] D. Grogg, U. Drechsler, A. Knoll, U. Duerig, Y. Pu, C. Hagleitner, and M. Despont, "Curved in-plane electromechanical relay for low power logic applications," *J. Micromech. Microeng.*, vol. 23, no. 2, p. 025024, 2013.

[6] J. T. Best, M. A. Masud, M. P. de Boer, and G. Piazza, "Phase change nanoelectromechanical relay for nonvolatile low leakage switching," *Adv. Electron. Mater.*, vol. 8, no. 9, p. 2200085, 2022.

[7] H. Samaali, F. Najar, and A. Chaalane, "Modeling and design of an ultra low-power NEMs relays: Application to logic gate inverters," *Analog Integr. Circuits Signal Process.*, vol. 104, pp. 17–26, 2020.

[8] S. Rana, T. Qin, D. Grogg, M. Despont, Y. Pu, C. Hagleitner, and D. Pamunuwa, "Modelling NEM relays for digital circuit applications," in *Proc. IEEE Int. Symp. on Circuits and Syst. (ISCAS)*, 2013, pp. 805–808.

[9] T. Qin, S. Rana, and D. Pamunuwa, "Design methodologies, models and tools for very-large-scale integration of NEM relay-based circuits," in *Proc. IEEE Int. Conf. on Computer-Aided Des. (ICCAD)*, 2015, pp. 641–648.

[10] J. B. Muldavin and G. M. Rebeiz, "Nonlinear electro-mechanical modeling of mems switches," in *Proc. IEEE MTT-S Int. Microwave Symp. Dig. (IMS)*, 2001, pp. 2119–2122.

[11] S. Rana, T. Qin, A. Bazigos, D. Grogg, M. Despont, C. L. Ayala, C. Hagleitner, A. M. Ionescu, R. Canegallo, and D. Pamunuwa, "Energy and latency optimization in NEM relay-based digital circuits," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 61, no. 8, pp. 2348–2359, 2014.

[12] D. Pamunuwa, E. Worsey, J. D. Reynolds, D. Seward, H. M. H. Chong, and S. Rana, "Theory, design, and characterization of nano-electromechanical relays for stiction-based non-volatile memory," *J. Microelectromech. Syst.*, vol. 31, no. 2, pp. 283–291, 2022.

[13] F. Chen, H. Kam, D. Markovic, T.-J. K. Liu, V. Stojanovic, and E. Alon, "Integrated circuit design with NEM relays," in *Proc. IEEE Int. Conf. on Computer-Aided Des. (ICCAD)*, 2008, pp. 750–757.

[14] M. Spencer, F. Chen, C. C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T.-J. K. Liu, D. Marković, E. Alon, and V. Stojanović, "Demonstration of integrated micro-electro-mechanical relay circuits for VLSI applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 308–320, 2011.

[15] Q. Tang, E. Worsey, M. K. Kulsreshath, Y. Fan, Y. Li, S. Bleiker, H. Chong, F. Niklaus, and D. Pamunuwa, "Measurement and analysis of dynamic energy consumption in microelectromechanical relays," *submitted to IEEE Int. Symp. Circuits Syst. (ISCAS)*, 2025.

[16] Z. A. Ye, *Millivolt Micro-Electro-Mechanical Relay Devices & Circuits*. University of California, Berkeley, 2020.

[17] S. Rana, J. D. Reynolds, T. Y. Ling, M. S. Shamsudin, S. H. Pu, H. M. Chong, and D. Pamunuwa, "Nano-crystalline graphite for reliability improvement in mem relay contacts," *Carbon*, vol. 133, pp. 193–199, 2018.

[18] J. D. Reynolds, E. W. S. Rana, Q. Tang, M. K. Kulsreshath, H. M. H. Chong, and D. Pamunuwa, "Single-contact, four-terminal microelectromechanical relay for efficient digital logic," *Adv. Electron. Mater.*, vol. 9, no. 1, p. 2200584, 2023.

[19] Keithley Instruments, Inc., *2600B Series SourceMeter® SMU Instruments User's Manual*, Aug. 2016, accessed: Sep. 25, 2023. [Online]. Available: https://download.tek.com/manual/2600BS-901-01_C_Aug_2016_2.pdf

[20] M. Han, Q. Yuan, X. Sun, , and H. Zhang, "Design and fabrication of integrated magnetic MEMS energy harvester for low frequency applications," *J. Microelectromech. Syst.*, vol. 23, no. 1, pp. 204–212, 2013.

[21] B. Andò, S. Baglio, C. Trigona, N. Dumas, L. Latorre, and P. Nouet, "Nonlinear mechanism in MEMS devices for energy harvesting applications," *J. Micromech. Microeng.*, vol. 20, no. 12, p. 125020, 2010.

[22] P. Kocanda and A. Kos, "Energy losses and DVFS effectiveness vs technology scaling," *Microelectron. Int.*, vol. 32, no. 3, pp. 158–163, 2015.

[23] ——, "Static and dynamic energy losses vs. temperature in different CMOS technologies," in *Proc. Int. Conf. Mixed Design Integr. Circuits & Syst. (MIXDES)*, 2015, pp. 446–449.

[24] V. Leus and D. Elata, "Fringing field effect in electrostatic actuators," *Technion-Israel Institute of Technology technical report no ETR-2004-2*, 2004.

[25] H. Wang, P. Lai, M. Z. Islam, A. S. M. K. Hasan, A. D. Mauro, R. Russell, Z. Feng, K. Chen, A. Faruque, and T. White, "A review of silicon carbide CMOS technology for harsh environments," *Mater. Sci. Semicond. Process.*, vol. 178, p. 108422, 2024.

[26] D. Kimoto, "Characterization and modeling of SiC integrated circuits for harsh environment," Ph.D. dissertation, KTH Royal Institute of Technology, 2017.

[27] M. K. Rai, A. Gupta, and S. Rai, "Comparative analysis & study of various leakage reduction techniques for short channel devices in junctionless transistors: A review and perspective," *Silicon*, vol. 14, no. 9, pp. 4423–4445, 2022.

[28] S. Datta, W. Chakraborty, , and M. Radosavljevic, "Toward attojoule switching energy in logic transistors," *Science*, vol. 378, no. 6621, pp. 733–740, 2022.

[29] P. L. Dreike, D. M. Fleetwood, D. B. King, D. C. Sprauer, and T. E. Zipperian, "An overview of high-temperature electronic device technologies and potential applications," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 17, no. 4, pp. 594–609, 1994.