Nanofabrication of monolithically integrated multilayer metasurfaces via fully CMOS-compatible processes

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Abstract: We have developed a novel metasurface stacking methodology that is fully compatible with standard Complementary Metal-Oxide-Semiconductor（CMOS） processes, advancing the mass production and commercialization of metasurface technologies.

Metasurfaces are planar arrays of subwavelength nanostructures that enable precise control over the amplitude, phase, polarization, spectrum, and propagation direction of light. These capabilities have been extensively explored over the past decade, leading to a wide range of potential applications, including ultra-thin imaging lenses, holography, and vortex beam light sources [1].

Regardless of these progresses, recent studies have highlighted inherent limitations of monolayer metasurfaces in their light manipulation capabilities. These limitations are primarily due to intrinsic constraints in light-matter interactions imposed by monolayer meta-atom designs, which cannot be fully compensated for using advanced design methods such as multiplexing and machine learning-based inverse design. Similar to conventional optics, multilayer metasurfaces offer enhanced light manipulation capabilities, as each additional layer introduces new degrees of freedom. This enables advanced functionalities such as wide field-of-view imaging, where focusing and phase correction, two essential components of wavefront shaping, are implemented using two different metasurfaces [2].

Multilayer metasurfaces can be categorized into two types: multi-wafer cascaded configurations and monolithically integrated configurations. The former resembles traditional optical assemblies, where multiple metasurfaces are precisely aligned to achieve the desired function [3]. Although easier to fabricate, this approach is limited by its large spatial footprint and stringent alignment requirements. In contrast, monolithically integrated multilayer metasurfaces consolidate all layers onto a single substrate, greatly improving device compactness and eliminating alignment issues.

We have focused on the nanofabrication of monolithically integrated multilayer metasurfaces. Due to the potential importance of this type of metasurface, numerous nanofabrication methodologies have been explored. For instance, Reference [4] reported metasurfaces fabricated on both sides of a thick substrate, where the large and fixed distance between the two layers limits the applications of this method. References [5] and [6] used spin-coated polymers and thermal curing to create a flat silicon oxide intermediate layer, on which the second layer of metasurface was fabricated. References [7] and [8] used polymers such as PDMS and PMMA for metasurface encapsulation and stacking. Reference [9] used a special photoresist as an intermediate layer. These methods employed materials or processes that are not standard in semiconductor foundries, which can significantly increase the complexity and cost of mass production.

In contrast to these existing approaches, our nanofabrication methodology is fully CMOS-compatible. The critical step in our approach is chemical mechanical polishing (CMP), used to planarize a buffer layer before the fabrication of a second layer of metasurface. CMP is a standard semiconductor fabrication process that synergizes chemical etching and mechanical grinding to achieve high-precision planarization of wafer surfaces. Figures 1 and 2 show the morphology of a sample fabricated following this methodology. The fabrication of the first metasurface layer followed a standard process that utilized electron beam lithography (EBL). Subsequently, a 2.2 μm thick SiO_2 buffer layer was deposited via plasma-enhanced chemical vapor deposition (PECVD) over the nanostructures. Planarization was then carried out using CMP with a 50% colloidal silica slurry, resulting in a highly flat top surface of the buffer layer (Figure 1). The second metasurface layer was subsequently fabricated following the same procedure as the first.

[1] J. Hu, S. Bandyopadhyay, Y.-h. Liu, L.-y. Shao, A Review on Metasurface: From Principle to Smart Metadevices, Front. Phys. 8 (2021) 586087.
[2] F. Yang, M. Y. Shalaginov, H. Lin, S. An, A. Agarwal, H. Zhang, C. Rivero-Baleine, T. Gu, J. Hu, Wide field-of-view metalens: a tutorial, Adv. Photon. 5 (2023) 033001.
[3] F. Mei, G. Qu, X. Sha, J. Han, M. Yu, H. Li, Q. Chen, Z. Ji, J. Ni, C.-W. Qiu, Q. Song, Y. Kivshar, S. Xiao, Cascaded metasurfaces for high-purity vortex generation, Nat. Commun. 14 (2023) 6410.
[4] B. Groever, W.T. Chen, F. Capasso, Meta-Lens Doublet in the Visible Region, Nano Lett. 17 (2017) 4902–4907.
[5] J. Tan, R. Pan, Y. Xiang, Z. Tang, B. Wang, J. Li, Unilateral Asymmetric Radiation in Bilayer Metasurfaces, Adv. Funct. Mater. (2025) 2501156.
[6] Y. Bao, F. Nan, J. Yan, X. Yang, C.-W. Qiu, B. Li, Observation of full-parameter Jones matrix in bilayer metasurface, Nat. Commun. 13 (2022) 7550.
[7] J. Zhou, I. I. Kravchenko, H. Wang, J. R. Nolen, G. Gu, J. Valentine, Multilayer Noninteracting Dielectric Metasurfaces for Multiwavelength Metaoptics, Nano Lett. 18 (2018) 7529-7537.
[8] Y. Zhou, I.I. Kravchenko, H. Wang, H. Zheng, G. Gu, J. Valentine, Multifunctional metaoptics based on bilayer metasurfaces, Light Sci. Appl. 8 (2019) 80.
[9] L. Deng, Z. Li, Z. Zhou, Z. He, Y. Zeng, G. Zheng, S. Yu, Bilayer-Metasurface Design, Fabrication, and Functionalization for Full-Space Light Manipulation, Adv. Opt. Mater. 10 (2022) 2102179.

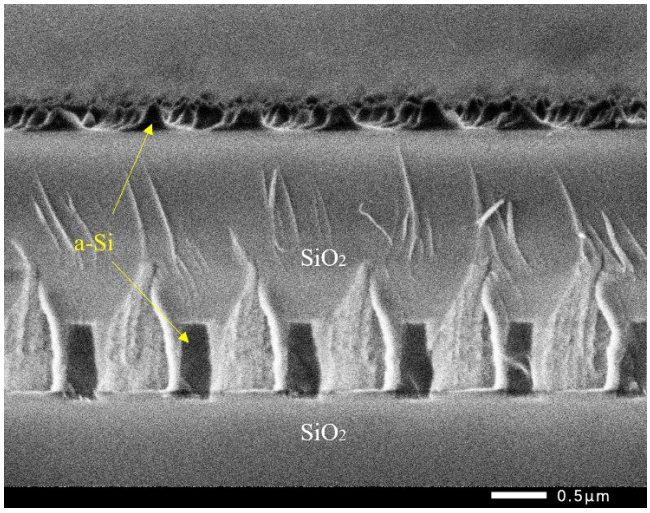

Figure 1. Cross-sectional SEM image of the double-layer metasurface fabricated using CMP planarization. The two metasurface layers, composed of amorphous silicon (a-Si) nanostructures, are separated by a SiO_2 buffer layer. CMP was employed to planarize this buffer layer. The features visible within the buffer layer are cleaving-induced fractures resulting from the wafer cross-sectioning process.

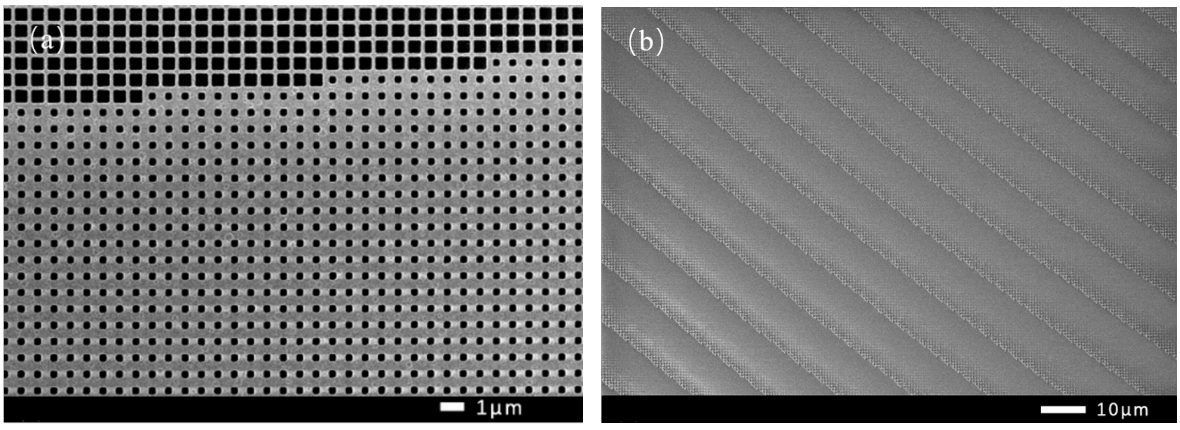

Figure 2. Planar view of the two metasurface layers. (a) Bottom layer, imaged prior to deposition of the SiO_2 buffer layer. (b) Top layer, imaged after completion of the nanofabrication process.