# Memristor synapse – A device-level critical review

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## Abstract

The memristor has long been known as a nonvolatile memory technology alternative and has recently been explored for neuromorphic computing, owing to its capability to mimic the synaptic plasticity of the human brain. The architecture of a memristor synapse device allows ultra-high-density integration by internetworking with crossbar arrays, which benefits large-scale training and learning using advanced machine-learning algorithms. In this review, we present a statistical analysis of neuromorphic computing device publications from 2018 to 2025, focusing on various memristive systems. Furthermore, we provide a device-level perspective on biomimetic properties in hardware neural networks such as short-term plasticity (STP), long-term plasticity (LTP), Spike Timing-Dependent Plasticity (STDP), and Spike Rate-Dependent Plasticity (SRDP). Herein, we highlight the utilization of optoelectronic synapses based on 2D materials driven by a sequence of optical stimuli to mimic the plasticity of the human brain, further broadening the scope of memristor controllability by optical stimulation. We also highlight practical applications ranging from MNIST dataset recognition to hardware-based pattern recognition, and explore future directions for memristor synapses in healthcare, including artificial cognitive retinal implants, vital organ interfaces, artificial vision systems, and physiological signal anomaly detection.

***Keywords: Memristor synapse, STP, LTP, SRDP, and STDP***

## 1. Introduction

Currently, the world is becoming increasingly dependent on artificial intelligence (AI) computations. AI-powered chips are not only used for supercomputers and cloud servers but also for personal gadgets and computers, which modern life and the global economy cannot run without. The development of these chips mainly focuses on advanced architectures, e.g., graphic and tensor processing units and AI-specific accelerators, and they stimulate the progress of deep learning due to their high computing speed [1]. Nevertheless, the current computer architecture is based on conventional von Neumann designs that rely on data transfer between the processing unit and memory unit, and its transfer rate is facing a limit as the task complexity increases[2]. This von Neumann bottleneck limits the processing speed due to the shared system bus between the CPU and memory, restricting simultaneous instruction fetching and data processing [3]. This problem makes the AI chips consume high energy and limits their efficiency and scalability [1].

Computing-in-memory (neuromorphic computing) is a new paradigm to solve this problem, where the data do not necessarily have to be processed at the processing unit but at the memory unit itself, mimicking how the human brain works. The brain is the most efficient computing system capable of performing complex data processing enabled by a large-scale interconnected neural network that stores and processes data at the same place and in parallel[4]. This interconnected neural network is governed by synapses to perform synaptic functions[5].

Several memristive systems, memristor, phase-change, spintronic and ferroelectric memory devices, can mimic the synaptic functions, showing the potential for neuromorphic computing architectures; thus, they are called artificial synapses [6–11]. Research on neuromorphic computing based on memristive systems has exponentially increased over the last decade, as shown in Figure 1. This trend indicates the urgent demand for faster and smarter computing machines in the real world. Among these memristive systems, it has been shown that phase-change and resistive memories are the most prominent subfields showing rapid growth in development (Fig. 1(b)). However, phase-change memory technology has a long history of scientific contributions and its development is much more mature[12]. Ferroelectric and spintronic memory devices have been developed over the last few decades[13]. The scientific progress in these fields is not as fast as that in resistive

memory. One of the reasons why resistive memory has gained considerable attention is its feasibility for integration with a diode selector, which has the same sandwich structure as a memristor (1D1M, 1-diode 1-memory). In circuit-level implementation, a selected device must be stacked with each memristive system to avoid the sneak-path issue in a massive array configuration. All memristive systems except memristors require transistors as their selectors (1T1M, 1-transistor 1-memory)[14]. The transistor cell structure (10-30$F^2$, where F is the feature size) is the constraining factor hindering the fabrication of an ultra-high-density synaptic network, whereas the 1D1M configuration has a cell size of $4F^2/N$ (N is the number of stacked layers), which is promising for a large artificial neural network (ANN)[15]. The facile architecture of the two-terminal memristor synapse offers a brain-inspired, highly dense computing element that complies with Moore's law[14].[6][16][17][2][18][19–21][22,23]

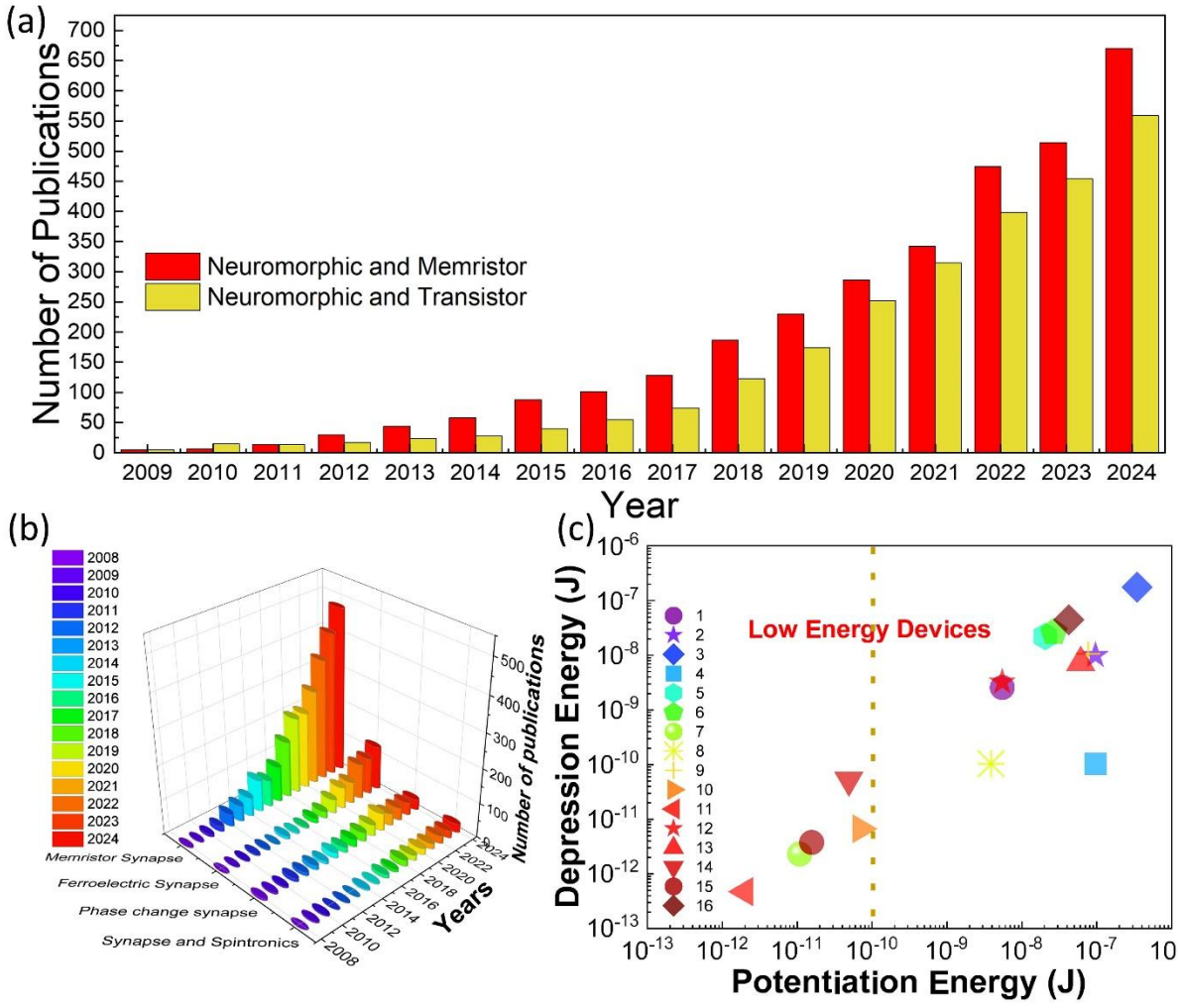


**Figure 1.** (a) Number of publications in neuromorphic computing based on memristor and transistor technologies; (b) Number of publications of artificial synapses based on various memristive systems; (c) Memristor

synapse exhibiting lower energy operation using Insulator Engineering (IE) and Electrode Engineering (EE) [6,16–30]. Data in (a) and (b) were obtained from webofscience.com.

An ANN employing a 1024-cell array of memristor synapses (memristor-based synaptic devices) consumes much less power than the Intel Xeon Phi processor [6]; von Neumann's consumes more energy for cognitive learning and data processing, not only because of the CPU memory bottleneck but also because its transistor-based processing unit is volatile and requires continuous power to maintain its synaptic weight[31]. Moreover, ANN should be integrated with CMOS-based neuron-driving circuits, which are power-hungry [32]. A feasible method to achieve low-power computation is to utilize a low-power ANN based on memristor synapses. The synaptic weight of a memristor synapse can be maintained over a period without continuous power (nonvolatile), and its programming voltage and current are typically 1V and 10 μA or less, respectively. If typical memristors require 1-3 nJ per spike [33] and $10^8$ spikes are needed for the full 10000-image MNIST test set (considering about $10^3$ spikes per neuron across $10^4$ neurons firing during training and inference cycles) [34], so we can hypothetically estimate that the memristors only consume less than 1 J when scaled to large arrays of memristor devices. On the other hand, if the Xeon Phi processor runs digital CNN-based MNIST and assuming it consumes 225 W under full load, and thus, it requires 25kJ just for one training session [35]. Therefore, the memristors can reduce the overall system-level power consumption by 4 to 5 orders of magnitude [2][36]. Furthermore, the operating power of the memristor synapse can be further reduced by reducing the cell size[37], stacking in a 3D configuration[38–40], and insulator and electrode engineering[41,42]. Based on the trend of the energy required to produce synaptic plasticity, shown in Figure 1(c), we found that insulator engineering is an effective approach to reduce the power consumption. Nevertheless, memristor synapses have several challenges that hinder their large-scale integration, e.g., device variability, nonlinear and asymmetric weight update, and epoch training variability. This review article discusses these challenges and overviews the recent approach to mitigate them.

## 1. Architectonics and device physics

The basic architecture of a memristor synapse is a two-terminal metal (top electrode)/insulator (switching layer)/metal (bottom electrode) sandwich structure, as shown in Figure 2(a). Among various two-terminal

configurations, such as planar (both electrodes face each other with a nanometer gap separation)[43], points (the electrodes have crossed[43], circular, [29] or rectangular shapes[44], where each cell does not share its electrode(s)) with other cells), and crossbars[45]. The crossbar configuration is the most feasible way to achieve a massive ANN because the cells share both the bottom and top electrodes along the intersecting line array, facilitating interconnection between cells (Fig 2(b, c)).

The synaptic weight of a memristor synapse is controlled by the electrochemistry of the ionic species in the insulator, which drift under the influence of an electric field to build a conduction channel in the switching layer.[46] These ionic species can be cations (metal ions: Ag[47–49], Cu[50–52], Ni[53], Co[54], In[55–58], Te[59], or Pd[60]), anions (non-metal ions, oxygen[61], nitrogen[62,63], carbon[64], and their vacancies), or a combination of both (hybrids)[65,66]. Cation-based memristor synapses, also known as conducting-bridge memory or electrochemical metallization memory (ECM), rely on the migration of metallic ions originating from the active electrode (as the cation source) into the switching layer, forming a bridge connecting the bottom and top electrodes. Fig 2(d) depicts the direct growth of Ag nanobridges in the $Ag/SiO_2/Pt$ ECM cell [67]. Nevertheless, in some cases, an inert metal may also migrate and form a bridge,[68] which could be due to the property of the film affecting the mass transport under an electric field[69]. The geometry of the metallic bridge is governed by film inhomogeneity and electric field distribution, which determine the redox rate, nucleation rate, and ionic mobility of the metal ions. For example, high rates and mobility result in an inverted cone-shaped filament that grows from the inert electrode, whereas low rates and mobility result in discrete nanoclusters growing from the active electrode, forming a forward cone shape[70]. However, if no active electrode is used in the device, the percolation of intrinsic donor defects in the switching film may form a conducting filament because of the drift of anions under an electric field. In metal oxide (MO) and metal nitride (MN) systems, the filament consists of oxygen ($V_O^{2+}$) and nitride ($V_N^{+}$) vacancies. The filament is formed by the reduction of oxygen or nitrogen atoms, forming $O^{2-}$ or $N^{3-}$ anions, respectively, where these anions move to the anode and create vacancies ($V_O^{2+}$ or $V_N^{3+}$) in the system[71,72]. Other possible ionic vacancy configurations are also possible, depending on the insulator and electrode materials[73,74]. Thereafter, these vacancies are ordered to connect both electrodes as a pathway for electrons to flow from the cathode to the anode.

Several studies have suggested that the arrangement of these vacancies in crystal lattices may induce a phase transformation, forming a highly conducting phase in the switching layer, such as the Zn-dominated $ZnO_{1-x}$ and $Ti_4O_7$ Magnéli phases in ZnO and TiOx systems, respectively; in some cases, it can also induce amorphous-to-crystalline to form a conducting filament(s), as depicted in Fig. 2(e-h) [75]. Another compelling evidence on the phase change phenomenon occurred in the SiOx system, where the filament is in the form of a semi-metallic Si state [76]. A similar phenomenon was also observed in the $SrTiO_3$ system; it is found that the formation of Sr-rich secondary phases leads to a high current density [77]; it is important to note that no Sr or Ti ionic movement is involved in the switching process. In hybrid-based devices, both anion and cation

species are involved in the switching operation, where the filament and bridge coexist to build a complete conduction channel connecting the electrodes[78,79]. Metal cations have a smaller radius and higher mobility than anions; thus, cations may reach the cathode faster, and the bridge structure has a larger portion of the channel than the filament[66]. Nevertheless, the involvement of various species in a complex system, such as memristor synapses with an active metal-doped oxynitride system, requires further investigation to explain the contribution of each defect to channel formation and its impact on synaptic stability.

In contrast to filamentary conduction, an electrochemical reaction can occur in most parts of the bulk switching layer, which is known as a homogeneous or interfacial switching mechanism. This non-filamentary conduction is similar to the anion-based mechanism; in the ZnO-based system, for example, the repulsion of anions ($O^{2-}$) occurs in a much larger region in the bulk, where this process creates a conducting (oxygen-poor) region above the anode and an insulating (oxygen-rich) region below the cathode in the switching layer[80]. In the $ABO_{3-x}$ system, the electrochemical reaction induces a brownmillerite-perovskite phase transformation, a phenomenon known as reversible phase change [81]. Figure 2(i) depicts the phase transformation process in the LaSrMnO system [82], Contrary to most metal-oxide systems, the conducting (perovskite) and insulating (brownmillerite) regions in $ABO_{3-x}$ are oxygen-rich and oxygen-poor phases, respectively [83]. Electron transport in LaSrMnO relies on the hopping of electrons via $Mn^{4+}$ and $Mn^{3+}$ cations, and the introduction of oxygen shifts the under-doped phase (insulating) towards the effective doping level, thereby decreasing the electrical resistance [82].

Based on the above discussion, the anion-based filamentary and homogeneous switching behaviors rely on electrochemically induced phase transition. Therefore, we can argue that the physical nature of the filamentary and interfacial mechanism is not simply a pile of oxygen vacancy defects providing electron path-ways between the two electrodes, but they rely on the transformation of an insulating phase into a conducting phase that occurs in the switching layer.

A similar phenomenon is observed in phase-change memory technologies; however, the difference is that the switching mechanism in phase-change memory relies on a heat-induced phase transition from crys-talline to amorphous, which means this process breaks the lattice frames and *vice versa [84]*. Nevertheless, this similarity brings us to question the fundamental terminology: can we classify anion-based filamentary and homogeneous memristor synapses as a class of (localized) phase-change memory?

A three-terminal structure, known as a memtransistor, was also proposed for fabricating memristor synapses [85]. Unlike the two-terminal memristor synapse, the gate in the memtransistor offers additional control to modify the conduction between the terminals[86]. Although the memtransistor offers operational

ability to minimize the sneakpath current across a large-scale array and mitigate device variability[87], the three-terminal device occupies a larger area than the two-terminal crossbar. Thus, this architecture limits high-density 3D integration. Nevertheless, the fabrication flow complexity of the memtransistor architecture is much less than that of any two-terminal memristive synapse with a transistor as the selection device (1T1M).

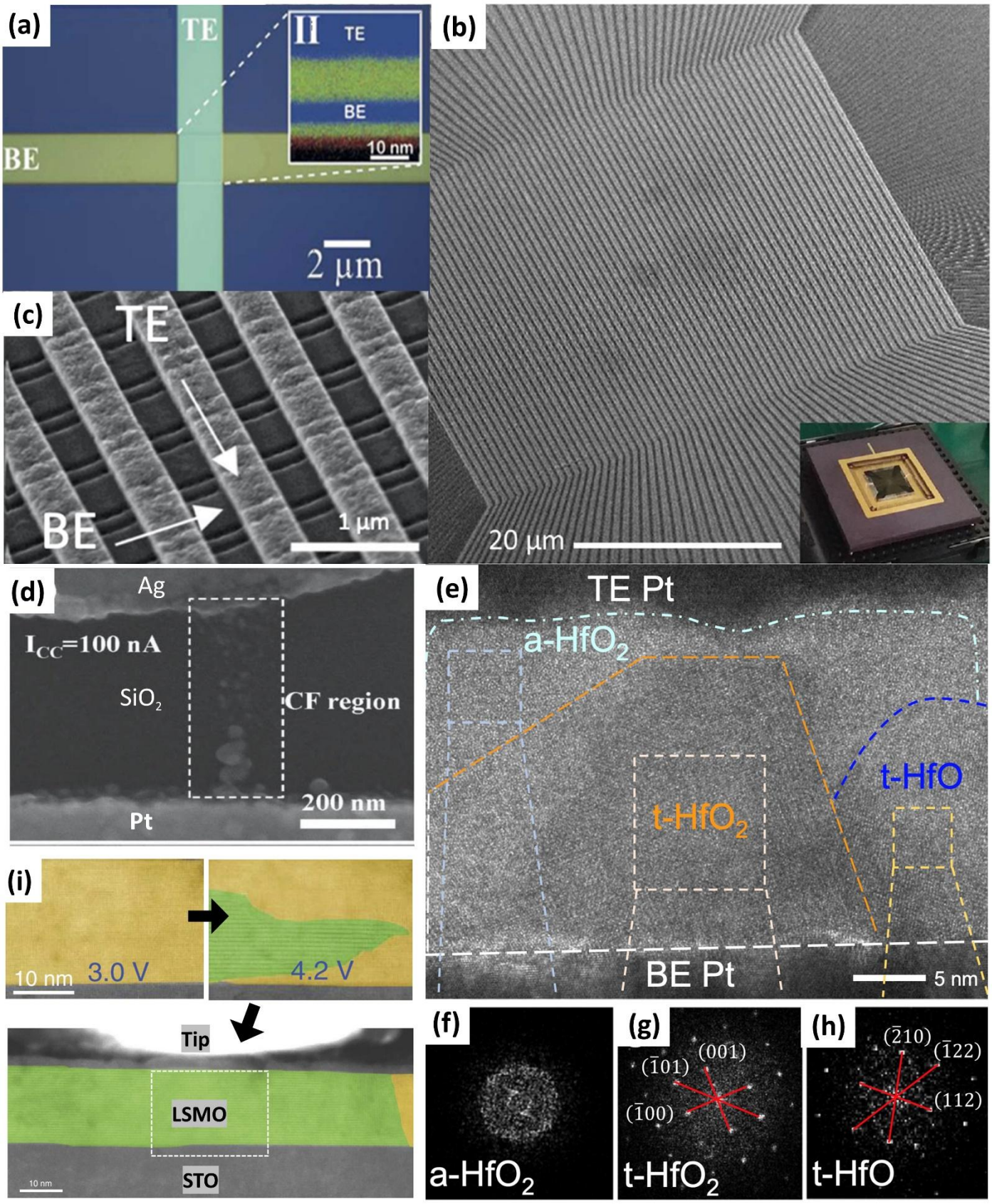

**Figure 2** (a) Typical architecture of two-terminal metal/insulator/metal memristor synapse, adapted from [88] and (b,c) high-density 64 x 64 memristor crossbar array configuration with a total of 4096 memory cells, adapted from [45], (d) Cation-based filamentary formations, adapted from [67], (e-h) Anion-based filamentary formations observed using TEM, adapted from [75], (i) homogeneous switching was observed using *in-situ* TEM, adapted from, adapted from [82].

## 2. Synaptic and neuromorphic capabilities

The mammalian brain consists of interconnected neurons that can process complex data via an electrochemical firing mechanism at synapses[89]. Synapses are junctions that connect each neuron in the network, as depicted in Figure 3(a), and transfer and receive chemical signals ($Ca^{2+}$, $Na^{+}$, or $K^{+}$ ions, known as neurotransmitters)[90]. Neurotransmission is mediated by the release of glutamate from a presynaptic neuron (the neuron or synapse that sends the neurotransmitter) to a postsynaptic neuron (the neuron that receives the neurotransmitter). Postsynaptic neurons contain AMPA receptors, which influence $Ca^{2+}$ influx, leading to synaptic plasticity[91,92]. Depending on how the presynaptic fires the transmitter and the postsynaptic response towards the incoming signal, the network can exhibit long-term and short-term memorization, which we define as neural plasticity [93,94].

Similarly, the firing mechanism of memristor synapses was achieved using electrical pulses, and the synaptic response was measured in terms of conductivity, as shown in Figure 3(b). In this case, the cathode acts as the pre-synapse and the anode as the post-synapse, whereas the mobile cation/anion in the insulator layer acts as the transmitter (Fig. 2). Various pulse schemes can be used to program memorization (synaptic strength); typically, a slow rate and low-amplitude stimulus will result in short-term memory (STM) that can retain the response for a short period (sub-milliseconds to minutes), after which the device starts to forget, followed by a rapid decay of conductance, as illustrated in Figure 3(c)[95].

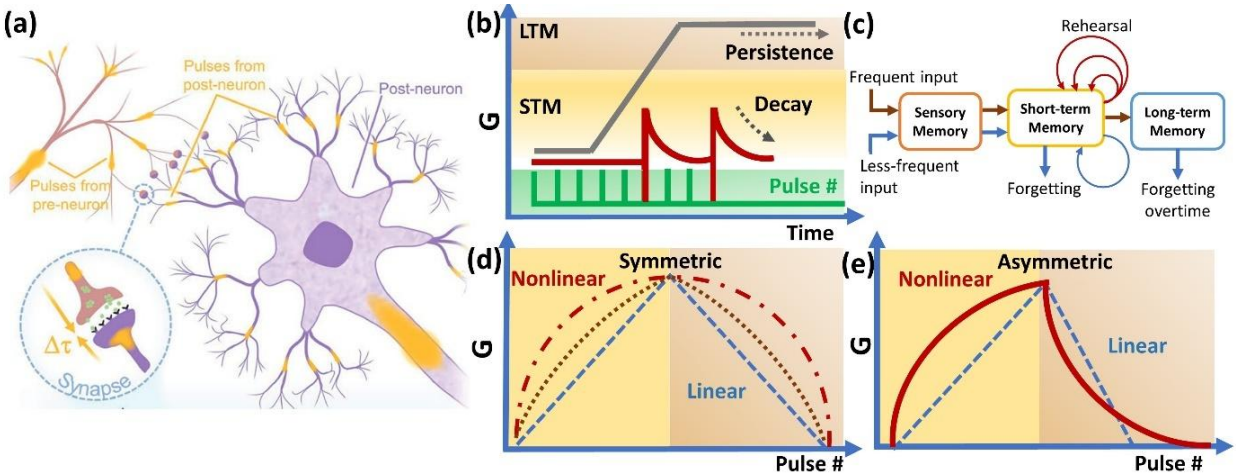


**Figure 3** (a) Schematic of synapses, reprinted from [96]; (b) & (c) Short-term and long-term memory effect on memristor synapse with different forgetting behaviour, inspired by [97]; (d) & (e) Symmetric and asymmetric synaptic feedback exhibiting linear and nonlinear actuation.

STM can evolve into long-term memory (LTM, hours to days) upon high-frequency stimuli or vice versa via opposite amplitudes. The rehearsal and forgetting mechanisms are similar to how the brain learns and processes information[91,92]. The decay rate of synaptic weight can be natural (intrinsic decay), programmed, or a combination of both. The increase and decrease in synaptic weight are called potentiation and depression processes, respectively, and the a/symmetricity of the potentiation and depression can be a linear or nonlinear response, as depicted in Figure 3(d, e). Ionic or organic-based memristor synapses often exhibit symmetric feedback, but these types of devices are less stable for lifelong deployment; meanwhile, whereas metal oxide-based devices are more durable but have asymmetric feedback because of the physical nature of the growth and dissolution of the conduction channel in the oxide[98]. Symmetrical synaptic feedback offers a more straightforward computing algorithm at the system level, and it is suggested that linearity determines the computing accuracy[99]. Most metal-oxide memristor synapses require soft breakdown (electroforming) to activate synaptic feedback (Figure 4(a))[45]. Different pulse schemes produce different synaptic feedback; Figs. 4(b-f) show the typical identical pulse (pairs) and nonidentical pulse schemes, and the nonidentical pulse often offers better linearity than its identical counterpart[2,45][100]. Linearity can also be enhanced by materials and interface engineering [2,45]; it is suggested that a multilayer switching film is an effective method to improve the linearity, since each layer has unique nanostructure and defect properties; thus, controlling the filament or bridge configuration during the synaptic process becomes easier [101,102]. However, there is still less investigation on the impact of nonlinear and asymmetric feedback on the speed and accuracy of ANN computations in actual implementation.

Besides nonlinearity, temporal variation, such as conductance drift and the dynamic range disparity, which often occur due to cycle-to-cycle and device-to-device fluctuation, can significantly affect the learning accuracy of the network. It is suggested that a network having a temporal variation of more than 22% would not be able to achieve 90% learning accuracy [103]. Device stacking techniques have been proposed to mitigate the temporal variation, e.g. 2M1T (a series of two memristor synapses connected with a transistor) [104] or put several memristors in parallel to suppress the random rejuvenation of the filament during the synaptic training process [105].

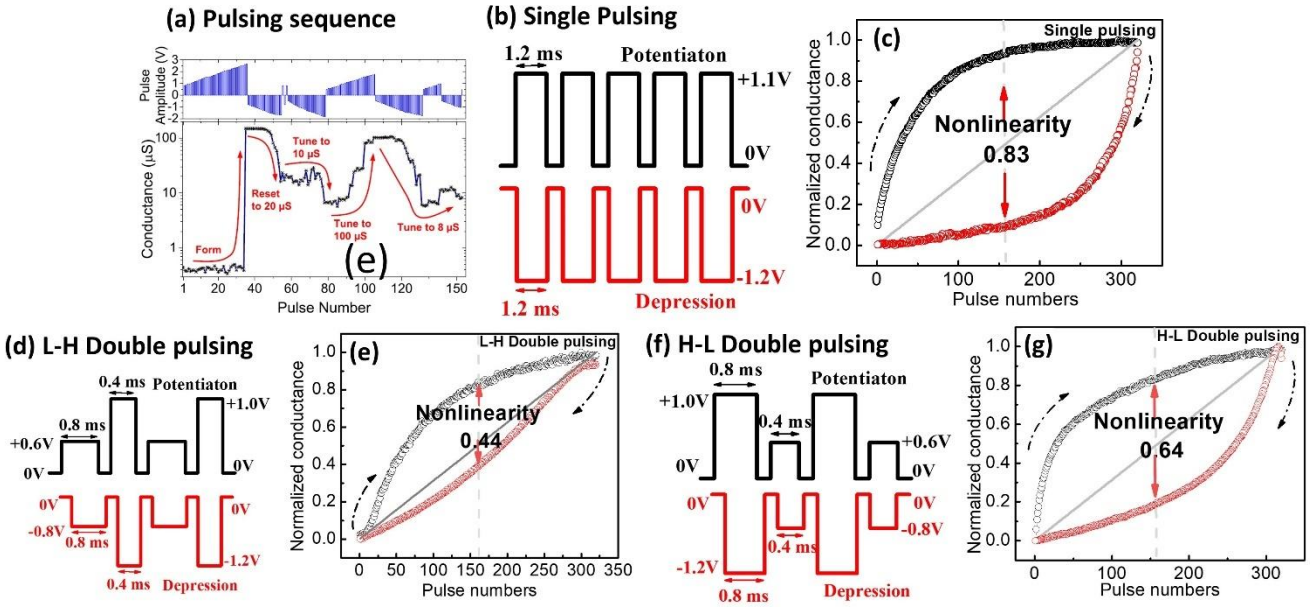


**Figure 4** (a) The typical pulsing sequence of the pristine memristor synapse, reprinted from [45]; on applying LTP and LTD of (b-c) identical pulses (single pulsing), (d-e) Low-High double pulsing, and (f-g) High-Low double pulsing schemes, reprinted from[100].

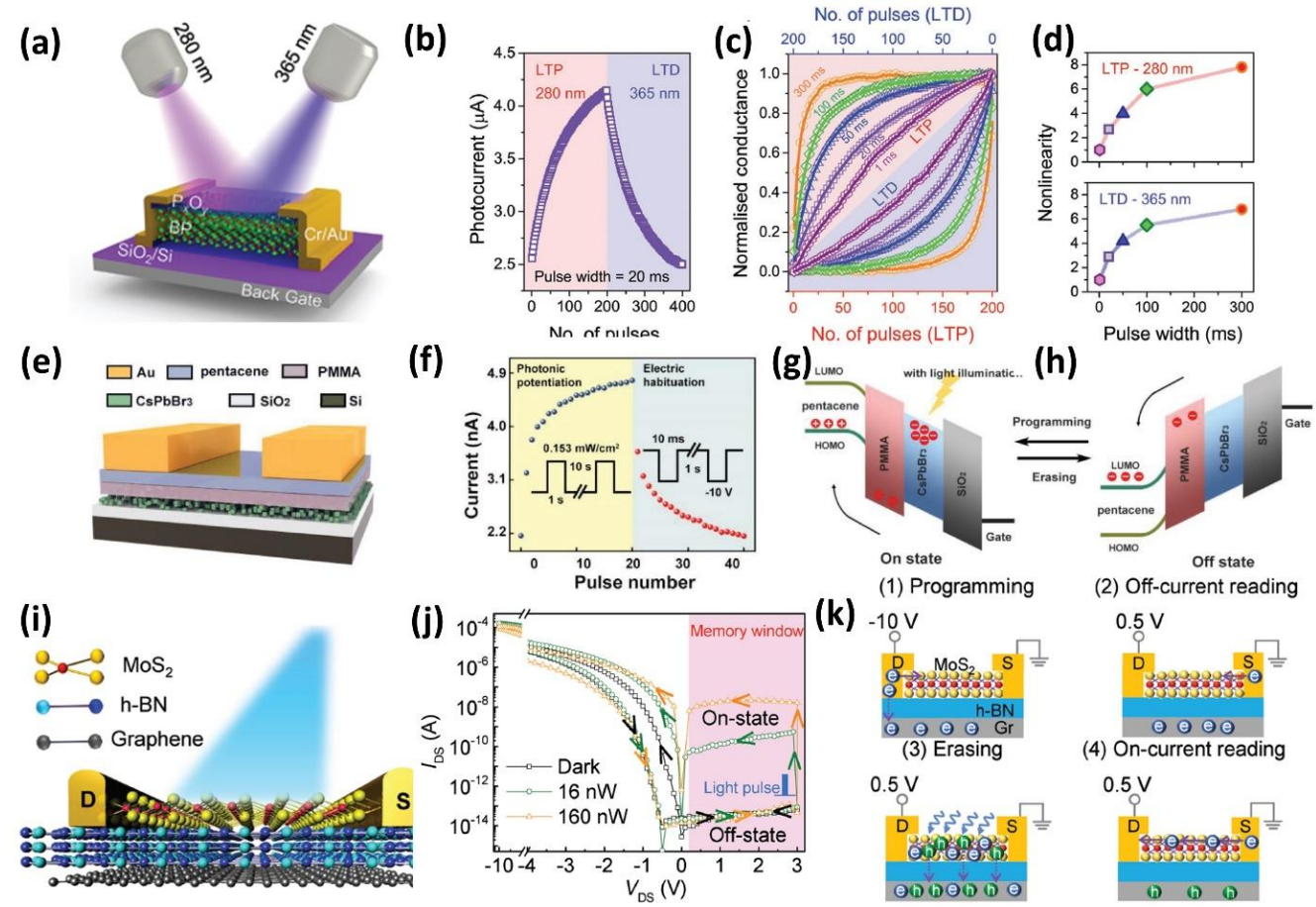


**Figure 5** Optoelectronics synapse UV light-based switching (a) schematic of BP memtransistor and its (b) optical LTP and LTD, (c) weight change on varying the light pulse width, and (d) the nonlinearity of the LTP and LTD at different wavelength and pulse width, adapted from [106]; (e)-(h) optically activated $CsPbBr_3$ memtransistor showcasing the potentiation and depression with ON state and OFF state band alignment,

adapted from [107]; (i)-(k) Optical response of two-terminal $MoS_2$ memristor synapse and its mechanisms; a higher light power increases the number of the generated electrons, adapted from [108].

Optical illumination can also induce or facilitate synaptic responses. [106] reported the optical stimulation of BP-based memtransistor using 280 nm and 365 nm UV light for potentiation and depression, respectively, as shown in Figure 5(a, b). The pulse width of the light stimuli can be adjusted to tune the linearity (Figs 5(c, d)). Yan et al. [107] suggested that light stimuli trigger charge trapping and release mechanisms in the $CsPbBr_2$ synapse (Figs. (e-h)). A similar mechanism can be found in the two-terminal planar Graphene/$MoS_2$ memristor synapse, where the light pulses induce photogenerated trapped electrons, thus enabling programming and erasing functions in the device (Figs 5 (i-k)) [108]. Metal oxide-based memristor synapses with point configurations can also produce photo-induced synaptic behavior, suggesting that the mechanism behind the increase or decrease in synaptic weight during light stimulation is due to the ionization and neutralization of oxygen vacancies in the oxide layer, respectively[109]. These devices require transparent electrodes, such as indium tin oxide (ITO), or a thin metal layer to enable light to penetrate the electrode into the oxide layer. It was found that various wavelengths, from ultraviolet to visible to infrared, can induce a photosynaptic response. Note that ultraviolet light is most commonly used to trigger the photosynaptic response owing to its high energy. Nevertheless, further investigations should be conducted to clarify or confirm the mechanism behind the photosynaptic response in devices with ITO electrodes. The high absorption of ITO in the UV region absorbs light before it can be transmitted into the oxides; thus, this brings us another idea that we may not necessarily expose the insulator layer if we can employ photosensitive electrode materials.

Table 1 summarises the performance metric of optomemristor and optomemtransistor synapses. Both optomemristor and optomemtransistor are suitable for visual AI systems due to their acceptable optical speed. Even though optomemtransistor synapses could perform better accuracy in conductance modulation and fast photoresponse, and high responsivity, their engineering complexity and integration may result in a higher fabrication cost than that of optomemristors. The use of perovskite or 2-dimensional materials tends to have better optical performance [110]; However, these materials are often sensitive to ambient, e.g. temperature, humidity, etc., that can pose challenges for practical use [111–113]. Table 2 summarises the common problems in developing 2-dimensional memristor synapses. A careful and tedious synthesis route is required to grow these materials, and slight process variation to the nanostructure or defects configuration could significantly affect their characteristics and performance.

Table 1. Typical performance metrics of optomemristor and optomemtransistor synapses in published literature.

| Performance metrics | Optomemristor | Optomemtransistor |
|---|---|---|
| Energy per optical spike | Sub-fJ to few fJ [114] | As low as 0.03 fJ per operation [115] |
| Programming speed (spike width, photocurrent decay) | Slow; seconds [116] | Fast; milliseconds [117] |
| Spectral selectivity | Good; can differentiate several bands of wavelength for multi-channel programming [118] | Excellent; can be designed to respond to a narrow band or specific wavelength via bandgap/channel engineering [119] |
| Optical responsivity | Low; 2.7 A/W [120] | High; 12 A/W [121] |

Table 2 Typical challenges in the development of 2-dimensional memristor synapses

| **Material system** | **Synaptic mechanism** | **Potential limitations** |
|---|---|---|
| Pt/$MoS_2$/Ti | Thermionic emission | Require uniform wafer-scale synthesis; interface trap states could cause variability; CMOS integration remains limited [122] |
| $MoTe_2$ | Ionic filament and phase transition | Phase instability might occur; sensitive to thermal and moisture; complex structure limits reproducibility [123] |
| Al/$WS_2$/$MoS_2$/ITO | Sulfur ions distribution at the interface | Short retention and endurance; random filament rupture-rejuvenation might limit large-scale integration maturity [124] |
| Ag/a-BN/Pt | Ag filament and Boron vacancy | Difficult to control the amorphous uniformity [125] |
| Au/Ti/h-BN/Au | Injection of Ti ions into the system | Switching variability; low endurance, tunneling current may be sensitive to film thickness; difficult to control the native defects in the atomic layers [126] |
| Al/$Ti_3C_2$:Ag/Pt | Aggregation of Ag ions around atomic vacancy | Trap-density variation can affect linearity [127] |

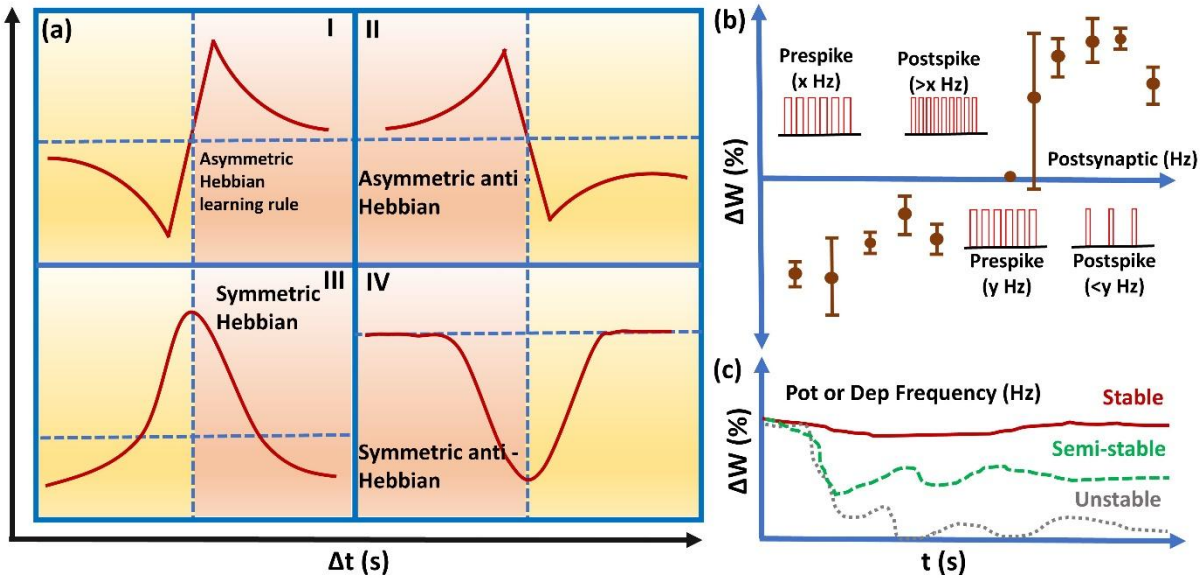


**Figure 6** (a) Hebbian learning rules for the symmetric and asymmetric responses, inspired by [128]; (b) schematic of SRDP programming procedure employing various frequencies for the pre- and post-spike response and (c) spike frequency of SRDP algorithm determines the synaptic weight, inspired by [129].

Remembering and forgetting are neuronal functions that neuromorphic computing systems try to mimic[130] and are deeply rooted in the learning rules that are used to modulate synaptic weights. A neurophysiologist, Donald Hebb, proposed that synaptic weight changes in biological neural networks may vary depending on the time gap between spikes, known as Hebbian learning rules (HLRs),[131] the most common of which are shown in Figure 6(a). Spike timing-dependent plasticity (STDP) and spike rate-dependent plasticity (SRDP) are frequently used as programming algorithms for implementing these rules.[132] STDP works on the relative timing between the pre-and postsynaptic spikes and influences the magnitude and direction of the weight update[133], whereas SRDP works on synaptic weight modulation by controlling the frequency of spiking neurons in the neural network, as illustrated in Figure 6(b). Although STDP is mostly reported in memristor synapse development owing to its practical implementation in decreasing or increasing the weight with precise timing of each spike, SRDP is closer to biological neuronal functions, where the spike rates control synaptic strength (Fig. 6(c)). Peng et al. [134] suggested that the SRDP is an efficient algorithm for high-accuracy unsupervised online learning. Ideally, s memristor synapse should be able to perform HLRs. Yi Li et al. [135] reported that a $Ge_2Sb_2Te_5$-based memristor synapse can exhibit all four rules with fast response time and low-power operation. However, most memristor synapse designs in the literature fail to demonstrate HRLs.

## 3. Hardware implementation and future scope

Recent advancements in memristor-based neuromorphic systems have enabled a wide spectrum of biomedical applications. These can be broadly categorized based on the nature of the signal they process—optical signals

for vision restoration, electrochemical signals for organ-level implants, and electrophysiological signals for wearable health monitoring. Additionally, these applications vary in their level of invasiveness, ranging from fully implantable devices to non-invasive wearable electronics. This section explores these applications in a structured manner to highlight the synergy between device-level innovations and system-level healthcare solutions.

### 4.1. Optical Signal Processing: Artificial Retinas and Vision Systems

Li et al. [136] proposed a $VO_2$-based ultraviolet nonvolatile synapse memtransistor actuated by 650, 532, 450, and 375 nm light sources. The synapse response of the memtransistor was used for neural network simulation to recognize handwritten numbers from the MNIST dataset. Figure 7(a) depicts the single-layer feedforward artificial neural network with 784 neuron input layers, 300 neuron hidden layers, and 10 neuron output layers presented in this network. The neural network was trained using the original MNIST test dataset, the RGB Gaussian noise dataset, and pre-processed data. The neural-network recognition accuracy was simulated as shown in Figure 7(b). The preprocessed dataset and the original MNIST test dataset achieved a recognition accuracy of 93%, whereas the dataset with RGB Gaussian noise achieved only 24% accuracy. The hardware implementation of a multilayer perceptron (MLP) neural network was realized by Bayat et al. by developing a 20 × 20 memristor synapse crossbar array based on $Pt/Al_2O_3/TiO_{2-x}/Ti/Pt$. The MLP consists of 16 input neurons, 10 hidden layer neurons, and four output neurons. The hardware-based neuron network was trained to classify 4 × 4 pixel patterns, shown in Figure 7(c). MNIST simulations based on memristor synapses typically achieve 90-95% accuracy, this performance is close to the accuracy achieved by traditional ANN software-based or other hardware, which could achieve up to 99% [137–139].

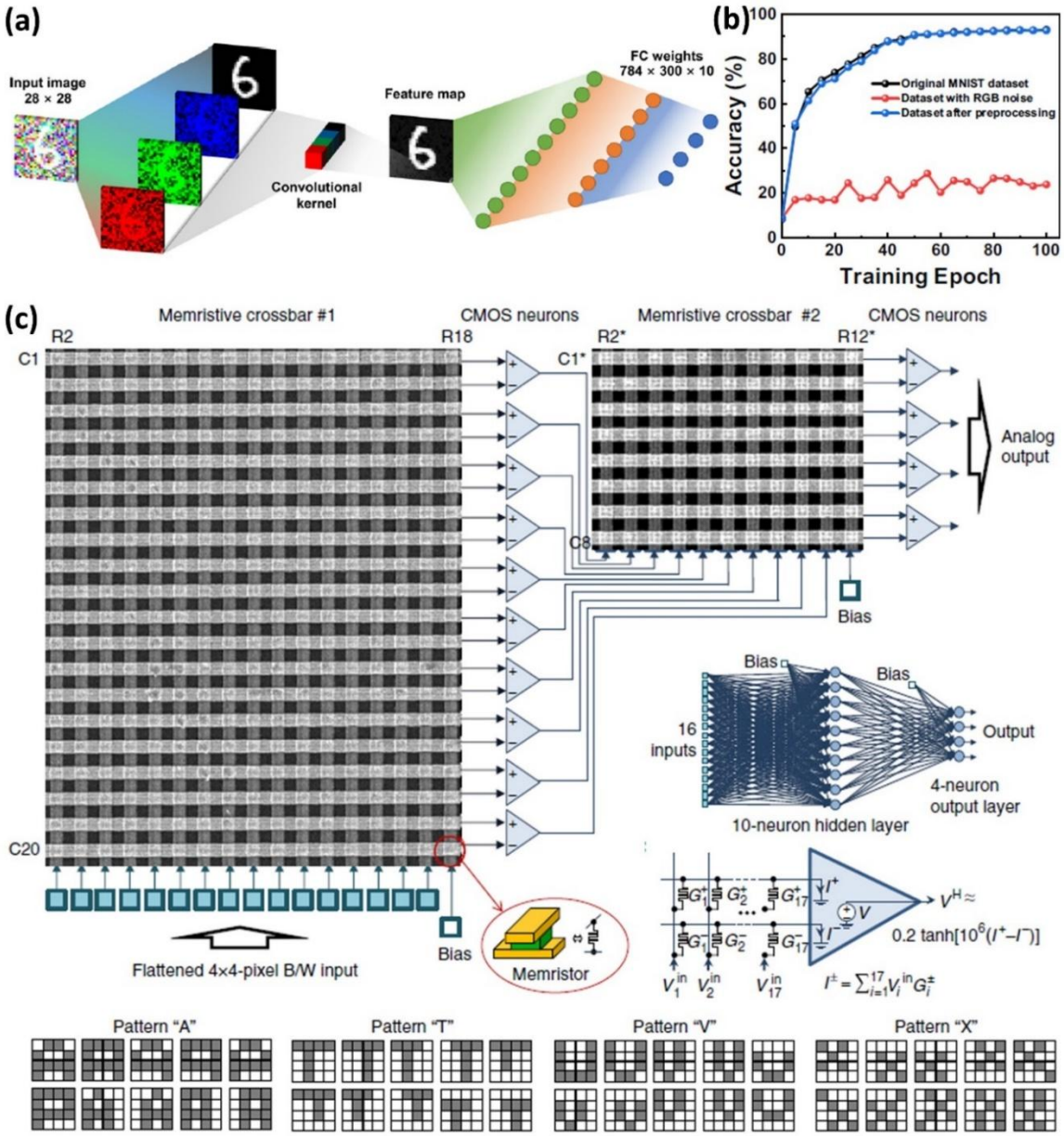


**Figure 7** (a) Neural network simulation of the MINST dataset handwritten numbers with and without RGB noise; (b) Recognition accuracy simulation of the neural network, adapted from [140]; and (c) High-density crossbar memory array for pattern recognition of various character patterns, adapted from [141].

In recent years, implantable electronics has grown rapidly owing to the significant leaps achieved by various artificial vision projects worldwide.[142,143] An artificial cognitive retina is based on a biocompatible synaptic array, such as a retinal implant, to transmit images efficiently into an optical neuronal signal. Retinal implants are directly connected to the optic nerve in the human brain. The main function of optical nerves in humans is to transmit visual data obtained from the rod and cone cells of the retina to neuronal signals of the human brain, which are then processed by the human brain as visual signals. Figure 8(a) depicts the location of the retinal implant connecting the optical nerves and retina[144]. The image from the camera was processed using a 3D stacked memristor array, which was then transferred to the retinal implant, as shown in Figures

8(b) and (c). The 3D stacked crossbar memristor that processes the image data into optical nerves as a visual impulse. The artificial neural network comprises two hidden-layer biocompatible synaptic memristor arrays for converting electronic data (image data) to chemical translation (optical nerves). The structure of the neural network is shown in Figure 8(d). The first layer of this neural network array was employed to capture a visual image and imprint it into an array of artificial neural networks.

The successive layer participates in the computations to further conduct the image processing operation for conversion into an optical signal. The primary function of the optical nerves is to convert images into signals. Retinal implants are expected to help improve the lives of patients with visual disabilities. Seo et al. proposed an artificial optic-neural synapse [145] that contributes to a significant enhancement in synthetic vision by directly interfacing an optical sensing device with a synaptic device connected to the visual cortex of the human brain. The structure of the integrated h-BN/$WSe_2$ (optical sensing) and $WSe_2$-based (synaptic device) is shown in Figure 8(e). The schematic also illustrates a symbolic representation of the connected device used in the study. The synaptic device is expected to be integrated into an array of neural networks for high-density integration and realization of artificial vision. The synaptic device response can be used in an optical neural network of RGB-based synaptic devices, and the neural network can achieve a peak recognition rate that exceeds 90% Figs. 8(f-g). While optical signal processing is crucial for restoring vision, similar neuromorphic architectures can be adapted for electrochemical interfaces in vital organ implants. These systems enable real-time monitoring and data interpretation directly within the body.

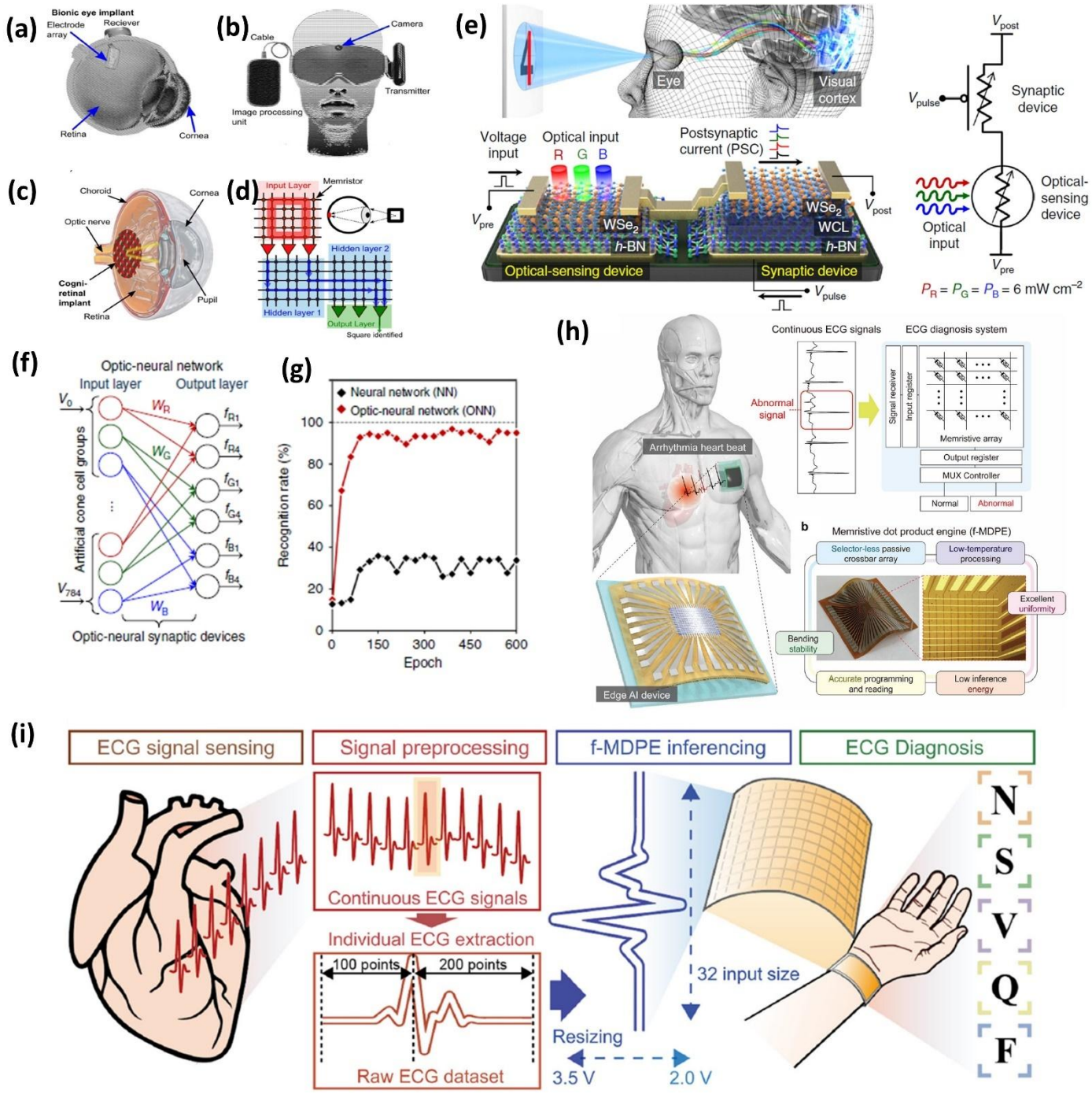


**Figure 8** (a-d) the concept of bionic retinal implant employing HNN, adapted from [144]; (e) integrated optical sensing and synaptic devices mimicking human optical nerve system and (f, g) RGB-based pattern recognition on optic-neural network, adapted from [146]; (h) human body-based various implantable electronics based on HNN and (i) vital parameters signal monitoring and diagnosis using memristor, adapted from [147].

### 4.2 Electrochemical Interfaces: Organ-Level Implants

In the future, memristive HNN cannot be restricted to bionic vision in the healthcare sector. HNN can be utilized in various applications, including heart, brain, ovarian, and lung implants, which are integrated with HNN, as depicted in Figs. 8(h-i). Artificial neural networks could dominate the future of biomedical applications, from heart implants to human brain implants. The future of biomedical analysis can be carried out using

heart or brain implants with sensors and an HNN to harness the data processing of the functionality of human organs. The HNN can also categorize patients' diseases using the data available from implants. Memristor synapses leveraging electrochemical interfaces are groundbreaking for organ-level implants, as they mimic biological synaptic function through ionic and redox-driven resistance switching, thus enabling ultra-low power and scalable architectures for physiological data processing [148]. Hardware neural networks incorporating memristor crossbar arrays can process multichannel physiological signals from these implants by applying learning algorithms like spike-timing and rate-dependent plasticity, supporting responsive closed-loop interventions directly at the organ interface. Implanting memristor synapses on the heart could facilitate real-time, energy-efficient detection of irregular cardiac activity by encoding and evaluating biosignals locally [149]. For brain implants, memristor synapses allow high-fidelity neural recording and the adaptive neuromodulation necessary for cognitive rehabilitation, via robust hardware neural network architectures; similarly, ovarian implants can exploit memristor synapses for continuous hormonal cycle monitoring, supporting both diagnosis and therapy through on-site computation with minimal energy overhead [150]. Another successful proof-of-hypothesis has also been reported for applications in functional monitoring of blood supply during liver transplantation [151]. This enables implantable electronics to perform real-time classification, anomaly detection, and feedback using integrated neuromorphic architectures proven to work in biomedical scenarios [152]. Beyond invasive implants, neuromorphic computing also supports non-invasive health monitoring through wearable electronics. These devices serve as external hubs, collecting and analyzing electrophysiological signals to provide continuous health insights.

### 4.3 Electrophysiological Monitoring: Wearable Sensors

Memristor synapses are revolutionizing non-invasive health monitoring through their potential integration in wearable electronics for ECG, $SpO_2$, heart rate, and blood pressure measurement [153]. Memristors can act as external hubs, continuously collecting electrophysiological signals and leveraging neuromorphic architectures for low-latency data processing [154]. The use of memristor-based in-memory computing within these wearables allows real-time analysis and pattern recognition directly at the sensor level, which is essential for anomaly detection such as arrhythmias or abnormal blood oxygenation [155]. By embedding computational functions into the storage medium, memristor synapses minimize energy consumption, enable scalable data fusion, and facilitate instant feedback to healthcare providers or end-users, ensuring timely intervention and improved patient outcomes [156]. Wearable electronics, which could act as a data hub to connect these implants, demonstrate the live functionality of the human organs and display the data using transparent

electronic eyeglasses or notify doctors. By using a similar approach, Ni et al. [157] proposed FeFET-based sensor data fusion technology using in-memory or neuromorphic memory computing. The FeFET-based neural network was designed to detect anomalies in the live ECG, $SpO_2$, heart rate, and blood pressure of human physiological signals. An in-memory logical array was designed to monitor and analyze human physiological signals. The in-memory correlation detection array is composed of multiple sensors that feed input to the correlation detection system, which is composed of a neural network of processing in the FeFET, and the anomaly detection scheme is used to detect anomalies in physiological signals.

## Conclusion

Resistive-synapse-based neuromorphic computing offers great potential for the development of next-generation AI hardware. The mimicking property of memristor synapses allows for the emulation of cognitive activity similar to that of the human brain, which exhibits STDP and SRDP. Research on highly dense crossbar array-based HNN shows a significant leap by realizing a simple perceptron neural network proposed to perform various applications based on recognition, classification, and detection. In the future, we anticipate that HNN-based systems will be used for broad healthcare solutions, including artificial vision, EEG signal monitoring, vital organ implants, disease detection, and physiological signal monitoring. Nevertheless, system-oriented benchmarking for memristor synapses should be developed to determine the minimum required synaptic performance for certain applications to ensure better synergy and a scientific leap between cleanroom engineers (device level) and system designers (system level). We also foresee further scientific progress in memristor synapses that mimic various types of neurons by controlling defects to behave like biological neurotransmitters. Therefore, the development of the next generation of memristor synapses will extend beyond elemental-to-molecular-level neural networks with massive interconnections close to the human brain.

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**Ethical Compliance:** All procedures performed in this study involving human participants were in accordance with the ethical standards of the institutional and/or national research committee and the 1964 Helsinki Declaration and its later amendments or comparable ethical standards.

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## Reference


1. Hou, W. Exploring the Horizon of AI Development: Navigating Constraints of Chips and Power in the Technological Landscape. *Applied and Computational Engineering* 2024, *77*, 177–182, doi:10.54254/2755-2721/77/20240688.

2. Yu, S. Neuro-Inspired Computing With Emerging Nonvolatile Memory. *Proceedings of the IEEE* 2018, *106*, 260–285, doi:10.1109/JPROC.2018.2790840.

3. Syed, G.S.; Le Gallo, M.; Sebastian, A. Non von Neumann Computing Concepts. In *Phase Change Materials-Based Photonic Computing*; Elsevier, 2024; pp. 11–35.

4. Dittmann, R.; Strachan, J.P. Redox-Based Memristive Devices for New Computing Paradigm. *APL Mater* 2019, *7*, doi:10.1063/1.5129101.

5. Zidan, M.A.; Strachan, J.P.; Lu, W.D. The Future of Electronics Based on Memristive Systems. *Nat Electron* 2018, *1*, 22–29, doi:10.1038/s41928-017-0006-8.

6. Yao, P.; Wu, H.; Gao, B.; Eryilmaz, S.B.; Huang, X.; Zhang, W.; Zhang, Q.; Deng, N.; Shi, L.; Wong, H.-S.P.; et al. Face Classification Using Electronic Synapses. *Nat Commun* 2017, *8*, 15199, doi:10.1038/ncomms15199.

7. Wu, W.; Wu, H.; Gao, B.; Deng, N.; Yu, S.; Qian, H. Improving Analog Switching in HfO x -Based Resistive Memory With a Thermal Enhanced Layer. *IEEE Electron Device Letters* 2017, *38*, 1019–1022, doi:10.1109/LED.2017.2719161.

8. Suri, M.; Bichler, O.; Querlioz, D.; Cueto, O.; Perniola, L.; Sousa, V.; Vuillaume, D.; Gamrat, C.; DeSalvo, B. Phase Change Memory as Synapse for Ultra-Dense Neuromorphic Systems: Application to Complex Visual Pattern Extraction. *Technical Digest - International Electron Devices Meeting, IEDM* 2011, 4.4.1-4.4.4, doi:10.1109/IEDM.2011.6131488.

9. Han, S.; Pool, J.; Tran, J.; Dally, W.J. Learning Both Weights and Connections for Efficient Neural Networks. *2018 IEEE Symposium on VLSI Technology* 2015, *28*, 29–30.

10. Kaneko, Y.; Nishitani, Y.; Ueda, M. Ferroelectric Artificial Synapses for Recognition of a Multishaded Image. *IEEE Trans Electron Devices* 2014, *61*, 2827–2833, doi:10.1109/TED.2014.2331707.

11. Burr, G.W.; Shelby, R.M.; Sebastian, A.; Kim, S.S.; Kim, S.S.; Sidler, S.; Virwani, K.; Ishii, M.; Narayanan, P.; Fumarola, A.; et al. Neuromorphic Computing Using Non-Volatile Memory. *Adv Phys X* 2017, *2*, 89–124, doi:10.1080/23746149.2016.1259585.

12. Prinzie, J.; Simanjuntak, F.M.; Leroux, P.; Prodromakis, T. Low-Power Electronic Technologies for Harsh Radiation Environments. *Nat Electron* 2021, *4*, 243–253, doi:10.1038/s41928-021-00562-4.

13. Prinzie, J.; Simanjuntak, F.M.; Leroux, P.; Prodromakis, T. Low-Power Electronic Technologies for Harsh Radiation Environments. *Nat Electron* 2021, *4*, 243–253, doi:10.1038/s41928-021-00562-4.

14. Salahuddin, S.; Ni, K.; Datta, S. The Era of Hyper-Scaling in Electronics. *Nat Electron* 2018, *1*, 442–450, doi:10.1038/s41928-018-0117-x.

15. Li, C.; Belkin, D.; Li, Y.; Yan, P.; Hu, M.; Ge, N.; Jiang, H.; Montgomery, E.; Lin, P.; Wang, Z.; et al. Efficient and Self-Adaptive in-Situ Learning in Multilayer Memristor Neural Networks. *Nat Commun* 2018, *9*, 7–14, doi:10.1038/s41467-018-04484-2.

16. Chandrasekaran, S.; Simanjuntak, F.M.; Saminathan, R.; Panda, D.; Tseng, T.-Y. Improving Linearity by Introducing Al in HfO 2 as a Memristor Synapse Device. *Nanotechnology* 2019, *30*, 445205, doi:10.1088/1361-6528/ab3480.

17. Kim, H.; Mahmoodi, M.R.; Nili, H.; Strukov, D.B. 4K-Memristor Analog-Grade Passive Crossbar Circuit. *Nat Commun* 2021, *12*, 1–11, doi:10.1038/s41467-021-25455-0.

18. Chandrasekaran, S.; Simanjuntak, F.M.; Panda, D.; Tseng, T.-Y. Enhanced Synaptic Linearity in ZnO-Based Invisible Memristive Synapse by Introducing Double Pulsing Scheme. *IEEE Trans Electron Devices* 2019, *66*, 4722–4726, doi:10.1109/TED.2019.2941764.

19. Prezioso, M.; Merrikh-Bayat, F.; Hoskins, B.D.; Adam, G.C.; Likharev, K.K.; Strukov, D.B. Training and Operation of an Integrated Neuromorphic Network Based on Metal-Oxide Memristors. *Nature* 2015, *521*, 61–64, doi:10.1038/nature14441.

20. Serb, A.; Bill, J.; Khiat, A.; Berdan, R.; Legenstein, R.; Prodromakis, T. Unsupervised Learning in Probabilistic Neural Networks with Multi-State Metal-Oxide Memristive Synapses. *Nat Commun* 2016, doi:10.1038/ncomms12611.

21. Gupta, I.; Serb, A.; Khiat, A.; Zeitler, R.; Vassanelli, S.; Prodromakis, T. Real-Time Encoding and Compression of Neuronal Spikes by Metal-Oxide Memristors. *Nat Commun* 2016, doi:10.1038/ncomms12805.

22. Moon, K.; Fumarola, A.; Sidler, S.; Jang, J.; Narayanan, P.; Shelby, R.M.; Burr, G.W.; Hwang, H. Bidirectional Non-Filamentary RRAM as an Analog Neuromorphic Synapse, Part I: Al/Mo/Pr0.7Ca0.3MnO3 Material Improvements and Device Measurements. *IEEE Journal of the Electron Devices Society* 2018, *6*, 146–155, doi:10.1109/JEDS.2017.2780275.

23. Gao, L.; Wang, I.-T.; Chen, P.-Y.; Vrudhula, S.; Seo, J.; Cao, Y.; Hou, T.-H.; Yu, S. Fully Parallel Write/Read in Resistive Synaptic Array for Accelerating on-Chip Learning. *Nanotechnology* 2015, *26*, 455204, doi:10.1088/0957-4484/26/45/455204.

24. Cüppers, F.; Menzel, S.; Bengel, C.; Hardtdegen, A.; Von Witzleben, M.; Böttger, U.; Waser, R.; Hoffmann-Eifert, S. Exploiting the Switching Dynamics of HfO2-Based ReRAM Devices for Reliable Analog Memristive Behavior. *APL Mater* 2019, *7*, doi:10.1063/1.5108654.

25. Li, Y.; Fuller, E.J.; Sugar, J.D.; Yoo, S.; Ashby, D.S.; Bennett, C.H.; Horton, R.D.; Bartsch, M.S.; Marinella, M.J.; Lu, W.D.; et al. Filament-Free Bulk Resistive Memory Enables Deterministic Analogue Switching. *Advanced Materials* 2020, *32*, 1–9, doi:10.1002/adma.202003984.

26. Choi, Y.J.; Kim, M.H.; Bang, S.; Kim, T.H.; Lee, D.K.; Hong, K.; Kim, C.S.; Kim, S.; Cho, S.; Park, B.G. Insertion of Ag Layer in TiN/SiNx/TiN RRAM and Its Effect on Filament Formation Modeled by Monte Carlo Simulation. *IEEE Access* 2020, *8*, 228720–228730, doi:10.1109/ACCESS.2020.3046300.

27. Wang, I.; Chang, C.; Chiu, L.; Chou, T.; Hou, T.-H. 3D Ta/TaO x /TiO 2 /Ti Synaptic Array and Linearity Tuning of Weight Update for Hardware Neural Network Applications. *Nanotechnology* 2016, *27*, 365204, doi:10.1088/0957-4484/27/36/365204.

28. Dalgaty, T.; Payvand, M.; Moro, F.; Ly, D.R.B.; Pebay-Peyroula, F.; Casas, J.; Indiveri, G.; Vianello, E. Hybrid Neuromorphic Circuits Exploiting Non-Conventional Properties of RRAM for Massively Parallel Local Plasticity Mechanisms. *APL Mater* 2019, *7*, doi:10.1063/1.5108663.

29. Rajasekaran, S.; Simanjuntak, F.M.; Chandrasekaran, S.; Panda, D.; Saleem, A.; Tseng, T.-Y. Flexible Ta 2 O 5 /WO 3 -Based Memristor Synapse for Wearable and Neuromorphic Applications. *IEEE Electron Device Letters* 2022, *43*, 9–12, doi:10.1109/LED.2021.3127489.

30. Jung, P.-Y.; Panda, D.; Chandrasekaran, S.; Rajasekaran, S.; Tseng, T.-Y. Enhanced Switching Properties in TaO x Memristors Using Diffusion Limiting Layer for Synaptic Learning. *IEEE Journal of the Electron Devices Society* 2020, *8*, 110–115, doi:10.1109/JEDS.2020.2966799.

31. Raúl Rojas; Ulf Hashagen “Nothing New Since von Neumann”: A Historian Looks at Computer Architecture, 1945–1995. In *The First Computers: History and Architectures*; MIT Press, 2002; pp. 195–217 ISBN 9780262282529.

32. Wijesinghe, P.; Ankit, A.; Sengupta, A.; Roy, K. An All-Memristor Deep Spiking Neural Computing System: A Step Toward Realizing the Low-Power Stochastic Brain. *IEEE Trans Emerg Top Comput Intell* 2018, *2*, 345–358, doi:10.1109/TETCI.2018.2829924.

33. Yuan, R.; Duan, Q.; Tiw, P.J.; Li, G.; Xiao, Z.; Jing, Z.; Yang, K.; Liu, C.; Ge, C.; Huang, R.; et al. A Calibratable Sensory Neuron Based on Epitaxial VO2 for Spike-Based Neuromorphic Multisensory System. *Nat Commun* 2022, *13*, 3973, doi:10.1038/s41467-022-31747-w.

34. Ostrau, C.; Klarhorst, C.; Thies, M.; Rückert, U. Benchmarking Neuromorphic Hardware and Its Energy Expenditure. *Front Neurosci* 2022, *16*, doi:10.3389/fnins.2022.873935.

35. Viebke, A.; Pllana, S. The Potential of the Intel (R) Xeon Phi for Supervised Deep Learning. In Proceedings of the 2015 IEEE 17th International Conference on High Performance Computing and Communications, 2015 IEEE 7th International Symposium on Cyberspace Safety and Security, and 2015 IEEE 12th International Conference on Embedded Software and Systems; IEEE, August 2015; pp. 758–765.

36. Lawson, G.; Sosonkina, M.; Shen, Y. Towards Modeling Energy Consumption of Xeon Phi. 2015.

37. Yang, J.; Xue, X.; Xu, X.; Wang, Q.; Jiang, H.; Yu, J.; Dong, D.; Zhang, F.; Lv, H.; Liu, M. 24.2 A 14nm-FinFET 1Mb Embedded 1T1R RRAM with a 0.022µm 2 Cell Size Using Self-Adaptive Delayed Termination and Multi-Cell Reference. In Proceedings of the 2021 IEEE International Solid- State Circuits Conference (ISSCC); IEEE, February 2021; pp. 336–338.

38. Barraud, S.; Ezzadeen, M.; Bosch, D.; Dubreuil, T.; Castellani, N.; Meli, V.; Hartmann, J.M.; Mouhdach, M.; Previtali, B.; Giraud, B.; et al. 3D RRAMs with Gate-All-Around Stacked Nanosheet Transistors for In-Memory-Computing. In Proceedings of the 2020 IEEE International Electron Devices Meeting (IEDM); IEEE, December 2020; pp. 29.5.1-29.5.4.

39. Li, H.; Li, K.-S.; Lin, C.-H.; Hsu, J.-L.; Chiu, W.-C.; Chen, M.-C.; Wu, T.-T.; Sohn, J.; Eryilmaz, S.B.; Shieh, J.-M.; et al. Four-Layer 3D Vertical RRAM Integrated with FinFET as a Versatile Computing Unit for Brain-Inspired Cognitive Information Processing. In Proceedings of the 2016 IEEE Symposium on VLSI Technology; IEEE, June 2016; Vol. 2016-Septe, pp. 1–2.

40. Wang, T.; Meng, J.; Chen, L.; Zhu, H.; Sun, Q.; Ding, S.; Bao, W.; Zhang, D.W. Flexible <scp>3D</Scp> Memristor Array for Binary Storage and Multi-states Neuromorphic Computing Applications. *InfoMat* 2021, *3*, 212–221, doi:10.1002/inf2.12158.

41. Banerjee, W.; Liu, Q.; Hwang, H. Engineering of Defects in Resistive Random Access Memory Devices. *J Appl Phys* 2020, *127*, 051101, doi:10.1063/1.5136264.

42. Zahoor, F.; Azni Zulkifli, T.Z.; Khanday, F.A. Resistive Random Access Memory (RRAM): An Overview of Materials, Switching Mechanism, Performance, Multilevel Cell (Mlc) Storage, Modeling, and Applications. *Nanoscale Res Lett* 2020, *15*, 90, doi:10.1186/s11671-020-03299-9.

43. Zhou, S.; Xing, Y.; Xu, Q.; Yan, Q.; Liu, P.; Wei, L.; Niu, W.; Li, F.; You, L.; Pu, Y. Planar Memristor and Artificial Synaptic Simulating Based on Two-Dimensional Layered Tungsten Oxychloride WO2Cl2. *Appl Phys Lett* 2023, *123*, doi:10.1063/5.0177899.

44. Li, Y.; Zhong, Y.; Zhang, J.; Xu, L.; Wang, Q.; Sun, H.; Tong, H.; Cheng, X.; Miao, X. Activity-Dependent Synaptic Plasticity of a Chalcogenide Electronic Synapse for Neuromorphic Systems. *Sci Rep* 2014, *4*, 4906, doi:10.1038/srep04906.

45. Kim, H.; Mahmoodi, M.R.; Nili, H.; Strukov, D.B. 4K-Memristor Analog-Grade Passive Crossbar Circuit. *Nat Commun* 2021, *12*, 1–11, doi:10.1038/s41467-021-25455-0.

46. Zhao, M.; Gao, B.; Tang, J.; Qian, H.; Wu, H. Reliability of Analog Resistive Switching Memory for Neuromorphic Computing. *Appl Phys Rev* 2020, *7*, 011301, doi:10.1063/1.5124915.

47. Tsuruoka, T.; Valov, I.; Tappertzhofen, S.; van den Hurk, J.; Hasegawa, T.; Waser, R.; Aono, M. Redox Reactions at Cu,Ag/Ta 2 O 5 Interfaces and the Effects of Ta 2 O 5 Film Density on the Forming Process in Atomic Switch Structures. *Adv Funct Mater* 2015, *25*, 6374–6381, doi:10.1002/adfm.201500853.

48. Yalishev, V.S.; Yuldashev, S.U.; Kim, Y.S.; Park, B.H. The Role of Zinc Vacancies in Bipolar Resistance Switching of Ag/ZnO/Pt Memory Structures. *Nanotechnology* 2012, *23*, 375201, doi:10.1088/0957-4484/23/37/375201.

49. Chung, Y.L.; Cheng, W.H.; Jeng, J.S.; Chen, W.C.; Jhan, S.A.; Chen, J.S. Joint Contributions of Ag Ions and Oxygen Vacancies to Conducting Filament Evolution of Ag/TaOx/Pt Memory Device. *J Appl Phys* 2014, *116*, 2012–2017, doi:10.1063/1.4899319.

50. Tada, M.; Sakamoto, T.; Banno, N.; Okamoto, K.; Miyamura, M.; Iguchi, N.; Hada, H. Improved Reliability and Switching Performance of Atom Switch by Using Ternary Cu-Alloy and RuTa Electrodes. In Proceedings of the 2012 International Electron Devices Meeting; IEEE, December 2012; pp. 29.8.1-29.8.4.

51. Liu, T.; Verma, M.; Kang, Y.; Orlowski, M. Volatile Resistive Switching in Cu/TaOx/δ-Cu/Pt Devices Volatile Resistive Switching in Cu/TaO x /d-Cu/Pt Devices. *Citation: Applied Physics Letters J. Appl. Phys* 2012, *101*, 1–5, doi:10.1063/1.4899319.

52. Chandrasekaran, S.; Simanjuntak, F.M.; Tsai, T.-L.; Lin, C.-A.; Tseng, T.-Y. Effect of Barrier Layer on Switching Polarity of ZrO2-Based Conducting-Bridge Random Access Memory. *Appl Phys Lett* 2017, *111*, 113108, doi:10.1063/1.5003622.

53. Wu, X.; Mei, S.; Bosman, M.; Raghavan, N.; Zhang, X.; Cha, D.; Li, K.; Pey, K.L. Evolution of Filament Formation in Ni/HfO 2 /SiO x /Si-Based RRAM Devices. *Adv Electron Mater* 2015, *1*, 1500130, doi:10.1002/aelm.201500130.

54. Belmonte, A.; Witters, T.; Covello, A.; Vereecke, G.; Franquet, A.; Spampinato, V.; Kundu, S.; Mao, M.; Hody, H.; Kar, G.S.; et al. Co Active Electrode Enhances CBRAM Performance and Scaling Potential. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM); IEEE, December 2019; Vol. 2019-Decem, pp. 35.8.1-35.8.4.

55. Qian, K.; Han, X.; Li, H.; Chen, T.; Lee, P.S. Uncovering the Indium Filament Revolution in Transparent Bipolar ITO/SiO x /ITO Resistive Switching Memories. *ACS Appl Mater Interfaces* 2020, *12*, 4579–4585, doi:10.1021/acsami.9b16325.

56. Sun, B.; Han, X.; Xu, R.; Qian, K. Uncovering the Indium Filament Formation and Dissolution in Transparent ITO/SiN x /ITO Resistive Random Access Memory. *ACS Appl Electron Mater* 2020, *2*, 1603–1608, doi:10.1021/acsaelm.0c00193.

57. Qian, K.; Tay, R.Y.; Lin, M.-F.; Chen, J.; Li, H.; Lin, J.; Wang, J.; Cai, G.; Nguyen, V.C.; Teo, E.H.T.; et al. Direct Observation of Indium Conductive Filaments in Transparent, Flexible, and Transferable Resistive Switching Memory. *ACS Nano* 2017, *11*, 1712–1718, doi:10.1021/acsnano.6b07577.

58. Rajasekaran, S.; Simanjuntak, F.M.; Panda, D.; Chandrasekaran, S.; Aluguri, R.; Saleem, A.; Tseng, T.-Y. Fast, Highly Flexible, and Transparent TaO x -Based Environmentally Robust Memristors for Wearable and Aerospace Applications. *ACS Appl Electron Mater* 2020, *2*, 3131–3140, doi:10.1021/acsaelm.0c00441.

59. Shi, Y.; Nguyen, L.; Oh, S.; Liu, X.; Koushan, F.; Jameson, J.R.; Kuzum, D. Neuroinspired Unsupervised Learning and Pruning with Subquantum CBRAM Arrays. *Nat Commun* 2018, *9*, 5312, doi:10.1038/s41467-018-07682-0.

60. Wang, H.; Yan, X.; Wang, S.; Lu, N. High-Stability Memristive Devices Based on Pd Conductive Filaments and Its Applications in Neuromorphic Computing. *ACS Appl Mater Interfaces* 2021, *13*, 17844–17851, doi:10.1021/acsami.1c01076.

61. Cooper, D.; Baeumer, C.; Bernier, N.; Marchewka, A.; La Torre, C.; Dunin-Borkowski, R.E.; Menzel, S.; Waser, R.; Dittmann, R. Anomalous Resistance Hysteresis in Oxide ReRAM: Oxygen Evolution and Reincorporation Revealed by In Situ TEM. *Advanced Materials* 2017, *29*, 1–8, doi:10.1002/adma.201700212.

62. Kim, M.J.; Jeon, D.S.; Park, J.H.; Kim, T.G. Bipolar Resistive Switching Characteristics in Tantalum Nitride-Based Resistive Random Access Memory Devices. *Appl Phys Lett* 2015, *106*, 3–7, doi:10.1063/1.4921349.

63. Kim, H.-D.; Yun, M.J.; Kim, T.G. Forming-Free Resistive Switching Characteristics and Improved Reliability in Sub-Stoichiometric NbN\n \n X\n \n Films. *physica status solidi (RRL) - Rapid Research Letters* 2015, *9999*, n/a-n/a, doi:10.1002/pssr.201510022.

64. Chang, Y.-C.; Wang, Y.-H. Resistive Switching Behavior in Gelatin Thin Films for Nonvolatile Memory Application. *ACS Appl Mater Inter* 2014, *6*, 5413–5421, doi:10.1021/am500815n.

65. Kang, Y.; Liu, T.; Potnis, T.; Orlowski, M.K. Composite Cu/Vo and Vo/Cu Nanofilaments in Cu/Ta 2O5/Pt Devices. *ECS Solid State Letters* 2013, *2*, doi:10.1149/2.004307ssl.

66. Chang, C.F.; Chen, J.Y.; Huang, C.W.; Chiu, C.H.; Lin, T.Y.; Yeh, P.H.; Wu, W.W. Direct Observation of Dual-Filament Switching Behaviors in Ta2O5-Based Memristors. *Small* 2017, *13*, 1–7, doi:10.1002/smll.201603116.

67. Sun, H.; Liu, Q.; Li, C.; Long, S.; Lv, H.; Bi, C.; Huo, Z.; Li, L.; Liu, M. Direct Observation of Conversion Between Threshold Switching and Memory Switching Induced by Conductive Filament Morphology. *Adv Funct Mater* 2014, *24*, 5679–5686, doi:10.1002/adfm.201401304.

68. Peng, C.-N.; Wang, C.-W.; Chan, T.-C.; Chang, W.-Y.; Wang, Y.-C.; Tsai, H.-W.; Wu, W.-W.; Chen, L.-J.; Chueh, Y.-L. Resistive Switching of Au/ZnO/Au Resistive Memory: An in Situ Observation of Conductive Bridge Formation. *Nanoscale Res Lett* 2012, *7*, 559, doi:10.1186/1556-276X-7-559.

69. Tian, X.; Wang, L.; Wei, J.; Yang, S.; Wang, W.; Xu, Z.; Bai, X. Filament Growth Dynamics in Solid Electrolyte-Based Resistive Memories Revealed by in Situ TEM. *Nano Res* 2014, *7*, 1065–1072, doi:10.1007/s12274-014-0469-0.

70. Yang, Y.; Gao, P.; Li, L.; Pan, X.; Tappertzhofen, S.; Choi, S.; Waser, R.; Valov, I.; Lu, W.D. Electrochemical Dynamics of Nanoscale Metallic Inclusions in Dielectrics. *Nat Commun* 2014, *5*, 4232, doi:10.1038/ncomms5232.

71. Waser, R.; Dittmann, R.; Staikov, G.; Szot, K. Redox-Based Resistive Switching Memories - Nanoionic Mechanisms, Prospects, and Challenges. *Advanced Materials* 2009, *21*, 2632–2663, doi:10.1002/adma.200900375.

72. Zhang, Z.; Gao, B.; Fang, Z.; Wang, X.; Tang, Y.; Sohn, J.; Wong, H.-S.P.; Wong, S.S.; Lo, G.-Q. All-Metal-Nitride RRAM Devices. *IEEE Electron Device Letters* 2015, *36*, 29–31, doi:10.1109/LED.2014.2367542.

73. Yang Chai; Yi Wu; Takei, K.; Hong-Yu Chen; Shimeng Yu; Chan, P.C.H.; Javey, A.; Wong, H.-S.P. Resistive Switching of Carbon-Based RRAM with CNT Electrodes for Ultra-Dense Memory. In Proceedings of the 2010 International Electron Devices Meeting; IEEE, December 2010; pp. 9.3.1-9.3.4.

74. Russo, P.; Xiao, M.; Zhou, N.Y. Electrochemical Oxidation Induced Multi-Level Memory in Carbon-Based Resistive Switching Devices. *Sci Rep* 2019, *9*, 1–10, doi:10.1038/s41598-018-38249-0.

75. Zhang, Y.; Mao, G.-Q.; Zhao, X.; Li, Y.; Zhang, M.; Wu, Z.; Wu, W.; Sun, H.; Guo, Y.; Wang, L.; et al. Evolution of the Conductive Filament System in HfO2-Based Memristors Observed by Direct Atomic-Scale Imaging. *Nat Commun* 2021, *12*, 7232, doi:10.1038/s41467-021-27575-z.

76. Yao, J.; Zhong, L.; Natelson, D.; Tour, J.M. In Situ Imaging of the Conducting Filament in a Silicon Oxide Resistive Switch. *Sci Rep* 2012, *2*, 242, doi:10.1038/srep00242.

77. Cooper, D.; Baeumer, C.; Bernier, N.; Marchewka, A.; La Torre, C.; Dunin-Borkowski, R.E.; Menzel, S.; Waser, R.; Dittmann, R. Anomalous Resistance Hysteresis in Oxide ReRAM: Oxygen Evolution and Reincorporation Revealed by In Situ TEM. *Advanced Materials* 2017, *29*, doi:10.1002/adma.201700212.

78. Liu, T.; Verma, M.; Kang, Y.; Orlowski, M.K. Coexistence of Bipolar and Unipolar Switching of Cu and Oxygen Vacancy Nanofilaments in Cu/TaOx/Pt Resistive Devices. *ECS Solid State Letters* 2012, *1*, Q11–Q13, doi:10.1149/2.012201ssl.

79. Chandrasekaran, S.; Simanjuntak, F.M.; Tsai, T.-L.; Lin, C.-A.; Tseng, T.-Y. Effect of Barrier Layer on Switching Polarity of ZrO2-Based Conducting-Bridge Random Access Memory. *Appl Phys Lett* 2017, *111*, 113108, doi:10.1063/1.5003622.

80. Huang, C.-H.; Huang, J.-S.; Lai, C.-C.; Huang, H.-W.; Lin, S.-J.; Chueh, Y.-L. Manipulated Transformation of Filamentary and Homogeneous Resistive Switching on ZnO Thin Film Memristor with Controllable Multistate. *ACS Appl Mater Interfaces* 2013, *5*, 6017–6023, doi:10.1021/am4007287.

81. Tambunan, O.T.; Parwanta, K.J.; Acharya, S.K.; Lee, B.W.; Jung, C.U.; Kim, Y.S.; Park, B.H.; Jeong, H.; Park, J.Y.; Cho, M.R.; et al. Resistance Switching in Epitaxial SrCoOx Thin Films. *Appl Phys Lett* 2014, *105*, doi:10.1063/1.4893323.

82. Yao, L.; Inkinen, S.; van Dijken, S. Direct Observation of Oxygen Vacancy-Driven Structural and Resistive Phase Transitions in La2/3Sr1/3MnO3. *Nat Commun* 2017, *8*, 14544, doi:10.1038/ncomms14544.

83. Kim, H.G.; Nallagatla, V.R.; Kwon, D.H.; Jung, C.U.; Kim, M. In Situ Observations of Topotactic Phase Transitions in a Ferrite Memristor. *J Appl Phys* 2020, *128*, doi:10.1063/5.0015902.

84. Wong, H.-S.P.; Raoux, S.; Kim, S.; Liang, J.; Reifenberg, J.P.; Rajendran, B.; Asheghi, M.; Goodson, K.E. Phase Change Memory. *Proceedings of the IEEE* 2010, *98*, 2201–2227, doi:10.1109/JPROC.2010.2070050.

85. Wang, L.; Liao, W.; Wong, S.L.; Yu, Z.G.; Li, S.; Lim, Y.; Feng, X.; Tan, W.C.; Huang, X.; Chen, L.; et al. Artificial Synapses Based on Multiterminal Memtransistors for Neuromorphic Application. *Adv Funct Mater* 2019, *29*, 1901106, doi:10.1002/adfm.201901106.

86. Sangwan, V.K.; Lee, H.-S.; Bergeron, H.; Balla, I.; Beck, M.E.; Chen, K.-S.; Hersam, M.C. Multi-Terminal Memtransistors from Polycrystalline Monolayer Molybdenum Disulfide. *Nature* 2018, *554*, 500–504, doi:10.1038/nature25747.

87. Yan, X.; Qian, J.H.; Sangwan, V.K.; Hersam, M.C. Progress and Challenges for Memtransistors in Neuromorphic Circuits and Systems. *Advanced Materials* 2022, *34*, 2108025, doi:10.1002/adma.202108025.

88. Berdan, R.; Vasilaki, E.; Khiat, A.; Indiveri, G.; Serb, A.; Prodromakis, T. Emulating Short-Term Synaptic Dynamics with Memristive Devices. *Sci Rep* 2016, *6*, 1–9, doi:10.1038/srep18639.

89. Löwel, S.; Singer, W. Selection of Intrinsic Horizontal Connections in the Visual Cortex by Correlated Neuronal Activity. *Science (1979)* 1992, *255*, 209–212, doi:10.1126/science.1372754.

90. Ringo, J.L. Neuronal Interconnection as a Function of Brain Size. *Brain Behav Evol* 1991, *38*, 1–6, doi:10.1159/000114375.

91. Neveu, D.; Zucker, R.S. Long-Lasting Potentiation and Depression without Presynaptic Activity. *J Neurophysiol* 1996, *75*, 2157–2160, doi:10.1152/jn.1996.75.5.2157.

92. Bliss, T.V.P.; Cooke, S.F. Long-Term Potentiation and Long-Term Depression: A Clinical Perspective. *Clinics (Sao Paulo)* 2011, *66 Suppl 1*, 3–17, doi:10.1590/S1807-59322011001300002.

93. Ohno, T.; Hasegawa, T.; Tsuruoka, T.; Terabe, K.; Gimzewski, J.K.; Aono, M. Short-Term Plasticity and Long-Term Potentiation Mimicked in Single Inorganic Synapses. *Nat Mater* 2011, *10*, 591–595, doi:10.1038/nmat3054.

94. Wu, C.-H.; Lin, S.-K.; Pan, C.-H.; Chen, P.-H.; Lin, W.-Y.; Chang, T.-C.; Tsai, T.-M.; Xu, Y.-L.; Shih, C.-C.; Lin, Y.-S.; et al. Analyzing Electric Field Effect by Applying an Ultra-Short Time Pulse Condition in Hafnium Oxide-Based RRAM. *IEEE Electron Device Letters* 2018, *39*, 1163–1166, doi:10.1109/LED.2018.2849507.

95. Hennig, M.H. Theoretical Models of Synaptic Short Term Plasticity. *Front Comput Neurosci* 2013, *7*, 1–10, doi:10.3389/fncom.2013.00045.

96. Kurenkov, A.; DuttaGupta, S.; Zhang, C.; Fukami, S.; Horio, Y.; Ohno, H. Artificial Neuron and Synapse Realized in an Antiferromagnet/Ferromagnet Heterostructure Using Dynamics of Spin–Orbit Torque Switching. *Advanced Materials* 2019, *31*, 1900636, doi:10.1002/adma.201900636.

97. Ohno, T.; Hasegawa, T.; Tsuruoka, T.; Terabe, K.; Gimzewski, J.K.; Aono, M. Short-Term Plasticity and Long-Term Potentiation Mimicked in Single Inorganic Synapses. *Nat Mater* 2011, *10*, 591–595, doi:10.1038/nmat3054.

98. Simanjuntak, F.M.; Hsu, C.-L.; Abbey, T.; Chang, L.-Y.; Rajasekaran, S.; Prodromakis, T.; Tseng, T.-Y. Conduction Channel Configuration Controlled Digital and Analog Response in TiO 2 -Based Inorganic Memristive Artificial Synapses. *APL Mater* 2021, *9*, 121103, doi:10.1063/5.0067302.

99. Simanjuntak, F.M.; Ohno, T.; Chandrasekaran, S.; Tseng, T.-Y.; Samukawa, S. Neutral Oxygen Irradiation Enhanced Forming-Less ZnO-Based Transparent Analog Memristor Devices for Neuromorphic Computing Applications. *Nanotechnology* 2020, *31*, 26LT01, doi:10.1088/1361-6528/ab7fcf.

100. Chandrasekaran, S.; Simanjuntak, F.M.; Panda, D.; Tseng, T. Enhanced Synaptic Linearity in ZnO-Based Invisible Memristive Synapse by Introducing Double Pulsing Scheme. *IEEE Trans Electron Devices* 2019, *66*, 4722–4726, doi:10.1109/TED.2019.2941764.

101. Juliano, H.; Limantoro, S.E.; Simanjuntak, F.M.; Tseng, T.-Y. Metal Interdiffusion Enhanced WOx/CuOx Heterojunction Optoelectronic Memristive Synapses for Face Recognition Application. *APL Mater* 2025, *13*, doi:10.1063/5.0252709.

102. Simanjuntak, F.M.; Chandrasekaran, S.; Lin, C.-C.; Tseng, T.-Y. ZnO2/ZnO Bilayer Switching Film for Making Fully Transparent Analog Memristor Devices. *APL Mater* 2019, *7*, doi:10.1063/1.5092991.

103. Chen, P.-Y.; Lin, B.; Wang, I.-T.; Hou, T.-H.; Ye, J.; Vrudhula, S.; Seo, J.; Cao, Y.; Yu, S. Mitigating Effects of Non-Ideal Synaptic Device Characteristics for on-Chip Learning. In Proceedings of the 2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD); IEEE, November 2015; pp. 194–199.

104. Lastras-Montaño, M.A.; Cheng, K.-T. Resistive Random-Access Memory Based on Ratioed Memristors. *Nat Electron* 2018, *1*, 466–472, doi:10.1038/s41928-018-0115-z.

105. Gao, B.; Bi, Y.; Chen, H.-Y.; Liu, R.; Huang, P.; Chen, B.; Liu, L.; Liu, X.; Yu, S.; Wong, H.-S.P.; et al. Ultra-Low-Energy Three-Dimensional Oxide-Based Electronic Synapses for Implementation of Robust High-Accuracy Neuromorphic Computation Systems. *ACS Nano* 2014, *8*, 6998–7004, doi:10.1021/nn501824r.

106. Ahmed, T.; Tahir, M.; Low, M.X.; Ren, Y.; Tawfik, S.A.; Mayes, E.L.H.; Kuriakose, S.; Nawaz, S.; Spencer, M.J.S.; Chen, H.; et al. Fully Light-Controlled Memory and Neuromorphic Computation in Layered Black Phosphorus. *Advanced Materials* 2021, *33*, 2004207, doi:10.1002/adma.202004207.

107. Wang, Y.; Lv, Z.; Chen, J.; Wang, Z.; Zhou, Y.; Zhou, L.; Chen, X.; Han, S.-T. Photonic Synapses Based on Inorganic Perovskite Quantum Dots for Neuromorphic Computing. *Advanced Materials* 2018, *30*, 1802883, doi:10.1002/adma.201802883.

108. Tran, M.D.; Kim, H.; Kim, J.S.; Doan, M.H.; Chau, T.K.; Vu, Q.A.; Kim, J.-H.; Lee, Y.H. Two-Terminal Multibit Optical Memory via van Der Waals Heterostructure. *Advanced Materials* 2019, *31*, 1807075, doi:10.1002/adma.201807075.

109. Pereira, M.E.; Martins, R.; Fortunato, E.; Barquinha, P.; Kiazadeh, A. Recent Progress in Optoelectronic Memristors for Neuromorphic and In-Memory Computation. *Neuromorphic Computing and Engineering* 2023, *3*, doi:10.1088/2634-4386/acd4e2.

110. Vashishtha, P.; Kofler, C.; Verma, A.K.; Giridhar, S.P.; Tollerud, J.O.; Dissanayake, N.S.L.; Gupta, T.; Sehrawat, M.; Aggarwal, V.; Mayes, E.L.H.; et al. Epitaxial Interface-Driven Photoresponse Enhancement in Monolayer WS 2 –MoS 2 Lateral Heterostructures. *Adv Funct Mater* 2025, doi:10.1002/adfm.202512962.

111. Prajapat, P.; Vashishtha, P.; Gupta, G. High-Temperature Resilient Neuromorphic Device Based on Optically Configured Monolayer MoS 2 for Cognitive Computing. *Small* 2025, *21*, doi:10.1002/smll.202411596.

112. Zhang, X.; Zhao, X.; Shan, X.; Tian, Q.; Wang, Z.; Lin, Y.; Xu, H.; Liu, Y. Humidity Effect on Resistive Switching Characteristics of the CH 3 NH 3 PbI 3 Memristor. *ACS Appl Mater Interfaces* 2021, *13*, 28555–28563, doi:10.1021/acsami.1c05590.

113. Haghshenas Gorgabi, F.; Morant-Miñana, M.C.; Zafarkish, H.; Abbaszadeh, D.; Asadi, K. Graphene Memristors Based on Humidity-Mediated Reduction of Graphene Oxide. *J Mater Chem C Mater* 2023, *11*, 1690–1695, doi:10.1039/D2TC04632F.

114. Xia, Z.; Sun, X.; Wang, Z.; Meng, J.; Jin, B.; Wang, T. Low-Power Memristor for Neuromorphic Computing: From Materials to Applications. *Nanomicro Lett* 2025, *17*, 217, doi:10.1007/s40820-025-01705-4.

115. Wu, Y.; Chang, A.; Chen, W.; Ercan, E.; Weng, Y.; Lin, B.; Liu, C.; Lin, Y.; Chen, W. High-Performance Synaptic Phototransistor Using A Photoactive Self-Assembled Layer toward Ultralow Energy Consumption. *Adv Opt Mater* 2024, *12*, doi:10.1002/adom.202302040.

116. Shrivastava, S.; Juliano, H.; Uong, P.A.L.; Tseng, T.-Y. Recent Developments on Neuromorphic Optoelectronic Memristors Based on Metal Oxide Semiconductors: A Review. *APL Electronic Devices* 2025, *1*, doi:10.1063/5.0275306.

117. Islam, M.M.; Dev, D.; Krishnaprasad, A.; Tetard, L.; Roy, T. Optoelectronic Synapse Using Monolayer MoS2 Field Effect Transistors. *Sci Rep* 2020, *10*, 21870, doi:10.1038/s41598-020-78767-4.

118. Shrivastava, S.; Limantoro, S.E.; Juliano, H.; Tseng, T.-Y. Perovskite Oxide Based Transparent Neuromorphic Photoelectric Memristor for Artificial Ocular System. *APL Mater* 2025, *13*, doi:10.1063/5.0261193.

119. Xie, P.; Li, D.; Yip, S.; Ho, J.C. Emerging Optoelectronic Artificial Synapses and Memristors Based on Low-Dimensional Nanomaterials. *Appl Phys Rev* 2024, *11*, doi:10.1063/5.0173547.

120. Dun, G.; Li, Y.; Zhang, H.; Wu, F.; Tan, X.; Qin, K.; He, Y.; Wang, Z.; Wang, Y.; Lu, T.; et al. All-in-one Perovskite Memristor with Tunable Photoresponsivity. *InfoMat* 2025, *7*, doi:10.1002/inf2.12619.

121. Islam, M.M.; Dev, D.; Krishnaprasad, A.; Tetard, L.; Roy, T. Optoelectronic Synapse Using Monolayer MoS2 Field Effect Transistors. *Sci Rep* 2020, *10*, 21870, doi:10.1038/s41598-020-78767-4.

122. Tang, B.; Veluri, H.; Li, Y.; Yu, Z.G.; Waqar, M.; Leong, J.F.; Sivan, M.; Zamburg, E.; Zhang, Y.-W.; Wang, J.; et al. Wafer-Scale Solution-Processed 2D Material Analog Resistive Memory Array for Memory-Based Computing. *Nat Commun* 2022, *13*, 3037, doi:10.1038/s41467-022-30519-w.

123. Khan, R.; Rehman, N.U.; Kalluri, S.; Elumalai, S.; Saritha, A.; Fakhar-e-alam, M.; Ikram, M.; Abdullaev, S.; Rahman, N.; Sangaraju, S. 2D MoTe 2 Memristors for Energy-Efficient Artificial Synapses and Neuromorphic Applications. *Nanoscale* 2025, *17*, 13174–13206, doi:10.1039/D5NR01509J.

124. Zhang, W.; Gao, H.; Deng, C.; Lv, T.; Hu, S.; Wu, H.; Xue, S.; Tao, Y.; Deng, L.; Xiong, W. An Ultrathin Memristor Based on a Two-Dimensional WS 2 /MoS 2 Heterojunction. *Nanoscale* 2021, *13*, 11497–11504, doi:10.1039/D1NR01683K.

125. Khot, A.C.; Dongale, T.D.; Nirmal, K.A.; Sung, J.H.; Lee, H.J.; Nikam, R.D.; Kim, T.G. Amorphous Boron Nitride Memristive Device for High-Density Memory and Neuromorphic Computing Applications. *ACS Appl Mater Interfaces* 2022, *14*, 10546–10557, doi:10.1021/acsami.1c23268.

126. Roldan, J.B.; Maldonado, D.; Aguilera-Pedregosa, C.; Moreno, E.; Aguirre, F.; Romero-Zaliz, R.; García-Vico, A.M.; Shen, Y.; Lanza, M. Spiking Neural Networks Based on Two-Dimensional Materials. *NPJ 2D Mater Appl* 2022, *6*, 63, doi:10.1038/s41699-022-00341-5.

127. Wang, K.; Chen, J.; Yan, X. MXene Ti3C2 Memristor for Neuromorphic Behavior and Decimal Arithmetic Operation Applications. *Nano Energy* 2021, *79*, 105453, doi:10.1016/j.nanoen.2020.105453.

128. Buchanan, K.A. The Activity Requirements for Spike Timing-Dependent Plasticity in the Hippocampus. *Front Synaptic Neurosci* 2010, *2*, doi:10.3389/fnsyn.2010.00011.

129. Li, Y.; Zhong, Y.; Zhang, J.; Xu, L.; Wang, Q.; Sun, H.; Tong, H.; Cheng, X.; Miao, X. Activity-Dependent Synaptic Plasticity of a Chalcogenide Electronic Synapse for Neuromorphic Systems. *Sci Rep* 2014, *4*, 4906, doi:10.1038/srep04906.

130. Caporale, N.; Dan, Y. Spike Timing–Dependent Plasticity: A Hebbian Learning Rule. *Annu Rev Neurosci* 2008, *31*, 25–46, doi:10.1146/annurev.neuro.31.060407.125639.

131. Hebb, D.O. *The Organization of Behavior; A Neuropsychological Theory*; John Wiley & Sons, Inc., Chapman & Hall,Ltd., 1949;

132. Saïghi, S.; Mayr, C.G.; Serrano-Gotarredona, T.; Schmidt, H.; Lecerf, G.; Tomas, J.; Grollier, J.; Boyn, S.; Vincent, A.F.; Querlioz, D.; et al. Plasticity in Memristive Devices for Spiking Neural Networks. *Front Neurosci* 2015, *9*, doi:10.3389/fnins.2015.00051.

133. Bi, G.; Poo, M. Synaptic Modification by Correlated Activity: Hebb's Postulate Revisited. *Annu Rev Neurosci* 2001, *24*, 139–166, doi:10.1146/annurev.neuro.24.1.139.

134. Huang, P.; Li, Z.; Dong, Z.; Han, R.; Zhou, Z.; Zhu, D.; Liu, L.; Liu, X.; Kang, J. Binary Resistive-Switching-Device-Based Electronic Synapse with Spike-Rate-Dependent Plasticity for Online Learning. *ACS Appl Electron Mater* 2019, *1*, 845–853, doi:10.1021/acsaelm.9b00011.

135. Li, Y.; Zhong, Y.; Xu, L.; Zhang, J.; Xu, X.; Sun, H.; Miao, X. Ultrafast Synaptic Events in a Chalcogenide Memristor. *Sci Rep* 2013, *3*, 1619, doi:10.1038/srep01619.

136. Li, G.; Xie, D.; Zhong, H.; Zhang, Z.; Fu, X.; Zhou, Q.; Li, Q.; Ni, H.; Wang, J.; Guo, E.; et al. Photo-Induced Non-Volatile VO2 Phase Transition for Neuromorphic Ultraviolet Sensors. *Nat Commun* 2022, *13*, 1729, doi:10.1038/s41467-022-29456-5.

137. Javanshir, A.; Nguyen, T.T.; Mahmud, M.A.P.; Kouzani, A.Z. Advancements in Algorithms and Neuromorphic Hardware for Spiking Neural Networks. *Neural Comput* 2022, *34*, 1289–1328, doi:10.1162/neco_a_01499.

138. Iyer, L.R.; Chua, Y.; Li, H. Is Neuromorphic MNIST Neuromorphic? Analyzing the Discriminative Power of Neuromorphic Datasets in the Time Domain. *Front Neurosci* 2021, *15*, doi:10.3389/fnins.2021.608567.

139. Siddique, A.; Vai, M.I.; Pun, S.H. A Low Cost Neuromorphic Learning Engine Based on a High Performance Supervised SNN Learning Algorithm. *Sci Rep* 2023, *13*, 6280, doi:10.1038/s41598-023-32120-7.

140. Li, G.; Xie, D.; Zhong, H.; Zhang, Z.; Fu, X.; Zhou, Q.; Li, Q.; Ni, H.; Wang, J.; Guo, E.; et al. Photo-Induced Non-Volatile VO2 Phase Transition for Neuromorphic Ultraviolet Sensors. *Nat Commun* 2022, *13*, 1729, doi:10.1038/s41467-022-29456-5.

141. Bayat, F.M.; Prezioso, M.; Chakrabarti, B.; Nili, H.; Kataeva, I.; Strukov, D. Implementation of Multilayer Perceptron Network with Highly Uniform Passive Memristive Crossbar Circuits. *Nat Commun* 2018, *9*, 2331, doi:10.1038/s41467-018-04482-4.

142. Jiang, H. Artificial Eye Boosted by Hemispherical Retina. *Nature* 2020, *581*, 264–265, doi:10.1038/d41586-020-01420-7.

143. Merabet, L.B. Building the Bionic Eye: An Emerging Reality and Opportunity. In; 2011; pp. 3–15.

144. Berco, D.; Shenp Ang, D. Recent Progress in Synaptic Devices Paving the Way toward an Artificial Cogni-Retina for Bionic and Machine Vision. *Advanced Intelligent Systems* 2019, *1*, 1900012, doi:10.1002/aisy.201900012.

145. Seo, S.; Jo, S.; Kim, S.; Shim, J.; Oh, S.; Kim, J.; Heo, K.; Choi, J.-W.; Choi, C.; Oh, S.; et al. Artificial Optic-Neural Synapse for Colored and Color-Mixed Pattern Recognition. *Nat Commun* 2018, *9*, 5106, doi:10.1038/s41467-018-07572-5.

146. Seo, S.; Jo, S.; Kim, S.; Shim, J.; Oh, S.; Kim, J.; Heo, K.; Choi, J.-W.; Choi, C.; Oh, S.; et al. Artificial Optic-Neural Synapse for Colored and Color-Mixed Pattern Recognition. *Nat Commun* 2018, *9*, 5106, doi:10.1038/s41467-018-07572-5.

147. Lee, Y.; Rhee, H.; Kim, G.; Cheong, W.H.; Kim, D.H.; Song, H.; Kay, S.N.; Lee, J.; Kim, K.M. Flexible Self-Rectifying Synapse Array for Energy-Efficient Edge Multiplication in Electrocardiogram Diagnosis. *Nat Commun* 2025, *16*, 4312, doi:10.1038/s41467-025-59589-2.

148. Chen, S.; Zhang, T.; Tappertzhofen, S.; Yang, Y.; Valov, I. Electrochemical-Memristor-Based Artificial Neurons and Synapses—Fundamentals, Applications, and Challenges. *Advanced Materials* 2023, *35*, doi:10.1002/adma.202301924.

149. Lan, J.; Chen, Y.; Cao, Z.; Wang, K.; Lu, Q.; Ren, F.; Lv, Y.; Sun, B.; Wu, R. Memristor-Based Intelligent Systems for Sensing, Computing, and Therapeutic Integration Applications. *Mater Today Adv* 2025, *28*, 100628, doi:10.1016/j.mtadv.2025.100628.

150. Dias, C.; Castro, D.; Aroso, M.; Ventura, J.; Aguiar, P. Memristor-Based Neuromodulation Device for Real-Time Monitoring and Adaptive Control of Neuronal Populations. *ACS Appl Electron Mater* 2022, *4*, 2380–2387, doi:10.1021/acsaelm.2c00198.

151. Cao, Z.; Xiang, L.; Sun, B.; Gao, K.; Yu, J.; Zhou, G.; Duan, X.; Yan, W.; Lin, F.; Li, Z.; et al. A Reversible Implantable Memristor for Health Monitoring Applications. *Mater Today Bio* 2024, *26*, 101096, doi:10.1016/j.mtbio.2024.101096.

152. Mikhaylov, A.; Pimashkin, A.; Pigareva, Y.; Gerasimova, S.; Gryaznov, E.; Shchanikov, S.; Zuev, A.; Talanov, M.; Lavrov, I.; Demin, V.; et al. Neurohybrid Memristive CMOS-Integrated Systems for Biosensors and Neuroprosthetics. *Front Neurosci* 2020, *14*, doi:10.3389/fnins.2020.00358.

153. Lee, Y.; Rhee, H.; Kim, G.; Cheong, W.H.; Kim, D.H.; Song, H.; Kay, S.N.; Lee, J.; Kim, K.M. Flexible Self-Rectifying Synapse Array for Energy-Efficient Edge Multiplication in Electrocardiogram Diagnosis. *Nat Commun* 2025, *16*, 4312, doi:10.1038/s41467-025-59589-2.

154. Prieto-Avalos, G.; Cruz-Ramos, N.A.; Alor-Hernández, G.; Sánchez-Cervantes, J.L.; Rodríguez-Mazahua, L.; Guarneros-Nolasco, L.R. Wearable Devices for Physical Monitoring of Heart: A Review. *Biosensors (Basel)* 2022, *12*, 292, doi:10.3390/bios12050292.

155. Li, H.; Kumar, D.; El-Atab, N. A Memristor-Based Event-Driven Reservoir Computing System for Cardiac Arrhythmia Detection. *Advanced Intelligent Systems* 2025, doi:10.1002/aisy.202500350.

156. Wang, Z.; Yang, D.W.; Liu, Z.; Yan, E.; Sun, H.; Ge, N.; Hu, M.; Wu, W. Multi-Diseases Detection with Memristive System on Chip. *Advanced Intelligent Systems* 2025, *7*, doi:10.1002/aisy.202400736.

157. Ni, K.; Grisafe, B.; Chakraborty, W.; Saha, A.K.; Dutta, S.; Jerry, M.; Smith, J.A.; Gupta, S.; Datta, S. In-Memory Computing Primitive for Sensor Data Fusion in 28 Nm HKMG FeFET Technology. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM); IEEE, December 2018; Vol. 2018-Decem, pp. 16.1.1-16.1.4.