An Adaptive Dual-Mode HBC Transceiver for Medical and Entertainment Applications

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***Abstract*—Human body communication (HBC) is a low-power communication method using the human body as a medium for wearable and implantable devices. Existing systems support either Carrier-Based HBC (CB-HBC) with carrier modulation for noise immunity or Carrierless HBC (CL-HBC) with carrier-free signaling for simplicity and higher data rates, leading to separate transceiver (TRX) designs and limited flexibility. This work presents a unified TRX in TSMC 65nm silicon supporting both modes with real-time adaptability. Key features include: (1) a reconfigurable transmitter (TX) switching between CB-HBC across 4 carrier frequencies (up to 21 MHz) and CL-HBC, (2) an adaptive receiver (RX) with 4 digitally controlled bias levels for mode-specific gain-bandwidth tuning, and (3) programmable data rates up to 2 Mbps in CB-HBC, and 5.25 Mbps in CL-HBC. Measurement results show an energy efficiency of 25 pJ/bit (CB-HBC) and 8.4 pJ/bit (CL-HBC), power consumption of 50 μW and 44 μW respectively, bit error rate (BER) $< 10^{-4}$ at a carrier-to-data rate ratio < 14 for CB-HBC, and sensitivity of –91 dBm in a 0.12 mm^2 area.**

***Index Terms*—HBC, CB-HBC, CL-HBC, Reconfigurable Transmitter, Adaptive Receiver, OOK, Programmable Data Rate, Wearable Devices, BER**

I. Introduction

The rapid growth of wearable and implantable devices has created an urgent need for communication technologies that can efficiently connect these devices while addressing their unique constraints. Introduced by [1], HBC has emerged as a compelling solution that leverages the conductive properties of human tissues to establish low-power, secure communication channels. Compared to conventional wireless technologies such as Bluetooth or Wi-Fi, HBC offers fundamental advantages: substantially lower power consumption, enhanced security through signal confinement to the body, replacing antennas with capacitive coupling or galvanic coupling electrodes [2], and minimal electromagnetic radiation, making it particularly suitable for medical and entertainment applications in the vicinity of the human body.

Despite these advantages, HBC faces a critical technical challenge: the fundamental tradeoff between CB-HBC and CL-HBC transmission approaches. CB-HBC systems [3]–[7] employ carrier modulation (such as on-off keying (OOK)) at frequencies of 1–21 MHz to elevate signals above the low-frequency noise floor prevalent in HBC channels. This approach delivers superior bit error rates and resilience to channel variations, but traditionally limits data rates to preserve a certain carrier-to-data rate ratio—often as high as 50 [6], [7]—to maintain suitability for envelope detector-based systems. In scenarios where higher data rates are essential, low-power wake-up receiver architectures become necessary to enable fast and energy-efficient signal acquisition [8]. Conversely, CL-HBC systems [9]–[13] transmit digital signals without carrier modulation, enabling higher data rates up to the standard compliant of 5.25 Mbps, with simpler TX architectures and potentially lower energy-per-bit metrics. However, they exhibit significantly degraded performance in noisy environments, particularly affecting signal quality in noisy environments [14].

This architectural choice forces system designers to select between robust operation (CB-HBC) and simplified implementation (CL-HBC)—a compromise that limits the versatility of HBC technology. Current HBC TRXs address either CB-HBC or CL-HBC operation exclusively, with designs optimized for specific carrier frequencies and fixed data rates, preventing adaptation to varying application requirements. As illustrated in Table I, medical applications such as glucose monitoring and ECG typically demand ultra-low power consumption, high reliability, and strong privacy guarantees even at modest data rates (3-32 Kbps). In contrast, consumer applications such as audio streaming require substantially higher throughput (>2 Mbps) with different optimization priorities. Moreover, many emerging applications require both characteristics at different times: an endoscopic capsule might need robust, interference-resistant transmission when passing through human tissue in noisy environments but benefit from higher-rate direct transmission in favorable channel conditions.

Previous work [15] introduced digitally configurable modulation schemes for HBC, but relied on high-resolution, power-hungry ADC/DACs, resulting in 2317 μW TRX power and 231.7 pJ/bit energy efficiency, with fixed data rates across all modes. In contrast, our earlier system [13] achieved significantly lower energy consumption—349 pJ/bit (CB-HBC) and 16 pJ/bit (CL-HBC)—through autoencoder (AE)-based signal processing and CGAN-modeled channels. However, it was limited by fixed data rates (262.5 kbps for CB-HBC and 5.25 Mbps for CL-HBC), a single 21 MHz carrier, and significant overhead from the AE approach, as the data rate must be multiplied by a factor of 8 for proper AE operation, thereby constraining the maximum achievable rate.

To overcome previous limitations and advance HBC toward practical deployment, this work presents a fully integrated, silicon-proven TRX in TSMC 65 nm that supports dual-mode operation with adaptive data rates, selectable carrier frequen-

TABLE I: Key HBC Applications and Requirements

Application	Data Rate	Operational Mode
Medical		
Glucose Monitor	<10 Kbps	CB-HBC
Pacemaker	<50 Kbps	CB-HBC
ECG/SpO2	3-50 Kbps	CB-HBC
Endoscopic Imaging	>2 Mbps	CL-HBC
Consumer		
Audio Streaming	>2 Mbps	CL-HBC
Gaming Interface	>2 Mbps	CL-HBC
Authentication	<100 Kbps	CB-HBC
Adaptive		
Multi-sensor Array	0.1-1 Mbps	Both Modes
AR/VR Exchange	0.5-5 Mbps	Both Modes

cies, and digitally programmable analog front-ends. The TRX features digitally-controlled bias currents and programmable analog circuits that optimize performance for each operating mode. The unified architecture supports both CB-HBC and CL-HBC operation through precise digital control of critical circuit parameters, incorporating a programmable RX front-end with 4-level bias control and adaptive filtering that maintains robust performance across varying signal conditions. The flexible TX features programmable data rate control and selectable carrier frequency generation, supporting both OOK-modulated carriers across four selectable frequencies up to 21 MHz and direct CL-HBC transmission up to 5.25 Mbps through a single UART interface with digital mode selection.

The rest of the paper is organized as follows: Section II presents the system-level architecture. Section III details the circuit implementation. Section IV shows measurement results, and Section V concludes the paper.

II. System Overview

The proposed HBC TRX comprises a programmable TX and a dual-mode operating RX, as shown in Fig. 1. The TX subsystem incorporates a universal asynchronous receiver-transmitter (UART) and sensor interface that receives digital payload data, which is then buffered in a FIFO memory before being processed. Based on the Mode_Sel signal, this data is either directly transmitted as raw signals (CL-HBC mode) or modulated using OOK with selectable carrier frequencies (CB-HBC mode). A sophisticated configuration module allows for digital control of multiple transmission parameters via Baud_Sel, Rate_Sel, and Freq_Sel inputs, offering 8 distinct carrier frequencies up to 21 MHz and data rates up to 5 Mbps. The TX electrode couples the transmitted signal to the human body, which serves as the communication channel.

On the receiving end, the dual-mode RX features a signal processing chain optimized for both communication modes. The incoming signal from the RX electrode is first amplified by a frontend amplifier that provides a maximum gain of 20 dB, then processed through an envelope detector for carrier extraction (in CB-HBC mode) that is capable of detecting fronted amplified signal, followed by buffer and filtering stages to improve signal quality. Then, the analog multiplexer enables adaptive signal path reconfiguration to selects between CL-HBC and CB-HBC data based on the required mode of operation. The single-to-differential (S-to-D) buffer converts

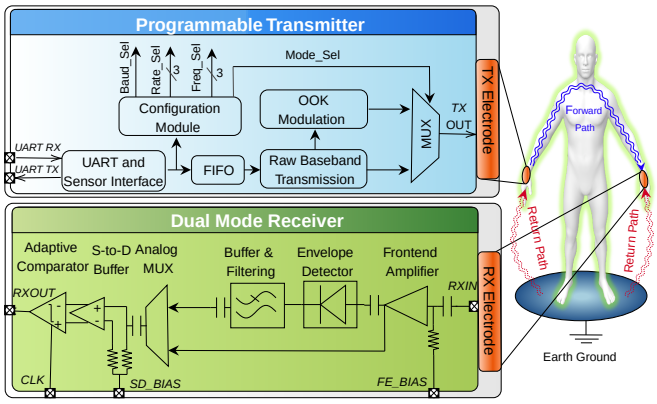


Fig. 1: System overview of the proposed dual-mode HBC TRX.

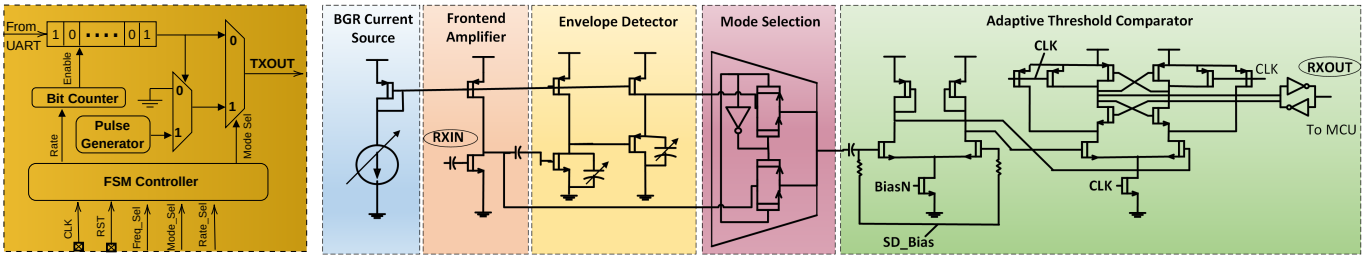
the signal to differential form to enhance noise immunity before the adaptive comparator generates the digital output. Notably, the system incorporates two critical bias control inputs (FE_BIAS and SD_BIAS) that enable programmable biasing of the frontend and signal detection stages, allowing dynamic optimization of circuit characteristics for different operating conditions and communication modes. The full RX is biased by a built in biasing circuit that provides trimming with two bit digital control signals to adapt for the required gain and bandwidth of each circuit. The entire architecture leverages the human body's conductive properties, with forward and return paths established between TX and RX electrodes, and earth ground serving as the external reference.

III. Circuit Implementation

Fig. 2 presents the circuit implementation of the proposed TRX showing a programmable TX using a bit counter, shift register, and pulse generator the signal transmission, while the dual-mode RX employs a frontend amplifier, envelope detector, and adaptive threshold comparator to process and output received signals. The circuit details of the transmitter and receiver are provided in the following subsections.

A. Transmitter Circuit Design

The TX architecture supports both CB-HBC and CL-HBC modes as presented in Fig.2a. Data received from the UART or sensor interface is first loaded into a shift register. This register is enabled by a control signal (`Enable`) generated by a bit counter, which is configured by the `Rate_Sel` signal from the FSM controller to set the desired data rate. The output of the shift register acts as the selector input to a multiplexer (MUX). When the selector is '0', the MUX outputs a logic low signal; when it is '1', it outputs a train of pulses generated by a pulse generator, where the frequency is set by the `Freq_Sel` control signal. This mechanism generates an OOK modulated signal for CB-HBC transmission. The CB-HBC OOK output and the CL-HBC signal (from the shift register) are then fed into a second MUX. The `Mode_Sel` signal determines the active transmission mode: '0' selects CL-HBC output, while '1' selects the CB-HBC output. The selected signal is finally transmitted via the `TXOUT` node.



(a) **(b)**

Fig. 2: Circuit level implementation of proposed TRX showing (a) programmable TX, and (b) dual-mode RX.

B. Receiver Circuit Design

1) Frontend Amplifier: The frontend amplifier employs a common-source topology with the main NMOS transistor biased in subthreshold region to achieve optimal g_m/I_D efficiency while minimizing power consumption. A carefully dimensioned current mirror serves as both the active load and bias generator, providing process-variation immunity and a high-impedance load path that contributes to the circuit's 20 dB voltage gain. This amplified signal then is fed into a buffer stage that performs dual functions critical to signal integrity: it prevents loading effects that would compromise the preamplifier's gain while simultaneously providing frequency-selective filtering to attenuate out-of-band interference inherent to human body channels. By suppressing interfering spectral components before the signal reaches the envelope detector, the buffer ensures cleaner demodulation in subsequent stages, thereby enhancing the overall resilience of the HBC RX in environments where signals are intrinsically weak and prone to interference.

2) Envelope Detector (ED): Following amplification, the signal is demodulated using a custom envelope detector (ED) featuring a complementary PMOS-NMOS topology with drain-terminal output. This design enhances output impedance and sensitivity while reducing capacitor size and area. The NMOS operates in subthreshold for improved nonlinearity, and a 2-bit trimming capacitor enables adaptive carrier rejection. The ED achieves 10 mVp sensitivity at 21 MHz. A subsequent adaptive low-pass filter—based on subthreshold transistors and a 2-bit variable capacitor—suppresses residual ripple and supports carrier-to-data rate ratios as low as 14:1 at BER of 10^{-4}. Together, the programmable ED and filter ensure robust, adaptable demodulation across varying HBC signal conditions.

3) Mode Selection Circuity : The mode selection circuit uses a four-transistor analog multiplexer (2 NMOS, 2 PMOS) implemented with high-threshold voltage (HVT) devices to minimize leakage and ensure high off-state impedance. Transistor sizing balances low on-resistance for minimal signal loss with controlled parasitics for bandwidth preservation. In CB-HBC mode, the demodulated output from the low-pass filter is selected; in CL-HBC mode, the signal bypasses the envelope detector, connecting directly from the preamplifier. This reconfigurable approach reduces area and power by eliminating redundant signal chains, while the transmission gate structure ensures low-distortion, high-integrity signal routing.

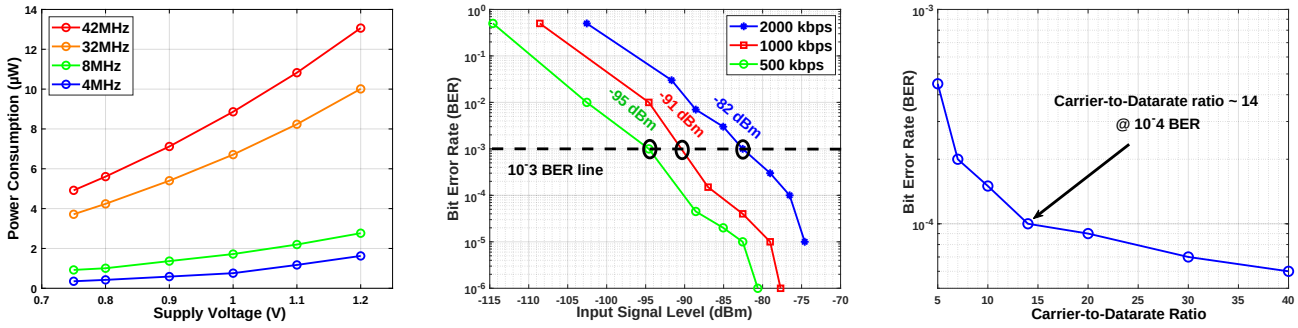
4) Adaptive Threshold Comparator: The final signal conditioning stage features a single-to-differential buffer followed by a dynamic comparator with a static latch. The buffer converts the single-ended multiplexer output into a balanced differential signal, $V_{diff}(t) = [0.5V_{MUX}(t), -0.5V_{MUX}(t)]$, using a diode-loaded PMOS differential pair biased by an NMOS tail current source. Matched transconductance ensures accurate phase inversion and amplitude halving, enhancing noise immunity and enabling adaptive thresholding. The dynamic comparator performs clocked polarity-based threshold detection, while the static latch holds the digital state between transitions, ensuring glitch-free data recovery. This architecture achieves high sensitivity with ultra-low power consumption, eliminating external references and supporting wide dynamic range signals typical in HBC environments.

IV. Measurement Results

The proposed adaptive HBC TRX is fabricated using the TSMC 65 nm low-power (LP) complementary metal-oxide-semiconductor (CMOS) technology. It supports both CB-HBC and CL-HBC communication modes and occupies an active area of only 0.12 mm^2. The total power consumption of the TX is measured across different supply voltages and supported clock frequencies. As shown in Fig. 3a, the measured power scales with supply voltage, demonstrating the TX's ability to operate across a range of clock frequencies and supply voltages achieving peak power of 9μA at 1V supply.

Bit error rate (BER) performance is evaluated using an ADALM-2000 (M2K) device, which captures the demodulated output at the RX. The captured data is post-processed in MATLAB. For each BER measurement point, 20 independent runs are performed with a data window size of 8 million samples to ensure statistical significance. Fig. 3b presents the BER performance at three data rates—500 kbps, 1 Mbps, and 2 Mbps—under varying input signal levels. At a BER threshold of 10^{-3}, the proposed TRX demonstrates a sensitivity of -95 dBm at 0.5 Mbps, -91 dBm at 1 Mbps and -82 dBm at 2 Mbps. To evaluate the effectiveness of the proposed envelope detector, additional BER measurements are conducted at different carrier-to-datarate ratios, keeping the data rate fixed at 1 Mbps. As shown in Fig. 3c, a minimum carrier-to-data rate ratio of 14 is sufficient to achieve a BER of 10^{-4}.

Table II presents a detailed comparison of the proposed TRX with state-of-the-art CB-HBC and CL-HBC HBC designs. The proposed design achieves dual-mode operation us-



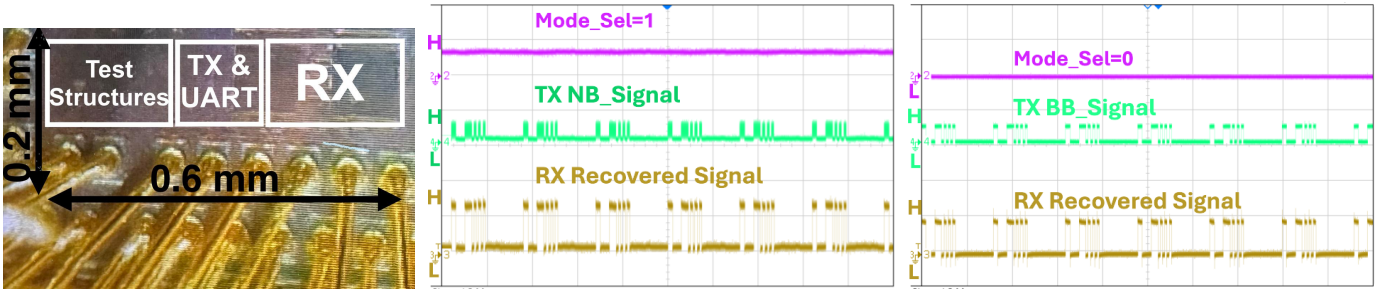
(a) (b) (c)

Fig. 3: Measurement results: a) the power consumption of the TX at different supply voltages and different data rates, b) BER at different input signal levels at the RX with different data rates, and 3) BER at different carrier-to-data rate ratios for CB-HBC mode.

TABLE II: Performance Comparison of HBC Transceivers

	[9]	[10]	[11]	[5]	[6]	[7]	[13]	[15]	**This Work**
Communication Mode	CL-HBC only			CB-HBC only			CB-HBC & CL-HBC		
Process (nm)	65	45	90	65	65	55	65	180	**65**
V_{DD} (V)	1.2	1.2	1.2	1.1	0.5	N/A	1.2	1.5	**1.0**
Clock (MHz)	42	42	42	120	1	2	42	40	**42**
Max Data Rate (Mbps)	5.25	5.25	1.31	2	0.001	0.5	0.26 (CB) / 5.25 (CL)	10	**2 (CB) / 5.25 (CL)**
Total Power (μW)	4140	1468	784	1970	0.415	710	91.8 (CB) / 85.3 (CL)	2317	**50 (CB) / 44 (CL)**
Energy (pJ/bit)	788	280	390	985	415	1420	349 (CB) / 16 (CL)	231.7	**25 (CB) / 8.4 (CL)**
RX Sensitivty (dBm)	-72 @ 5.25MHz	N/A	N/A	-83 @ 2MHz	-64 @ 1kHz	-104 @ 0.5MHz	N/A	N/A	**-91 @ 1MHz**
Area (mm^2)	0.672	N/A	N/A	0.54	0.17	0.123	0.27	0.216	**0.12**

* Measured based on 90 kΩ body channel model [7].



(a) (b) (c)

Fig. 4: a) Die micrograph, b) transient waveforms of CB-HBC mode c) transient waveforms of CL-HBC mode.

ing the same hardware, supporting data rates up to 5.25 Mbps (CL-HBC) and 2 Mbps (CB-HBC), with a maximum power consumption of 50 μW and 44 μW for CB-HBC and CL-HBC operation respectively. It demonstrates up to 14 $\times$ and 1.9 $\times$ improvement in energy efficiency compared to prior CB-HBC and CL-HBC architectures, respectively. Additionally, it achieves a sensitivity of -91 dBm at 1 MHz bandwidth occupying a compact 0.12 mm^2 active area. The fabricated die micrograph is shown in Fig. 4a, and measured transient waveforms for CB-HBC and CL-HBC modes are presented in Fig. 4b and Fig. 4c, respectively.

V. Conclusion

This work presents a fully integrated adaptive HBC TRX that bridges the trade-off between CB-HBC and CL-HBC communication through programmable analog and digital control in TSMC 65 nm silicon. The design supports adaptive data rates up to 2 Mbps (CB-HBC) and 5.25 Mbps (CL-HBC), four selectable carrier frequencies up to 21 MHz, and digitally controlled 2-bit biasing for dynamic tuning to varying channel conditions. A low-leakage analog multiplexer enables efficient signal path reconfiguration, minimizing area overhead. The envelope detector offers programmable carrier rejection, achieving a carrier-to-data-rate ratio of 14 for a BER below 10^{-4}. Unlike prior fixed-parameter prototypes, this implementation is validated through silicon measurements, demonstrating 50 μW and 44 μW power consumption for CB-HBC and CL-HBC modes, respectively. It achieves energy efficiencies of 25 pJ/bit (CB-HBC) and 8.4 pJ/bit (CL-HBC), occupies only 0.12 mm^2, complies with IEEE 802.15.6 standard rates and center frequencies, and supports both CB-HBC and CL-HBC signaling through a unified UART interface—enabling real-time adaptation across diverse application scenarios.

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