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Low-Temperature Al_2O_3/ZnO Thin-Film Transistors for 3D Heterogeneous Integration: Interface Engineering, Bias Stress Instability, and Reliability Mechanisms

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Abstract

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Back-end-of-line (BEOL) process scaling and the emergence of three-dimensional heterogeneous integration (3D-HI) demand thin-film transistors (TFTs) that can be integrated within a limited thermal budget while maintaining high electrical performance ($\mu_{\mathrm{FE}} > 10\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$), long-term reliability ($|\Delta V_{\mathrm{TH}}| < 0.5$ V after 1 h stress), and low manufacturing cost. Zinc oxide (ZnO) has attracted sustained interest as a channel material owing to its wide bandgap (∼3.3 eV), optical transparency, and compatibility with low-temperature processing. However, the stability of ZnO TFTs remains a major bottleneck, particularly in devices employing atomic-layer-deposited (ALD) aluminium oxide (Al_2O_3) gate dielectrics, where the dielectric/semiconductor interface critically governs bias-stress degradation.

This thesis systematically investigates the interdependence between Al_2O_3 deposition temperature (150–300 °C), interface-trap density (D_{it}), and bias-stress instability mechanisms in ZnO TFTs. A unified device platform was developed, incorporating both global p-Si bottom gates and patterned AZO bottom gates, enabling separation of intrinsic dielectric effects from gate-geometry-induced field crowding. Cross-sectional transmission electron microscopy (TEM), together with SILVACO/TCAD simulations, confirms the presence of localised electric-field enhancement at wet-etched sharp gate corners, which promotes percolation-type leakage paths and soft breakdown, particularly under high drain bias ($V_{\mathrm{D}} = 15$ V), where threshold-voltage shifts exceeding 1.2 V are observed.

A clear trade-off between mobility and reliability is identified as a function of Al_2O_3 deposition temperature. Devices fabricated with Al_2O_3 deposited at 150 °C exhibit lower field-effect mobility ($\mu_{\mathrm{FE}} \approx 4.8\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$) yet the most stable behaviour, with small hysteresis (< 0.2 V) and reduced trap density ($N_{\mathrm{trap}} \sim 3 \times 10^{12}\ \mathrm{cm^{-2}}$), consistent with hydrogen-assisted defect passivation. By contrast, films deposited at 300 °C are denser and yield higher mobility ($\mu_{\mathrm{FE}} \approx 8.7\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$), but suffer from substantially increased hysteresis (> 1.0 V) and higher trap density ($N_{\mathrm{trap}} > 1 \times 10^{13}\ \mathrm{cm^{-2}}$). Capacitance–voltage (C–V) analysis shows a dielectric constant of $k \approx 8.2$ and a stable oxide capacitance ($C_{\mathrm{ox}} \approx 7.5 \times 10^{-7}\ \mathrm{F\,cm^{-2}}$). Under positive bias stress (PBS, +10 V) in the dark, significant charge trapping is observed with ΔV_{TH} up to +2.3 V, whereas negative bias stress (NBS) in the dark is comparatively weak ($\Delta V_{\mathrm{TH}} > -0.2$ V), consistent with limited de-trapping dynamics in p-Si gated structures.

Optical excitation at 365 nm (photon energy ∼3.4 eV) profoundly alters the stress response through photo-generated carriers. Under illumination, PBS exhibits an initial rapid ΔV_{TH} shift (e.g., $\sim +0.8$ V within 60 s), followed by partial saturation consistent with enhanced de-trapping. Conversely, NBS becomes strongly destabilising, producing large negative shifts (e.g., -1.5 V after 1 h) accompanied by marked subthreshold-slope degradation. These results demonstrate that illumination accelerates both trapping and de-trapping processes and highlights the dynamic charge balance at the Al_2O_3/ZnO interface.

By synthesising structural, chemical, and electrical analyses, this thesis establishes a comprehensive reliability map for Al_2O_3/ZnO TFTs under BEOL-compatible conditions. Three practical design strategies are proposed: (i) gate-geometry engineering to mitigate field crowding and suppress edge-initiated percolation leakage, (ii) interface/dielectric optimisation using lower deposition temperatures (typically $\lesssim 200\,^{\circ}\mathrm{C}$) to leverage hydrogen-assisted passivation, and (iii) control of plasma chemistry during PEALD to reduce sub-oxide defects. Collectively, these principles provide a pathway to stabilise oxide TFTs for 3D-HI platforms, flexible electronics, and low-power integrated systems.

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List of Parameters

Electrical Parameters

$V_{\mathrm{TH}}(V_{\mathrm{th}})$	Threshold voltage (V).
μ_{FE}	Field-effect mobility ($\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$).
μ_{eff}	Effective mobility ($\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$).
$\mathrm{I_{DS}}$	Drain-Source current (A).
$\mathrm{I_G}$	Gate leakage current (A).
$\mathrm{g_m}$	Transconductance (A/V).
$\Delta\mathrm{V_{th}}$ $(\Delta\mathrm{V_{TH}})$	Threshold voltage shift between two measurements (V).
ΔSS	Change in subthreshold slope (mV/dec)
SS	Subthreshold slope (mV/dec).
$\mathrm{g_d}$	Channel Conductance (S).
$\mathrm{D_{it}}$	Interface trap states density ($\mathrm{cm}^2\mathrm{eV}^{-1}$).
C/A	Capacitance per unit area ($\mathrm{F/cm}^2$).
$\mathrm{V_G}(\mathrm{V_{GS}})$	Gate voltage (V).
$\mathrm{V_D}(\mathrm{V_{DS}})$	Drain voltage (V).

Device Geometry

W	Channel width (μm).
L	Channel length (μm).

C_{ox}	Gate-oxide capacitance per area (F/cm^2).
t_{ox}	Oxide thickness (nm).
GPC	Growth per cycle in ALD (nm/cycle).

Stress Measurement

PBS	Positive Bias Stress.
NBS	Negative Bias Stress.
t_{stress}	Stress time (s).
ΔV	Hysteresis window (V).

Material & Surface Analysis

V_O	Oxygen vacancy.
V_{Zn}	Zinc vacancy.
O_i	Oxygen interstitial.
Zn_i	Zinc interstitial.
Zn_O	Anti-site defect, Zn atom at O site.
O_{Zn}	Anti-site defect, O atom at Zn site.
V_{Al}	Aluminium vacancy.
Al_i	Aluminium interstitial.
$^{\smile}OH$	Hydroxyl group.
Q_{ot}	Oxide trap charge.
$Q_{ZnO,t}$	ZnO-related interface trap charge.

Declaration of Authorship

I declare that this thesis and the work presented in it is my own and has been generated by me as the result of my own original research.

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;
2. Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
3. Where I have consulted the published work of others, this is always clearly attributed;
4. Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
5. I have acknowledged all main sources of help;
6. Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
7. None of this work has been published before submission

Signed:..... Date:March 2026

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List of Publications

Journal Paper Publications:

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[2] B. D. Rowlinson, J. Zeng, C. Patzig, M. Ebert, and H. M. H. Chong, "Impact of Bias Stress and Endurance Switching on Electrical Characteristics of Polycrystalline ZnO-TFTs with Al_2O_3 Gate Dielectric," *Journal of Physics D: Applied Physics*, vol. 58, no. 2, p. 025308, Oct. 2024, doi: 10.1088/1361-6463/ad8663.

Conference Publications:

[1] J. Zeng, B. D. Rowlinson, O. Kapur and H. M. H. Chong, "Impact of PEALD Temperature on Al_2O_3 Gate Dielectric of ZnO-TFTs," *MNE 2025*, Southampton, United Kingdom, 15–18 Sep. 2025.

[2] J. Zeng, B. D. Rowlinson, M. Ebert, K. Kalna, C. Patzig, L. Berthold and H. M. H. Chong, "Investigation of Sharp Corners Effect of Al-doped ZnO Gate and Al_2O_3 Insulator in ZnO Thin Film Transistors," *MNE 2023*, Berlin, Germany, 25–28 Sep. 2023.

[3] B. D. Rowlinson, J. Zeng, A. C. Mallari, J. D. Akrofi, M. Ebert, L. A. Boodhoo, and H. M. H. Chong, "Contiguous Plasma-Enhanced ALD for High-Performance Zinc Oxide TFTs," *SSDM 2022*, Chiba, Japan, 26–29 Sep. 2022.

[4] B. D. Rowlinson, J. Zeng, V. Mourgelas, C. Patzig, L. Berthold, J. D. Akrofi, M. Ebert, and H. M. H. Chong, "Integrated Zinc Oxide Inverters with Optimised

Al-doped Zinc Oxide Contacts," *MNE 2022*, Leuven, Belgium, 17–23 Sep. 2022.

Chapter 1

Introduction

As three-dimensional heterogeneous integration (3D-HI) and back-end-of-line (BEOL) processing rapidly advance, transistor technologies are required to fulfill demanding thermal budgets (typically $< 400\ ^{\circ}C$), large-area deposition, and low-power, high-reliability switching Wang et al. (2023); Kim et al. (2024c); Niu et al. (2024). Within metal-oxide thin-film transistors (TFTs), zinc oxide (ZnO) is unique in that it can be deposited at room-to-low temperatures (typically $< 300\ ^{\circ}C$) Wang et al. (2007); Rowlinson et al. (2024b), can be stacked in monoliths without damaging underlying interconnects and polymers Li et al. (2023); Wu et al. (2020). This low-temperature process window is critical to 3D-HI/BEOL logic, sensing and memory periphery Kim et al. (2024b); Mao et al. (2022). Meanwhile, the gate-dielectric/channel interface controls device performance and long-term stability: interface and dielectric traps lead to threshold-voltage drift, sub-threshold slope (SS) broadening, hysteresis, and light-assisted bias-stress instabilities (PBS/NBS) Jin et al. (2022); Lee et al. (2020a). Such reliability bottlenecks are the major obstacles in transferring ZnO TFTs out of the laboratory demonstrations to engineered systems.

1.1 Significant Results and Contributions

The thesis sets up a quantitative correlation between bottom-gate sharp corners and electrical failure. Devices under high drain bias experience progressive loss of gate control with a steep increase of gate leakage. TEM cross-sections and

SILVACO/TCAD field simulations indicate that field crowding occurs strongly at sharp corners that seed percolation paths across Al_2O_3. The percolation path is a direct cause of ΔV_{TH} drift and soft breakdown. A critical work plan is suggested: dielectric quality uplift.

Between 150-300 $^{\circ}C$ deposition of Al_2O_3, 250 $^{\circ}C$ is superior in drive/mobility, but worsens in stress stability, 300 $^{\circ}C$ is worse, 150 $^{\circ}C$ provides the most predictable baseline: lowest hysteresis, controlled gate leakage. Metal insulator semiconductor (MIS) C-V on p-Si is applied to isolate D_{it} and hysteresis, distinguishing between interface and bulk-dielectric effects and supporting the effect of temperature on the evolution of trap populations.

The severity of stress is monotonically proportional to photon energy under 340/365/405/490 nm light. Short wavelengths of 365 nm (nearer to ZnO 3.3 eV band edge) produce more e-h pairs, fill traps more efficiently at the interface/dielectric, and augment ΔV_{TH} and SS broadening. Wavelength-dependent instability spectra are measured with a single drive current. Devices containing 150 $^{\circ}C$ Al_2O_3 exhibit the least baseline instability that shows lowest effect of light-induced effects.

1.2 Thesis Structure

Chapter 2: Background and Motivation: Summarise ZnO TFT development, interface physics, hysteresis/bias instability mechanisms and the advantages/disadvantages of Al_2O_3 dielectrics under BEOL constraints. It develops three research gaps and gives an overview of the experimental/theoretical plan.

Chapter 3: Methods and Metrics. Specifies the electrical and physical measurements employed in the analysis: V_{TH}, SS, mobility, hysteresis, D_{it}, peak g_m, and gate-leakage indices. Defines the analysis tools of I-V and C-V (with Terman-style D_{it}) and sets the common stress/measurement protocols.

Chapter 4: Fabrication and Measurement Platforms. Specifications stack and process (low-temperature ALD/PE-ALD Al_2O_3 and ZnO, global p-Si-gate and patterned AZO bottom-gate). Details I-V/C-V benches, optical PBS/NBS with unified stress conditions, including the wavelength control.

Chapter 5: Gate Geometry, Field Crowding, and Failure. Reports the experimental-simulation study of sharp-corner effects: electrical (gate-control loss,

leakage increase), TEM, and TCAD simulated electric-field maps. Suggests a dielectric material quality optimization.

Chapter 6: Dielectric/Interface Engineering vs. Temperature. Comparative studies the Al_2O_3 deposition at 150/ 200/ 250/ 300 $°C$ and relate the structural/chemical indicators to the device characteristics (hysteresis, ΔV_{TH} under PBS/NBS). Presents the performance-stability trade-off and suggests 150 $°C$ as the preferred stability deposition temperature window for Al_2O_3 gate oxide in low-temperature oxide electronics.

Chapter 7: Optical PBS/NBS Spectroscopy. Implements the multi-wavelength stress protocol (340-490 nm) and measures wavelength-dependent ΔV_{TH} and SS and correlates photon energy dependence to interface/dielectric defect involvement. Elaborates on dark and illuminated processes and the mechanism of photo-assisted trapping/detrapping.

Chapter 8: Conclusions and Prospects. Surveys contributions in gate geometry, dielectric/interface engineering, and light-assisted stress. Suggests three BEOL-based paths, including gate-shape engineering, low-temperature dielectric/interface recipes, and ZnO plasma-chemistry control, to stabilize ZnO-based circuits in 3D-HI, flexible substrates and oxide logic.

Succinctly, this thesis combines gate geometry structure analysis, gate oxide process/defect engineering, and Oxide/ZnO interface spectroscopic stress probing to create a unified failure/stability map to Al_2O_3/ZnO TFTs in BEOL-compatible conditions. The resulting design-to-measurement architecture offers realistic suggestions and recipes to implement the high-stability oxide electronics for low temperature applications such as 3D heterogeneous integration.

Chapter 2

Literature Review

2.1 Introduction

With the rapid development of large-area displays, flexible electronics, and low-temperature processing technologies, oxide semiconductors are gaining significant attention due to their excellent physical properties. They are becoming key candidate materials for the active layer in thin-film transistors (TFTs). Among this family of materials, n-type oxide semiconductors represented by zinc oxide (ZnO) and its related complexes (for example, indium gallium zinc oxide (IGZO) and zinc tin oxide (ZTO)) demonstrate a wide range of applications due to their wide band gap (3.3 eV), high carrier mobility in polycrystalline and amorphous states, and good transparency to visible light Hosono (2010); Nomura et al. (2004). These advantages make ZnO-based TFTs ideal for emerging areas such as transparent display backplanes, wearable electronics, and low-power sensing systems.

The motivation for research on ZnO TFTs can be traced back to the performance limitations of traditional amorphous silicon (a-Si:H) and organic semiconductors. Although the fabrication process of a-Si:H is well established, the application of high resolution and high refresh-rate displays is limited due to its low mobility ($\backsim$0.5 $cm^2/(Vs)$). Organic semiconductors face poor working stability and a low current on/off ratio Sze and Ng (2006). Based on these specific requirements, under an optimized fabrication process, ZnO TFTs not only achieve high field effect mobility ($>$ 10 $cm^2/(Vs)$) but also demonstrate excellent thermal stability and chemical stability,

and are compatible with a wide range of substrates, including flexible plastics Kim et al. (2011); Kamiya et al. (2009).

Moreover, ZnO and its related complexes can be deposited through a variety of thermal processes, for example, atomic layer deposition (ALD), plasma enhanced atomic layer deposition (PEALD), pulsed laser deposition (PLD), and RF magnetron sputtering. Due to high deposition technology compatibility, ZnO can be integrated into various applications, such as heterogeneous integration (shown in fig. 2.1 Kim et al. (2024a); Wang et al. (2023)), display backplane, flexible electronic systems based on polymers Banger et al. (2010). However, the intrinsic n-type conductivity of ZnO is widely linked to oxygen vacancies, which function as carrier donors or compensating defects. Although these vacancies enable efficient electron transport, they simultaneously undermine device stability under bias stress, manifesting as threshold voltage instability and performance degradation. Therefore, to improve device stability and reliability, the in-depth study of interface state regulation, dielectric optimization, and trap state modeling receives attention Kim et al. (2021); Rowlinson et al. (2024a,b).

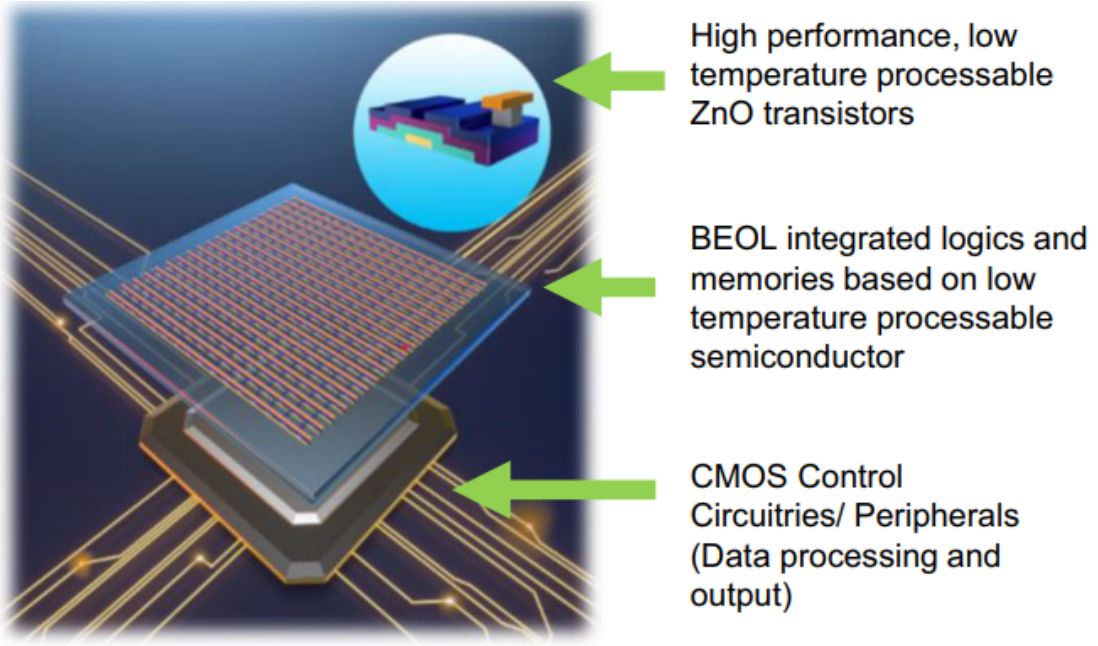

Figure 2.1: Schematic of ZnO based 3D heterogeneous integration, adapted from Wenhui Wang et al. (2023).

In summary, ZnO-based TFTs have become a research hotspot in the fields of display technology, semiconductor physics, and materials science due to their material advantages and process compatibility. This chapter provides a review of the historical development of ZnO TFTs, including the fabrication process, electrical properties, and

their characterization results under various measurement methods, for example, current-voltage (I-V), capacitance-voltage (C-V), positive bias stress (PBS) and negative bias stress (NBS), analyzing key issues in current research and suggesting future directions.

2.2 Historical Development of ZnO-Based TFTs

The exploration of ZnO as a semiconductor material initially began in the mid to late 20th centuryBoesen and Jacob (1968). However, research on its practical application as a thin-film transistor (TFT) started gradually in the 1990s. At that time, vacuum deposition or magnetron-sputtering techniques were mainly used by researchers to prepare thin polycrystalline ZnO films, which initially demonstrated good semiconductor properties Hoffman et al. (2003). In 2004, the research group led by Prof. Hosono of the Tokyo Institute of Technology first reported work on the deposition of amorphous indium-gallium-zinc oxide (a-IGZO) thin films at room temperature and successfully fabricated transparent and flexible thin film transistors (TFT) with excellent performance (Hall effect mobility of 10 $cm^2/(Vs)$) Nomura et al. (2004). This work laid the foundation for ZnO-based thin-film transistors (TFTs) in the field of transparent electronics and displays.

ZnO thin films present a higher mobility potential compared to a-Si:H. However, the difficult control of grain boundaries, defect state density, and carrier concentration limits its application. Therefore, to improve stability and mobility, researchers are moving towards multicomponent oxide semiconductors. IGZO is becoming the industry standard due to its high electron mobility, even in the amorphous state, and good device stability Fortunato et al. (2012). In recent years, some new materials, such as zinc tin oxide (ZTO) Singh et al. (2019), indium zinc oxide (IZO)Stojanoska et al. (2023), and other binary, ternary, or quaternary oxide materials, have further expanded the material platform of ZnO-based TFTs, gradually improving and balancing the overall performance between mobility, stability, and transparency Zhang et al. (2019b). Similar interface and reliability challenges have been reported in advanced high-mobility semiconductor systems, such as $In_{0.53}Ga_{0.47}As$ MOSFETs with ALD A_2O_3 gate dielectrics, where a high density of border traps causes hysteresis and bias-stress instability Ji et al. (2015).

ZnO still receives a lot of research interest although multicomponent oxides like IGZO and ZTO have shown superior stability and are currently finding extensive application in industry. The reasons are threefold. First, ZnO is inexpensive and simple in terms of chemical properties as compared to compounds including indium, thus it can be scaled to large area electronics with low cost. Second, ZnO has inherent properties of large bandgap, high optical transparency, and good compatibility with a variety of deposition technologies, including ALD, sputtering and solution processing, and enables integration with numerous different platforms. Third, ZnO offers a model system to study the basic physics of defects, interface engineering and mechanisms of reliability. The knowledge acquired in ZnO can be used as the basis of knowledge about more complicated multicomponent systems and be optimized. Thus, even though IGZO and related alloys have conquered the industrial market, ZnO-based TFTs are still a good topic to be studied and a potential candidate to be used in situations where cost, ease of process, or a particular set of physical characteristics will be the determining factors. Versus CMOS processes, low-temperature deposition is one of the main advantages of ZnO TFT compared to traditional silicon-based materials.

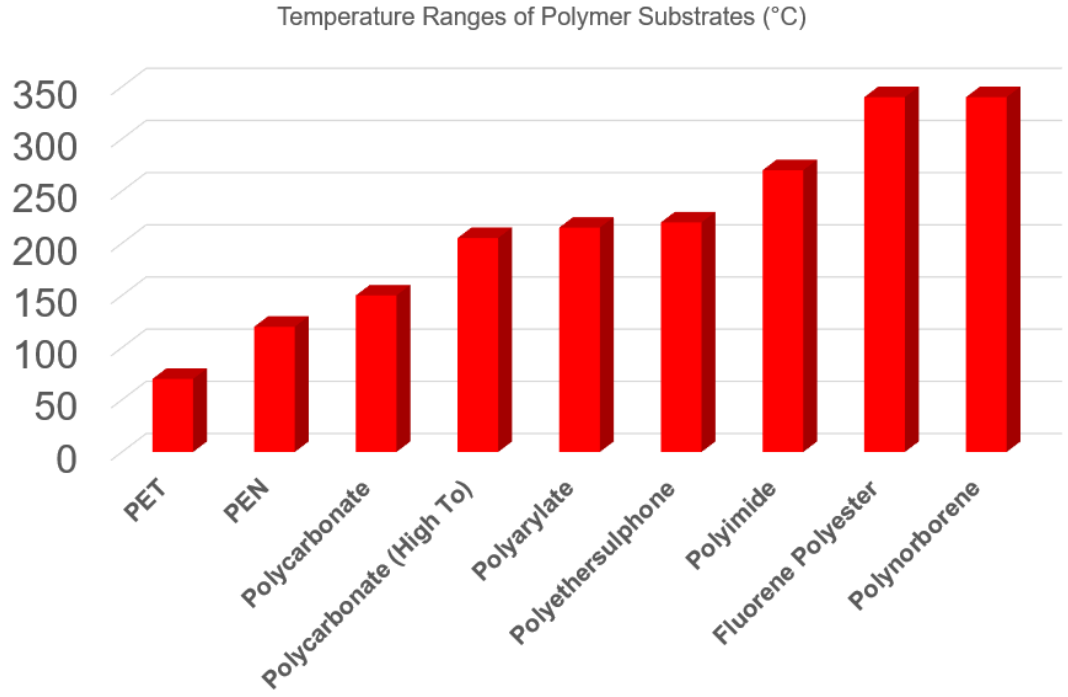

FIGURE 2.2: Glass transition temperatures of commonly used plastic substrates in printed sensors and electronics, adapted from Saleem Khan et al. (2015).

2.3 Interface Properties in ZnO TFTs

The electrical performance of general metal oxide TFTs is highly dependent on the quality of the interface between the channel layer and the dielectric layer. Ideally, a lower interface state density (D_{it}) is expected to provide better transfer characteristics, such as high field effect mobility, a steep subthreshold slope, and a stable threshold voltage with small hysteresis, especially regarding reliability and stability under long-term bias Nomura et al. (2004); Kamiya and Hosono (2010).
The influence of interface state density on the overall interface quality is most evident in the defect states that emerge at the boundary between the ZnO channel and the dielectric layer Oktasendra and Utama (2020). Those defect states can trap the free carriers and significantly reduce the effective mobility of the TFT. Fast charge trapping and detrapping processes similar to those observed in high-k Flash memory stacks can occur at the ZnO/Al_2O_3 interface, leading to dynamic instabilities and time-dependent hysteresis Robinson et al. (2014). First, the D_{it} is one of the most important parameters for demonstrating the quality of the material. Moreover, a high interface state density can induce a threshold voltage shift, resulting in the characteristic uncertainty of the devices under prolonged working conditions. The high D_{it} plays a role in high-frequency charge and discharge during the device switching process, causing hysteresis and a high subthreshold slope. To quantify such trapping dynamics, discharge-based pulse techniques have been developed to map the energy distribution of positive charges in gate dielectrics, revealing multiple defect origins across and beyond the silicon bandgap Gao et al. (2015); Hatta et al. (2013).
Numerous studies have shown that the density of the interface state can be reduced using interface optimization methods, such as post-annealing Wang et al. (2016); Jang et al. (2010); Zhou et al. (2020). Carrier scattering at the interface is a physical transport mechanism induced by interface roughness and charged defect states, which degrades device performance, long-term degradation can also involve defect loss and slowdown phenomena, where thermally activated recombination or hardening of precursors alters the recharge kinetics and effectively extends device lifetime Duan et al. (2012). The carrier scattering occurs as a result of a rough or non-uniform interface. This phenomenon will directly reduce field mobility and increase the subthreshold sweep (SS)Wang and Dodabalapur (2021). By adjusting the conditions of

the deposition process, the roughness and uniformity of the interface can be optimized Alshammari et al. (2016); Song et al. (2021); Huang et al. (2021).

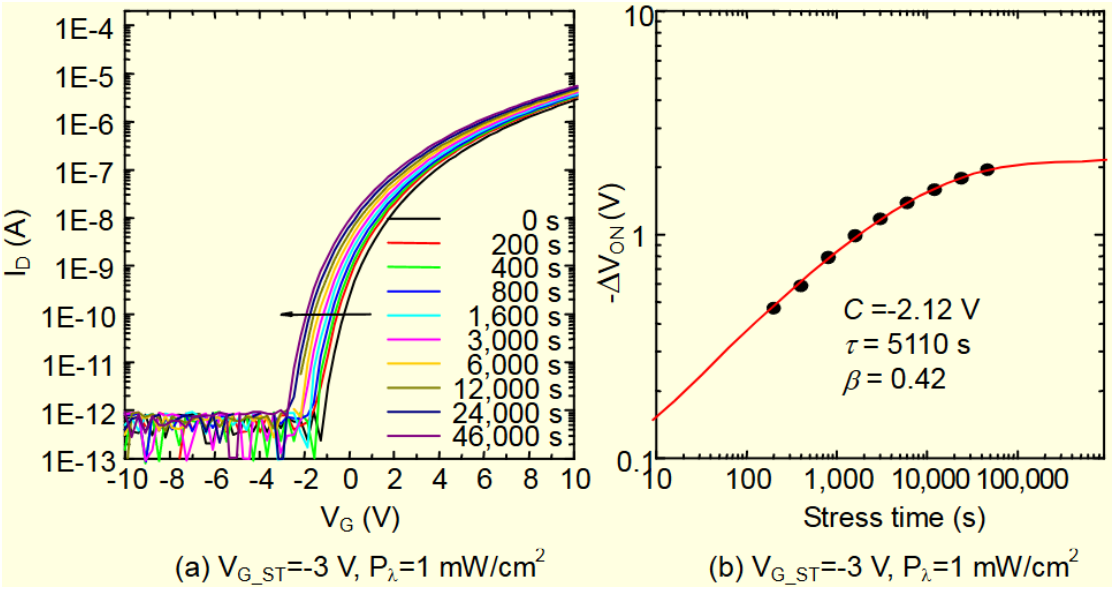

FIGURE 2.3: (a) Changes in the $I_D - V_G$ characteristics of ZnO TFTs(W/L = 40 µm/20 µm) under ˇ3 V gate bias stress with light intensity of 1 mW/cm^2 and (b) ΔV on vs. stress time in log scale (circles: experiments, line: theoretical calculation, adapted from Jae-Heon Chowdhury et al. (2015).

The working environment, such as humidity, light, and temperature, could also affect the performance of ZnO thin-film transistors by changing the interface properties.

- Humidity effect: Water molecules are easily absorbed on the surface, forming additional trap charges, leading to mobility degradation, V_{th} drift, and a high SS. Therefore, the conductivity of the ZnO channel will change significantly as a result of the absorption of water molecules. Surface passivation can be used to improve stability Li et al. (2005); Lim et al. (2017); Lee and Jeong (2018).

- Light effect: Photons can excite defect states within the ZnO channel or at the interface, generating excess charge carriers. These carriers are redistributed and partially trapped at defect sites, thereby enhancing charge imbalance and accelerating the V_{th} shift. This phenomenon could be observed by conducting an optical bias stress measurement Chowdhury et al. (2015); Chen et al. (2017); Kim et al. (2016); Shin et al. (2009). Shown in figure 2.3, Long-term light stress can significantly cause a negative shift in the threshold voltage.

- Temperature effect: High temperatures accelerate the charge and discharge of trap states, as well as electronically excite oxygen-related defect states at the Al_2O_3/ZnO interface. Inducing mobility degradation and faster V_{th} drift. Annealing is a method to overcome this problem Chen et al. (2017); Kim et al. (2023).

Therefore, based on the above considerations, interface engineering of ZnO TFTs is essential for achieving stable and reliable operation. Gaining deeper insight into the role of interface states and carrier scattering, together with advancing fabrication strategies to achieve higher process control, remains a central research challenge for ZnO TFTs. Advanced characterization methods such as the discharge-based and pulse I-V techniques have proven effective for probing trap energy distributions with sub-microsecond resolution, enabling accurate extraction of border-trap and interface-trap densities Gao et al. (2015); Hatta et al. (2013); Ji et al. (2015). It is important to note that densities and dynamics of interface states are the determinants of the basic properties of charge transport in the device not only when it is run on the long term electrical operation, but also when determining the response of the device. In fact, these (interfacial) traps react to mobile ionic species within the dielectric leading to hysteresis effects and bias stress instability (BSI). The following section (2.4) will address the causes of the methods with regard to the effects of the macroscopic manifestations, i.e. the shift of the threshold voltage and the hysteretic behaviour when the voltage was applied to the gate with the positive polarity or negative polarity. Analogous mechanisms have been extensively studied in CMOS technologies, where positive-bias temperature instability (PBTI) and negative-bias temperature instability (NBTI) originate from different trap types and charging kinetics. The as-grown-generation model separates pre-existing and generated traps for accurate lifetime prediction under both DC and AC stress Gao et al. (2018). Furthermore, investigations of electron traps under PBTI and hot-carrier aging confirm two distinct trap families—cyclic and antineutralization traps—governing short-term and permanent degradation, respectively Duan et al. (2016). In Ge-based pMOSFETs, NBTI is dominated by positive-charge formation in the GeO_2/Al_2O_3 stack rather than interface-state generation, offering insight into the asymmetry between positive and negative bias stress responses Ma et al. (2014). This transformation shows the basic

linkage that is present between the interfacial defect chemistry and the operational stability of ZnO TFTs.

2.4 Hysteresis Mechanisms and Bias Stress Instability in Al_2O_3/ZnO TFTs

In the ZnO-based n-type thin film transistors (TFTs), bias stress instability (BSI) and hysteresis phenomena are mainly dominated by the capture and release processes of interface trap charges, as well as the migration of mobile ionic charges in the gate dielectric layer Daus et al. (2025); Balakrishna Pillai and De Souza (2017); Daus et al. (2016).

- Positive bias stress: When a positive voltage is applied to the gate, channel electrons can inject into defect states in the Al_2O_3 dielectric layer or the Al_2O_3/ZnO interface. The injected carriers could lead to a positive threshold voltage (V_{th}) shift (in the clockwise direction), which means that a higher voltage is needed to turn on the device. Moreover, the asymmetry in charge capture and release during the forward sweep and reverse sweep results in the unmatched I-V characteristic curve Daus et al. (2016).
- Counter-clockwise hysteresis phenomenon: In some cases, a negative threshold voltage shift or counter-clockwise hysteresis may occur. This could be explained in two ways: (1) Electrons are injected into the dielectric from the gate rather than from the channel. (2) There are movable ions (such as hydrogen ions, hydroxyl ions, or metal ions) that exist in the dielectric layer, and these ions move under bias stress, resulting in an inverted hysteresis direction by changing the distribution of the interface electric fieldDaus et al. (2025); Balakrishna Pillai and De Souza (2017).

Figure 2.4 (a) presents the typical threshold voltage shift and hysteresis phenomenon under positive bias stress in ZnO TFT Balakrishna Pillai and De Souza (2017). When a positive voltage is applied to the gate, the device may experience a positive threshold voltage shift and clockwise hysteresis.

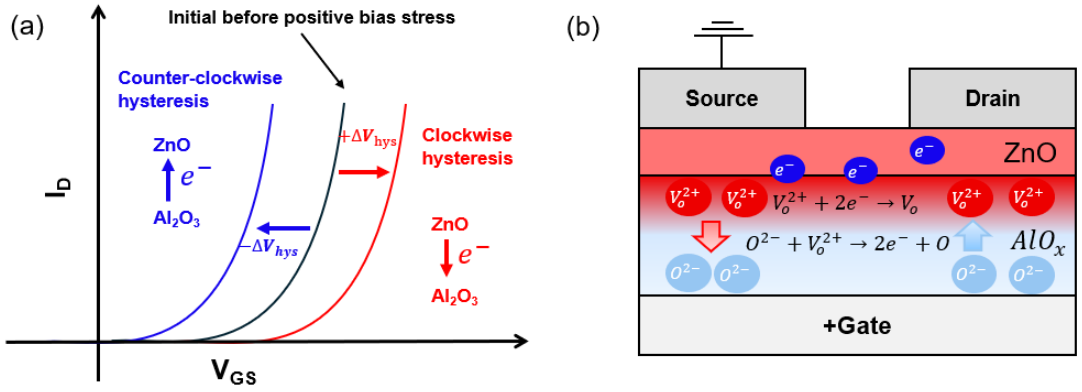

FIGURE 2.4: (a) Schematic of transfer characteristic of ZnO TFTs under positive bias stress (PBS): Clockwise hysteresis (red, $+\Delta V_{hys}$); it occurs due to electrons being trapped in the Al_2O_3/ZnO interface or dielectric traps; Counter-clockwise hysteresis (blue,$-\Delta V_{hys}$), usually due to the movement of the movable ions in the dielectric layer. (b) Schematic of the defect mechanism in Al_2O_3/ZnO interface under positive bias stress (PBS), including electrons injected from the channel into the oxygen vacancy and the movable ionized oxygen moving in the Al_2O_3. Those two defects lead to the threshold voltage shift and degradation of device instability.

The mechanism behind this phenomenon could be that channel electrons are injected into the Al_2O_3/ZnO interface and trapped by the defect state ($V_o{}^{2+}$), thereby causing the device to require a greater gate voltage to turn on, resulting in a positive threshold voltage shift ($+\Delta V_T$). On the other hand, if movable ions exist in the the Al_2O_3 dielectric layer (o^{2-}), a counter-clockwise hysteresis could occur, accompanied by a negative threshold voltage shift ($-\Delta V_T$). Figure 2.4 (b) presents the schematic of Al_2O_3/ZnO interface under positive bias stress (PBS), which illustrates the defect mechanism. While a positive voltage is applied to the gate, the ZnO channel electrons are injected into the oxygen vacancy defect state. At the same time, inside Al_2O_3, the oxygen ions (o^{2-}) could react with vacancies, and further adjustments to the interface electric field exacerbate the instability of the threshold voltage Balakrishna Pillai and De Souza (2017).

Therefore, the direction of hysteresis and PBS instability depends on interface trap density (D_{it}), dielectric defect states, and the presence of mobile ions. By adapting high-quality dielectrics, the device reliability could be improved by reducing interface traps and mobile ions.

2.5 The Advantages of Al_2O_3 Dielectric Layer

In ZnO thin film transistors (TFTs), the dielectric layer plays a decisive role in determining the threshold voltage (V_{th}), field effect mobility (μ_{FE}), subthreshold slope (SS), and stability under positive and negative bias stress (PBS/NBS). Among dielectric materials, Al_2O_3 possesses a significantly higher dielectric constant than conventional SiO_2 and has been widely used in ZnO-based thin-film transistors due to its superior dielectric performance Nomura et al. (2004); Fortunato et al. (2012). The intrinsic advantage of a high-k dielectric is its ability to provide a higher gate capacitance per unit area (C_{ox}) at the same physical thickness. An increased gate capacitance enables more efficient electrostatic control of the channel, which, in turn, lowers the threshold voltage, while enhanced gate control also contributes to the suppression of leakage currents.

From a fabrication perspective, atomic layer deposition (ALD) offers a reliable and scalable method for the growth of Al_2O_3 thin films, providing atomic-level thickness control and excellent surface uniformity. For Al_2O_3/ZnO based thin-film transistors, ALD technology enables the sequential growth of both layers in a single process without breaking vacuum, thereby minimizing interfacial contamination and ensuring a cleaner surface. In particular, plasma-enhanced ALD (PEALD) provides improved film quality, since O_2 plasma effectively removes residual surface groups $-CH_3$ and other organic contaminants during deposition Rowlinson et al. (2024a,b). Defects within the dielectric can be further minimized by high-temperature post-annealing. For applications requiring low-temperature processes, the optimization of the ALD conditions allows for the deposition of dense and smooth films, thus improving both the chemical stability and the interfacial morphology of the Al_2O_3/ZnO interface system Zhou et al. (2020); Wang et al. (2016). This not only improves the chemical stability and physical flatness of the Al_2O_3/ZnO interface but also decreases the interface state density (D_{it}). In recent years, by combining the optimization of the ALD process and the high-temperature post-annealing process, the interface state density of Al_2O_3 could be reduced to below $10^{12} cm^{-2} eV^{-1}$, and the series resistance Kim et al. (2018) could also be reduced.

Therefore, Al_2O_3 demonstrated significant potential in applications related to flexible electronics, low-power consumption, and wearable electronics due to the high dielectric constant and the high adaptability of the low-temperature ALD process.

However, some studies have also noted that low temperature deposited Al_2O_3 is not free from reliability concerns. Specifically, vacancies and leftover hydroxyl groups are potential charge trapping centres in the bulk dielectric or at the Al_2O_3/semiconductor interface Zhang et al. (2011); Nam et al. (2016); Tadmor et al. (2024). These stuck charges can cause hysteresis in the transfer characteristics, threshold voltage shifts caused by bias-stress interactions Castillo-Saenz et al. (2022b); Kwon et al. (2019); Tadmor et al. (2024) and subthreshold slopes. The low-temperature ALD procedures have a high tendency to incorporate a greater percentage of hydrogen that, although helpful in the passivation of defects, can also diffuse into the channel and change the carrier concentrations with time. Hence, conditions of deposition, post-annealing, and interface engineering are influential to dielectric quality of Al_2O_3 and the deposition conditions and interface engineering have to be carefully optimised to reduce these negative effects.

2.6 Optimization Strategies for Al_2O_3/ZnO Interface and Transistor Electrical Performance

The performance of ZnO-based TFTs is strongly dependent on the quality of the Al_2O_3/ZnO interface.Therefore, the optimization of this interface has become a critical research focus, with the deposition process being the primary step in determining interface quality. Key process parameters, such as deposition temperature, precursor dosage and purge time, as well as post-annealing treatments, play decisive roles in controlling interface defect states and improving device reliability. In addition, employing multi-layer dielectric stacks (for example, Al_2O_3 combined with high-k oxides) provides an effective strategy to modulate gate capacitance and further enhance transistor performance, which can efficiently reduce the defect of threshold voltage hysteresis Lee et al. (2020b).

Low-temperature (200 $°C$) plasma enhanced atomic layer deposition (PEALD) Al_2O_3 has been reported to exhibit excellent dielectric strength ($> 10.4 MV/cm$) after performing post-annealing Lee et al. (2016). Even at a relatively low deposition temperature of 70 $°C$ and without any post-annealing treatment, Al_2O_3 films deposited by PEALD can still achieve an acceptable dielectric constant of 7.6 and a dielectric strength of 5 MV/cm Castillo-Saenz et al. (2021).Table 2.1 summarizes reported works

in which Al_2O_3/ZnO thin-film transistors were widely adopted for their electrical performance. It could be observed that, although there are differences between the device structure and deposition method, the overall trend shows that low temperature deposited Al_2O_3 dielectric can maintain a low subthreshold slope (SS) and a high current on/off ratio while also having great interface stability. For example, a device employing AZO/Al2O3 deposited by PEALD at 150 °C exhibits a steep subthreshold swing (SS) of 190 mV/dec and a high current on/off ratio of 10^9, together with a relatively low interface trap density ($N_{it} = 1.8 \times 10^{-12}$ cm^{-2}) Rowlinson et al. (2022b). These results indicate that appropriate selection of the PEALD process and deposition temperature can effectively optimize the dielectric/semiconductor interface Castillo-Saenz et al. (2022c). In comparison, the ZnO-based TFTs, which were fabricated using traditional ALD with low deposition temperatures (80-100 $°C$), show higher SS Chen et al. (2021), a lower on/off ratio Dong et al. (2020), and a higher interface state density Chen et al. (2018), which indicates that the deposition method could optimize strategies. For the same device structure and the same deposition method, with different growth temperatures (100 $°C$ and 80 $°C$), the electrical performance and control of the interface states density can vary, which indicates that the growth temperature could be key to optimizing the interface quality and improving the electrical performance of a device. Overall, compared to traditional ALD, PEALD can reduce oxygen vacancies and carbon residues at low growth temperature ranges due to its plasma activation reaction characteristics Tadmor et al. (2024). Thereby, PEALD could provide better interface quality and electrical stability. This pattern provides an important reference for the selection of process windows and interface optimization strategies for subsequent Al_2O_3/ZnO TFTs.

TABLE 2.1: *Comparison of previously reported ZnO TFTs.*

Substrate/dielectric	Method	Growth temperature($°C$)	W/L (um)	SS (mV/dec)	I_{on}/I_{off}	Total Trap Density (D_{Total}) ($10^{-12}cm^{-2}$)	Charge trap density (N_{it}) ($10^{-12}cm^{-2}$)	Year/Ref
AZO/Al_2O_3	PEALD	150	50/3	190	10^9	-	1.8	2022/Rowlinson et al. (2022b)
Glass/Al_2O_3	PEALD	70	40/5	190	10^7	-	-	2022/Castillo-Saenz et al. (2022c)
p-Si/Al_2O_3	ALD	100	200/50	170	10^8	2.06	-	2021/Chen et al. (2021)
PET/Al_2O_3	ALD	100	100/10	210	10^7	-	-	2021/Dong et al. (2020)
p-Si/Al_2O_3	ALD	80	500/50	320	10^7	-	3.06	2019/Chen et al. (2018)

2.7 Fabrication Process of ZnO Thin Films

The fabrication process has the most straightforward effect on the electrical properties and working stability. The process of ZnO based TFT usually includes active layer

deposition, gate dielectric deposition, electron contact deposition, and post annealing. Moreover, for some special applications that avoid annealing to protect the substrate, such as flexible electronics, this approach is necessary. The deposition temperature window is crucial for growing a uniform, dense thin film with a low defect interface. This sub-chapter will summarize the deposition methods that people usually use and high-light the advantages of plasma enhanced atomic layer deposition (PE-ALD) technology in the Al_2O_3/ZnO system.

ZnO, as a channel layer in thin film transistors, has been deposited using various techniques, including chemical vapor deposition (CVD)Kaushik et al. (2018), pulsed laser depositionRodriguez-Davila et al. (2019), sol-gel processSalgueiro et al. (2017), sputteringZhu et al. (2021), and atomic layer deposition (ALD)Chen et al. (2020); Lin et al. (2023); Wang et al. (2023); Zhao et al. (2022). Compared with other deposition techniques, ALD becomes unique due to its precise thickness control, low roughness, and high uniformityProfijt et al. (2011b).

Table 2.2 summarizes the influence of ALD deposition processes on Al_2O_3/ZnO thin films and their electrical performance in recent years. All trends show that the choice of deposition method and oxygen source could affect device performance. For example, the Al_2O_3/ZnO thin film, deposited via the PEALD process with O_2 plasma as the oxygen source, can achieve a steep subthreshold slope of 130 mV/dec, a current on/off ratio of 10^9, and a high field effect mobility of 44.8 $cm^2/V{\cdot}s$, which indicates excellent interface control and electrical stability. In comparison, the thermal ALD process demonstrates limitations in achieving a high subthreshold slope and low mobility. There is another defect of thermal ALD: at the low deposition temperature window, the growth per cycle (GPC) rate is lower than that of the PEALD process, which could cause precursor waste issues Castillo-Saenz et al. (2022c); Profijt et al. (2011b).

TABLE 2.2: *Comparison of deposition techniques for ZnO thin films and their impact on TFT electrical performance.*

Structure	Method	Oxygen Source	Growth temperature($^\circ C$)	W/L (um)	SS (mV/dec)	I_{on}/I_{off}	$\mu_{EFF}(cm^2/V{\cdot}s)$	Year/Ref
Al_2O_3/ZnO	PEALD	O_2	190	50/3	130	10^9	44.8	2024/Rowlinson et al. (2024a)
Al_2O_3/ZnO	ALD	H_2O	175	10000/10	75.3	10^{12}	32.8	2023/Lin et al. (2023)
HfO_2/ZnO	ALD	H_2O	200	10/10	110	10^8	85	2023/Wang et al. (2023)
Al_2O_3/ZnO	ALD	O_3	200	40/5	195	10^9	-	2023/Zhao et al. (2022)
Al_2O_3/ZnO	PEALD	H_2O	70	40/5	207	10^7	-	2022/Castillo-Saenz et al. (2022c)
Al_2O_3/ZnO	ALD	H_2O	150	1000/80	490	10^7	12.4	2022/Yang et al. (2022b)

The oxygen source could also affect the surface. The oxygen source of H_2O could induce surface residual hydroxyl ($-OH$) groups due to an incomplete reaction at low

temperature, which could increase the interface states density. In comparison, the oxygen source of O_3 and O_2 plasma could have more advantages in improving film density and reducing defect density Tadmor et al. (2024).
In summary, the PEALD technique has become our choice because of its precise thickness control, uniform and clean surface, and high GPC within the deposition temperature window. Based on those advantages, the PEALD technique could theoretically ensure delivery of a better Al_2O_3/ZnO interface quality (uniform surface with low surface state density). This advantage not only ensures the stability and high mobility of TFTs but also provides a feasible path for flexible electronics and low-temperature process applications.

2.8 Research Gaps

In a systematic review of ZnO-based thin-film transistors (TFTs), ZnO and its derived multicomponent oxides (such as IGZO, ZTO, and IZTO) have demonstrated potential applications in displays, flexible electronics, and wearable devices due to their wide band gap, high mobility, and compatibility with low-temperature deposition processes. At the same time, the gate dielectric layer, especially the material with a high dielectric constant (Al_2O_3), has played a critical role in suppressing leakage current, improving interface state density (D_{it}), and increasing threshold voltage (V_{th}). Several studies show that interface quality is the key factor in determining the performance and reliability of ZnO-based TFTs. The critical parameters (such as PBS/NBS stability, SS, V_{th}, D_{it}) shifts are closely related to interface defects and trap states.
In terms of fabrication technology, the plasma-enhanced atomic layer deposition (PEALD) process could be a key method for depositing a high-quality ZnO and Al_2O_3 thin film at a low process temperature. However, the mechanism of adjusting different process conditions (such as plasma time, precursor dosage, purge time, and deposition temperature) at the Al_2O_3/ZnO interface is not fully understood. Especially for the Al_2O_3 deposition temperature window of 150-300 $^\circ C$, the mechanism for determining how the Al_2O_3/ZnO interface affects the dielectric strength, stability, and electrical performance of the transistor still needs to be studied.
Moreover, environmental stress (such as humidity, light, and temperature) often acts synergistically with electrical bias stress (PBS/NBS), making the Al_2O_3/ZnO interface

issues more complex. Currently, the solution (surface passivation, multi-dielectric layer, and annealing) either complicates the process or requires a high process temperature, which increases costs and makes it unsuitable for applications that require a low process temperature.
In summary, the research gaps and challenges in Al_2O_3/ZnO-based TFTs are in the following areas:

- The dynamic mechanism of the ZnO / Al_2O_3 interface is not clear. although it is known that D_{it} will cause V_{th} to shift, the mechanism behind the formation and release of interface traps under different process parameters is still incomplete.
- There is insufficient correlation between process-interface-TFT performance; in particular, there is a lack of systematic study of the quantitative relationship between deposition conditions (temperature, plasma environment) and transistor electrical characteristics under different environmental stresses.

2.8.0.1 Research Motivation

According to our group research, the device exhibiting sharp gate-edge geometry had already shown 2.7 μA of gate leakage current and the gate bias control loss at $V_d > 9$ V, in agreement with breakdown behaviour known for sharp-corner MOSFET structures. The gate sharp-corner issue has been well established as a cause of localized crowding of the electric field, which worsens short-channel control and device reliability Kansal and Medury (2019). The wet etching process that was used to pattern the AZO bottom gate Lan et al. (2024), however, was the key drawback in our case as it was the major cause of the sharp-corner defects. This problem was radically reduced by adopting a global-gate structure, where wet etching is not required to form gates. Although the global-gate structure effectively suppresses sharp gate-edge defects by eliminating wet gate etching, the insights gained from this approach may not be directly transferable to local-gate devices. In local-gate architectures, where gate patterning is unavoidable, additional process optimization is required to mitigate edge-induced electric-field crowding.
In the case of the global gate, we used highly doped Si as a bottom gate electrode rather than proceeding with AZO. The rationale is twofold. First, the Si substrate

offers a stable, high-conducting, and planar gate electrode, thus preventing the polycrystalline irregularities and etching-induced undercut typical of AZO films. Second, a Si global gate creates a clean baseline instrument with no structure related to the gate geometry, allowing us to concentrate on the intrinsic dielectric and interface behaviour without having to deal with structural defects.
It was based on this that we directed our study towards the Al_2O_3/ZnO interface that ultimately determines the long-term stability and reliability of the ZnO TFTs. Although an optimization of the gate geometry can be used to reduce local field concentration, the quality of the dielectric/semiconductor interface is the ultimate determinant of the device performance. Thus, we systematically examined the role of varying temperature of depositing Al_2O_3 in the interface defect states and associated them with electrical properties. The strategy does not only build on the previous effort to eradicate structural corner defects, but it also shifts the attention toward interface engineering that is the most important avenue to enhance the reliability of the ZnO TFTs to the next level of integration.
Based on known research gaps, this dissertation focuses on the statement of the following sections, which are informed by the research work that spans my PhD studies and aims to provide a deeper understanding of the interface of ZnO TFT and to lay a foundation for the development of future high stability, low-power consumption, flexible electronic devices.

- Section 1 (First 18 months): Systematic I-V characterization of the electrical properties of ZnO-based TFTs. The devices involved include the device with Al-doped ZnO (AZO) gate and AZO source drain contact. This background chapter will provide a fundamental understanding of the working mechanism of ZnO-based TFT. Combine experimental and simulation by inducing a localized gate structure defect through wet etching and further study the stability of the device under different operating electric fields. The analysis of the leakage path provides the foundation for subsequent research on the device interface.
- Section 2 & 3 (3rd year): By adopting a global gate structure of p-type silicon and aluminum as Source/drain contacts, a highly representative Al_2O_3/ZnO-based TFT is manufactured. Despite the elimination of the influence of structure and material, the effects of different PEALD deposition conditions (Al_2O_3 deposition temperature, plasma dose of ZnO deposition O_2) on the

electrical properties and stability of the device are studied. A correlation “model for "deposition condition, interface quality, and device performance” is demonstrated.

Chapter 3

Theoretical background of TFTs

This chapter introduces the theoretical background of metal oxide semiconductor field effect transistors (MOSFETs). As a sub-branch of MOSFET, thin film transistors (TFTs) are widely used in flexible electronics and displays due to their high transparency and mobility. As TFTs are a type of MOSFETs, the mechanism of MOSFETs could be applied to TFTs as well. Therefore, this chapter will introduce all parameters in general MOSFET discussions first. Then, the behaviour of the TFTs transistors is described, and extraction methods for essential parameters in this work are discussed. Finally, the focus will be on how they work in TFTs.

3.1 Capacitance Voltage (C-V) Characterization

Capacitance Voltage analysis is important to assess whether a device has a good gate oxide. The measurement data can be used to extract MOS device parameters (such as dielectric capacitance per unit area C_{ox} and interface state density D_{it} Novkovski (2017)). Additionally, the measurement data illustrate the operating characteristics of the device, including channel accumulation and channel depletion. A standard set-up for C-V measurement is the 2-terminal measurement, which is used to measure the device without a source or drain. The structure consists of 3 layers: metal, oxide, and semiconductor (MOS). The schematic graph is shown in Figure 3.1. The structures concerned here are the devices of my PhD work, which could provide a better understanding of the results. The schematic presents a comparison of the typical

working regions between p-Si MOS and n-type ZnO-TFT. For p-type MOS 3.1(a - c), holes accumulate when a negative gate voltage (V_G), which is less than the flat band voltage (V_{FB}), is applied to the gate. The measured capacitance ($C_{measure}$) is approximately equal to the oxide capacitance (C_{OX}). When the gate voltage moves forward and crosses the point of V_{FB}, the major carriers start to be pushed away from the gate side. Therefore, there will be a small depletion region and a depletion capacitance (C_{DEP}). The series capacitance of C_{DEP} and C_{OX} causes the decreased total capacitance. The depletion region will continue to increase as the applied voltage increases until it crosses the point of V_{TH}, at which point the device enters the full depletion region. For n-type ZnO TFT, due to the wide band gap, the minority carriers are difficult to move within the channel. Therefore, there is normally no inversion region. The most important property of the MOS capacitor is that its capacitance changes with the applied DC voltage. Based on the value of applied DC voltage, there are three operational modes: accumulation, depletion, and inversion. The information is a conclusion of Dolzhenko et al. (2018); Acharya et al. (2018); Hlali et al. (2016). However, for the thin film transistors, due to the highly doped channel, there are only fewer carriers that can form an inversion layer. Therefore, ideally, there would be a full depletion region rather than an inversion region.

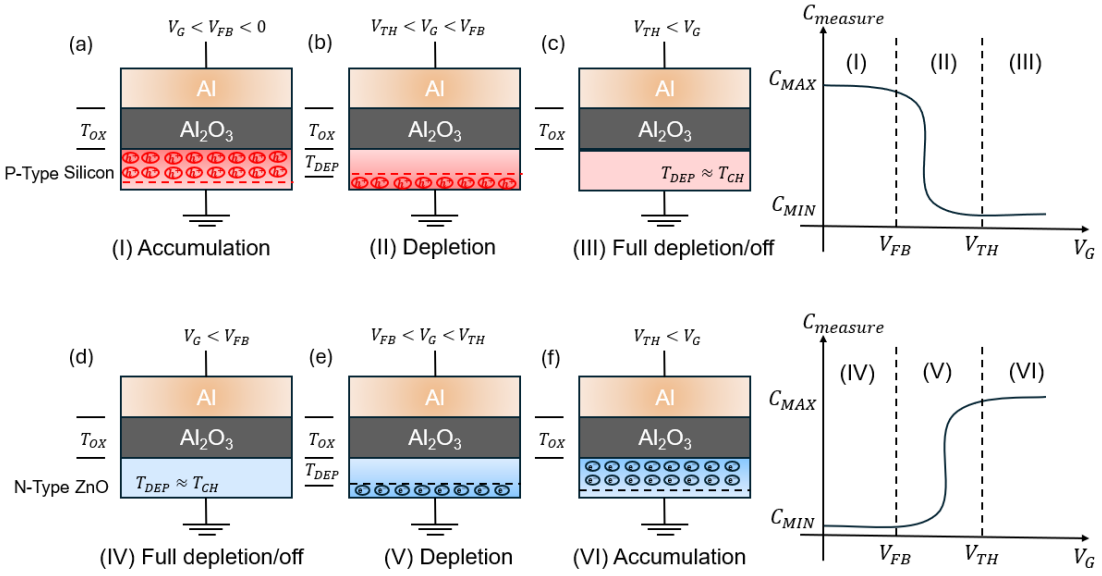

FIGURE 3.1: Schematic of channel switch mechanism, including accumulation, depletion, and off regions for both n-type and p-type TFTs. (a-c): p-type Si/Al_2O_3/Al structure. (d-f): n-type ZnO/Al_2O_3/Al structure. An ideal high frequency capacitance Voltage (C-V) characteristic is presented, where C_{MAX} and C_{min} represent maximum capacitance and minimum capacitance, respectively.

3.1.0.1 Accumulation Region

With no voltage applied, a p-type semiconductor has holes as the majority carriers in the valence band. In contrast, electrons serve as the majority carriers in the conduction band for n-type semiconductors. When a negative voltage is applied to the gate, due to the law of charge conservation, more holes appear in the valence band at the oxide-semiconductor interface. The accumulated positive charges (holes) at the interface between the semiconductor and the oxide, as well as the number of charge carriers in the oxide, equal the negative charge of the metal. For n-type semiconductors, since the major carriers are electrons, a positive voltage should be applied to the metal to accumulate an electron channel. Thereby, there would be negative charges (electrons) at the interface between the semiconductor and the oxide. At the strong accumulation region, due to the major carriers filling up the entire channel, the total capacitance is the oxide capacitance (C_{max}), which is measured when the applied voltage is sufficiently negative for the C-V curve to be nearly flat and constant. By applying a high frequency to offset the effect of trapped charge, the measured capacitance C_{MAX} is approximately equal to the oxide capacitance C_{OX}. Thus, the oxide thickness can be extracted from this value using equation 3.1, where A is the effective area, C_{OX} is the thickness of the oxide, and ε_{ox} is the dielectric constant. In our work, a Al_2O_3 dielectric constant of 8.6 is considered.

$$C_{OX} = \frac{A\varepsilon_{ox}}{T_{OX}} \tag{3.1}$$

Sometimes, for the relatively thin oxide ($< 5nm$), the C-V curve is not flattened in the accumulation region, and the measured oxide capacitance shows a different value from the actual oxide capacitance.

3.1.0.2 Depletion Region

When the applied gate voltage increases and reaches the flat-band voltage, the majority carriers (holes in p-type semiconductors and electrons in n-type semiconductors) are displaced from the semiconductor-oxide interface. This operational process is named depletion, since most carriers deplete the surface of the

semiconductor. In this region, the depleted area of the semiconductor can no longer conduct charge and functions as a dielectric or insulator.
At the strong depletion region, the gate voltage nearly reaches the threshold voltage. Due to the increase in gate voltage, the depletion region moves away from the gate, and the effective thickness of the dielectric between the gate and the semiconductor increases. The total capacitance becomes the sum of the oxide capacitance and the depletion layer capacitance in series. the measured capacitance decreases, and this capacitance is the minimum capacitance C_{min} of the MOS device.
For ZnO thin film transistors, since the n-type capacitance-voltage (C-V) curve is a mirror image of the p-type curve, the depletion region is the same as that of the p-type MOS device. However, the minimum capacitance point is the point at which the gate voltage equals the flat band voltage.

3.1.0.3 Inversion Region

As a p-type MOS device's gate voltage reaches and exceeds the threshold voltage, the positive gate voltage generates electron-hole pairs and attracts electrons toward the gate. In contrast, the negative gate voltage will attract holes toward the gate in an n-type MOS device. The insulating nature of the oxide confines minority (electron) carriers near the semiconductor–oxide interface, thereby promoting their accumulation at the interface. This layer formed by accumulation is called the inversion layer because the carrier polarity is inverted. As the gate voltage continues to increase, after reaching a specific positive gate voltage, most available minority carriers (electrons) in the semiconductor are located within the inversion layer. More gate voltage will not further deplete the semiconductor, and the slope of the C-V curve becomes flat. However, if the concentration of minority carriers is really low, there will not be a clear inverse relationship in the inversion region. For those wide bandgap semiconductors, such as ZnO, the minority carriers cannot move within the channel. Therefore, there will be a fully depleted region rather than an inversion region.
For the measured C-V curve, the inversion-region capacitance at the maximum depletion depth depends on the measurement frequency. C-V curves measured at different frequencies may yield different results due to interface trap defects.
As equation 3.1 shows, capacitance has a relationship with the thickness of $C \propto \frac{1}{T}$. Therefore, the maximum capacitance can be calculated when the thickness T_{ox} reaches

its minimum value, which should be measured in the accumulation region. Conversely, the minimum capacitance can be measured when the thickness T_{ox} reaches its maximum value, as it is in the fully depleted region.
For our device, to estimate simply, the minimum thickness($T_{ox,min}$) is the thickness of the dielectric layer (30 nm Al_2O_3), and the maximum thickness ($T_{ox,max}$) is the combined thickness of the dielectric layer and the semiconductor layer (40 nm ZnO).

$$T_{ox(nm)} = \frac{Ae_{ox}}{C_{ox}} \tag{3.2}$$

Table 3.1 shows parameter explanations and predictive details. The thickness of the minimum oxide layer is 30 nm, and the maximum oxide thickness is 70 nm. The permittivity of our oxide layer (ε_{r,Al_2O_3}) is 8.6, extracted from the C-V measurement, while the device's dimensions are measured using SEM. The SEM result shows that the channel width is 49 μm and the channel length is 2.9 μm. The complex permittivity of the oxide layer can be obtained by multiplying the permittivity by the permittivity of free space ($\varepsilon = \varepsilon_o \times \varepsilon_r$), which is 7.6×10^{-13} (F/m). Therefore, the maximum capacitance is 38 pF, and the minimum capacitance is 15.2 pF.

TABLE 3.1: *Predict and calculation value of capacitance in bottom gate TFTs*

Parameter	Definition	Predict Value
$T_{minimum}$	Oxide thickness (nm)	30
$T_{maximum}$	Oxide thickness (nm)	70
A	Gate area (μm^2)	150
e_{ox}	Complex permittivity of oxide layer (F/cm)	7.6
$C_{max,ox}$	Maximum Capacitance (pF)	3.8×10^{-2}
$C_{min,ox}$	Minimum Capacitance (pF)	1.52×10^{-2}
ε_r	Permittivity of Al_2O_3	8.6
ε_o	Permittivity of free space (F/m)	8.854×10^{-12}

3.2 Thin Film Transistor behaviour

The Current-Voltage (I-V) transfer characteristic is an important curve for predicting device performance. The carriers in the channel are electrons or holes. The device is divided into n-type (Carriers: Electrons) and p-type (Carriers: Holes). According to

the value of the threshold voltage, the transistor can operate in depletion mode, D-mode (threshold voltage, $V_{th} < 0$), or enhancement mode, E-mode (threshold voltage, $V_{th} > 0$). Therefore, due to material characteristics and the fabrication process, a MOSFET or a TFT can be a D-mode n-Type transistor, an E-mode n-type transistor, a D-mode p-type transistor, or an E-mode p-type transistor.
Since the device in this work is n-type, an n-type device will be discussed here as an example. To explain a TFTs switching process, a plot of drain voltage against gate voltage is shown in Fig 3.2. The dashed lines indicate schematic boundaries and idealized operating trends, marking the threshold voltage and the transition between subthreshold, linear, and saturation regimes.The red curve represents the enhancement mode device, while the blue curve represents the depletion mode device. For ZnO TFT in this work, the channel material ZnO is highly doped n^+ type and is in depletion mode (blue curve). Fig 3.2 shows how devices are affected by drain and gate voltages. The gate voltage (x-axis) determines whether the device is on or off. The different point is referred to as the threshold voltage. Before the threshold voltage ($V_{GS} < V_{th}$), the region is called the subthreshold region. in this region, the thin film transistor is off, and only a leakage current exists in the channel ($10^{-14}A$) due to the highly doped channel, and the current is a drift-current. Moreover, no matter how the drain voltage increases, the current will not increase in this region. Once the gate voltage reaches a threshold voltage ($V_{GS} > V_{th}$), the transistor is turned on. In this region, depending on the value of the drain voltage, the transistor can operate in the linear region ($V_{DS} < V_{GS} - V_{th}$) or the saturation region ($V_{DS} > V_{GS} - V_{th}$). the so-called linear region means that with an increasing drain voltage, the drain current will also increase. In contrast, the saturation region indicates that the drain current no longer increases even as the drain voltage increases.

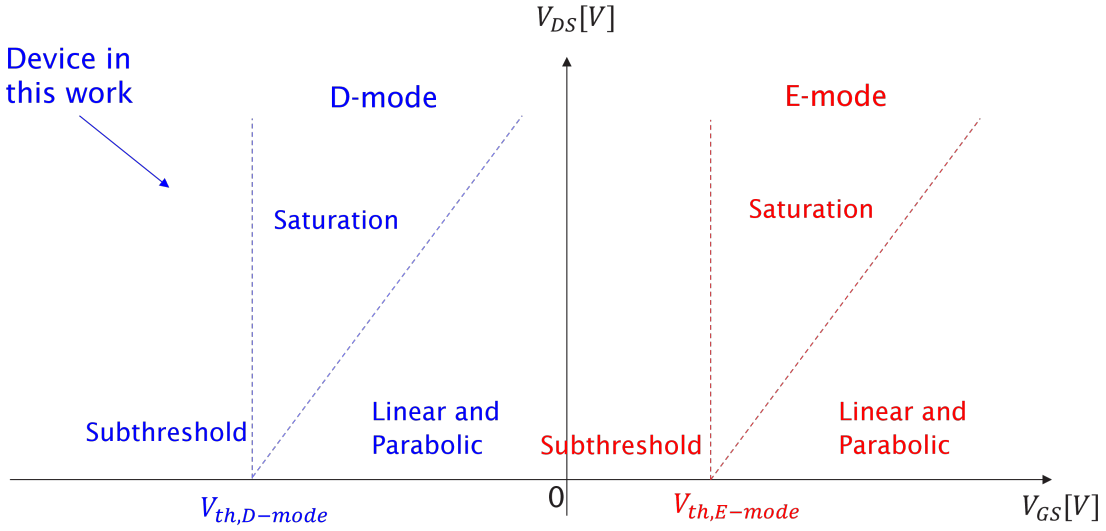

FIGURE 3.2: Graph illustrating the operation regions for D-mode TFT (Blue) and E-mode TFT (Red).

A standard n-type I-V transfer curve is shown in Fig 3.3. The figure explains how the drain current changes in the linear and saturation regions, where the x-axis represents the drain voltage and the y-axis represents the drain current. In general, the device can operate in a linear region and a saturation region. However, according to the relationship between drain current and drain voltage, the linear region can be divided into linear and parabolic regions. In summary, once the gate voltage reaches a threshold voltage, with the increasing drain voltage, the device can operate in I. the linear region, II. the parabolic region, and III. the saturation region.

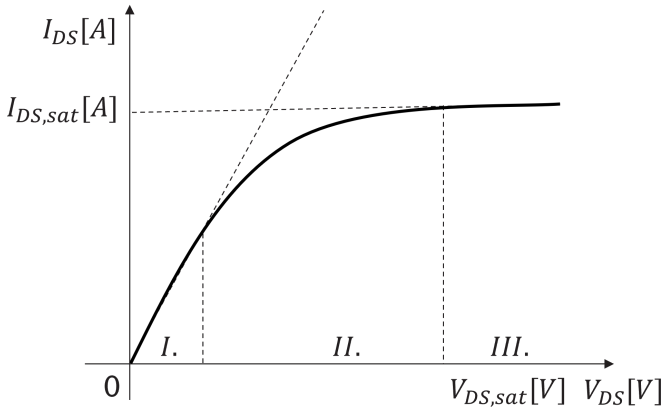

FIGURE 3.3: I_{DS} $Vs.$ V_{DS} curves for a typical n-type TFT.

3.2.0.1 Linear Region

When the drain voltage is low biased ($V_{DS} \ll V_{GS} - V_{th}$), the thin film transistor is in the linear region and shows a linear relationship of $I_{DS} \propto V_{DS}$. the drain current equation can be expressed as (3.3).

$$I_{DS(lin)} = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_{th}) V_{DS} \tag{3.3}$$

Where μ_{eff} is the field-effect mobility, C_{ox} is the oxide capacitance, W is the channel width, and L is the channel length. Therefore, the accumulation process occurs in this region. The schematic of a channel is shown in Fig 3.4. Due to the gate bias, most carriers accumulate at the interface between the semiconductor and the oxide. Moreover, the channel is not affected by the vertical electric field in this region because of the low drain voltage. The value of current in this region mainly depends on the magnitude of the gate voltage.

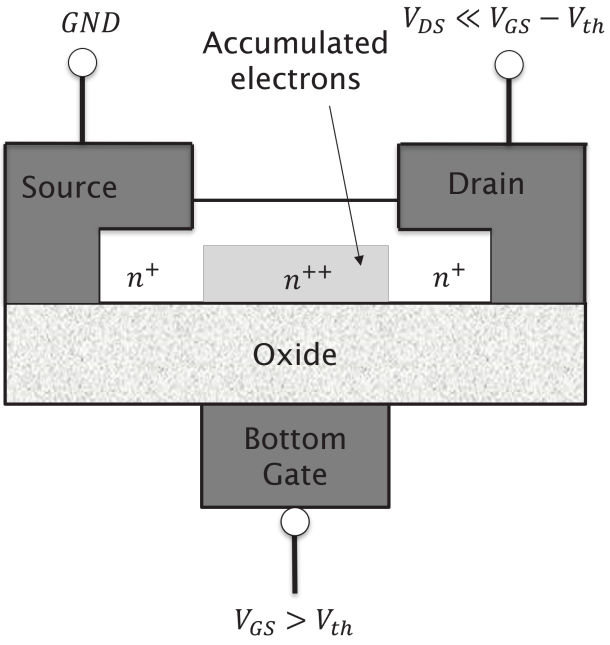

FIGURE 3.4: The schematic shows accumulation process of D-mode TFT in this work.

3.2.0.2 Parabolic Region

When the drain voltage slightly increases ($V_{DS} \leq V_{GS} - V_{th}$), a relation of $I_{DS} \propto -V_{DS}^2$ can be observed. The drain current in this region can be expressed as (3.4).

$$I_{DS(para)} = \mu_{eff} C_{ox} \frac{W}{L}((V_{GS} - V_{th})V_{DS} - \frac{mV_{DS}^2}{2}) \tag{3.4}$$

Where m represents the channel capacitance, it can be expressed by the equation (3.5). It includes maximum depletion capacitance, $C_{dep(max)}$, in Strong inversion ($\psi S = 2\psi B$), and includes the sum of additional parasitic capacitance. The parasitic capacitance consists of defects at the dielectric-channel interface, C_{dc}, dielectric charges (C_{di}), overlap capacitance at the gate-source $C_{(ov,gs)}$, and gate-drain $C_{(ov,gd)}$. To simplify the calculation process, the maximum depletion width is considered to be the channel thickness (the channel is fully depleted), which is 30 nm in my device. The parasitic capacitance is neglected for simplicity in the analysis because it is too small, and from the other's work (Dolzhenko et al. (2018); Norton et al. (2004)), the permittivity of the semiconductor, 40 nm ZnO in this work, is 8.6, while the permittivity of the oxide, 30 nm Al_2O_3, is 8.5. The channel capacitance coefficient in calculation can be expressed as equation (3.6), and the calculated value is m = 1.76.

$$m = 1 + \frac{C_{dep(max)}}{C_{ox}} + \frac{C_{dc} + C_{di} + C_{ov,gs} + C_{ov,gd}}{C_{ox}} \tag{3.5}$$

$$m \approx 1 + \frac{\varepsilon_{ZnO} t_{Al_2O_3}}{t_{ZnO} \varepsilon_{ox}} \tag{3.6}$$

Due to the higher drain voltage, the accumulation layer is affected by a vertical electric field. As Fig 3.5 shows, a higher vertical electric field causes a small depletion region between the accumulation region and the drain. Therefore, the accumulation area is reduced, and if the drain voltage continues to increase to the pinch-off point ($V_{DS} = V_{GS} - V_{th}$), the transistor enters the saturation region.

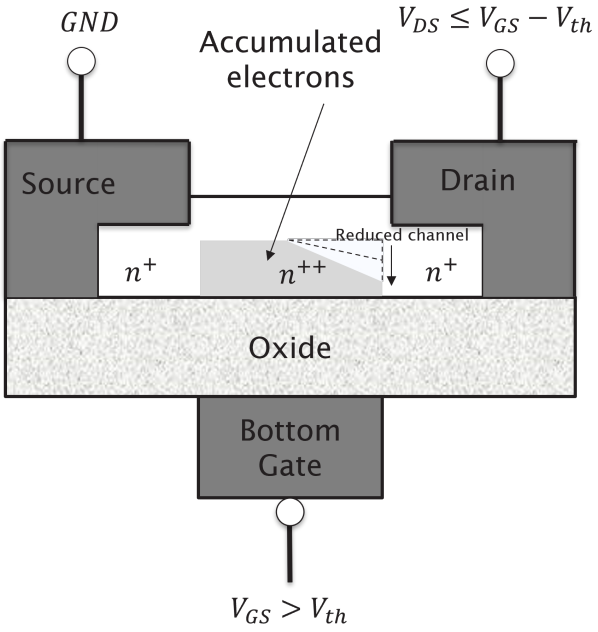

FIGURE 3.5: The channel effective length is reducing due to higher drain voltage.

3.2.0.3 Saturation Region

If the drain voltage continues to increase and reaches the pinch point ($V_{DS} > V_{GS} - V_{th}$), the channel becomes highly constricted and is pinched-off at the drain electrode. the drain current can be expressed as (3.7).

$$I_{DS(sat)} = \mu_{eff} C_{ox} \frac{W}{L} \frac{(V_{GS} - V_{th})^2}{2m} \tag{3.7}$$

The pinch-off point is shown in Fig 3.6. Due to the vertical electron field from the drain voltage in the channel, the region of high electron concentration is completely pinched-off. Therefore, if the drain voltage keeps increasing, the current will start to decrease because the "channel length" is decreased.

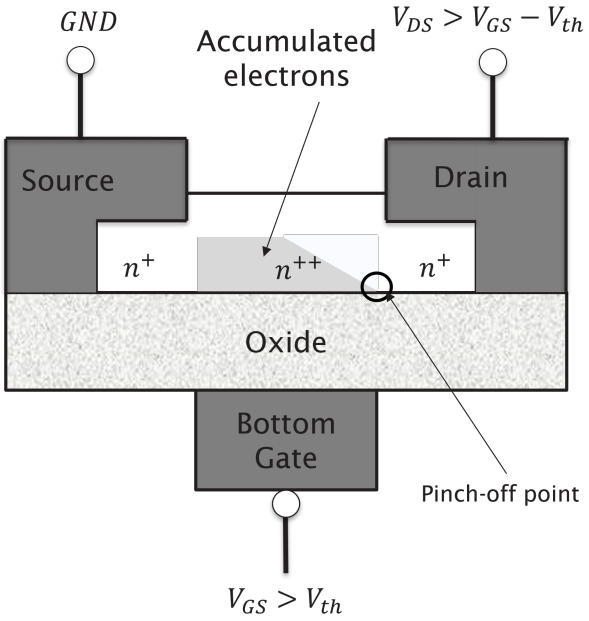

FIGURE 3.6: The pinch-off point appears because of high drain voltage.

3.2.1 Sub-threshold Slope (SS)

Subthreshold Slope (SS) is measured as the steepest gradient from the logarithmic plot of the drain current against the gate voltage in the subthreshold region. The unit is mV/dec. As shown in Fig 3.7. Since the D-mode n-type TFT has been studied in this work so far, the schematic is provided for the D-mode n-type device, and the value of the threshold voltage is negative. From the schematic graph, the on current and off current can be observed, and the value of SS can be calculated as shown in equation (3.8). The equation shows that the value of SS is highly relative to the channel capacitance coefficient, $SS \propto m$. As equation (3.5) shows, the lowest value of m is 1. Therefore, the lowest value of SS is 60 mV/dec at room temperature, where $ln(10) = 2.3$, $\frac{kT}{q} = 25mV$.

Furthermore, since the value of parasitic capacitance cannot be analytically determined and is neglected, based on the found value of oxide capacitance and depletion capacitance, the value in this work has been predicted to be 1.76. This way, an SS of 105.6 mV/dec can be calculated. Subsequently, the measured SS should be higher than this value because of the parasitic capacitance in the real device. According to the measured value, the value of parasitic capacitance can be estimated roughly.

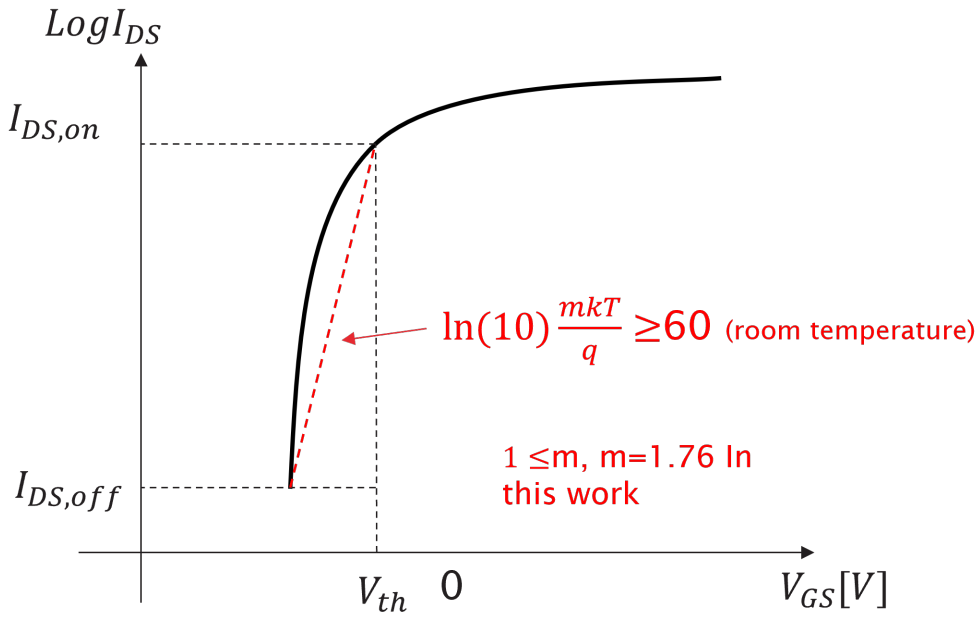

FIGURE 3.7: A schematic shows indicate the calculation of Subthreshold Slope plot.

A typical experimental subthreshold slope for a scaled MOSFET at room temperature is 70 $\frac{mV}{dec}$ Auth et al. (2012). The slight difference is due to the parasitic capacitance of short-channel MOSFET. An a-IGZO TFTs transistor shows an SS of 600 $\frac{mV}{dec}$, and it has been used to integrate as an inverterLin et al. (2019). In future circuit design, a steep subthreshold swing (SS) is expected in logic circuit design because a steeper SS means faster switching due to low parasitic capacitance. A measured SS of around 200 mV/dec is expected in this work.

$$SS = ln(10)\frac{mkT}{q} \tag{3.8}$$

3.2.2 Threshold Voltage (V_{th})

The threshold voltage, V_{th}, is commonly used to indicate the gate bias at which a measurable conducting channel is established and the drain current begins to rise rapidly. In ZnO-based TFTs fabricated in this work, the device operation is better described in terms of *accumulation* rather than inversion. ZnO is an n-type oxide semiconductor, and under a sufficiently positive gate-to-source voltage V_{GS}, electrons are electrostatically attracted towards the ZnO/Al_2O_3 interface, forming an electron-accumulation layer that serves as the conduction channel. In this context, V_{th} corresponds to the gate bias at which the surface electron concentration becomes high

enough for the channel to percolate and for the device to enter the high-conductance regime. Unlike classical inversion-mode MOSFETs, where V_{th} is often defined by the onset of strong inversion and a surface potential of approximately $2\phi_F$, the accumulation-mode ZnO TFT does not require the formation of a minority-carrier inversion layer. Instead, the gate field modulates the majority-carrier (electron) density near the interface, and the effective surface potential is governed by the balance of the oxide electric field, the space-charge in the semiconductor, and trap charging at or near the ZnO/Al_2O_3 interface. Therefore, the physical meaning of V_{th} in an accumulation-mode TFT is operational: it is the gate bias at which the accumulated electron sheet density and percolation pathways in the polycrystalline/amorphous oxide channel become sufficient to yield a rapid increase in I_{DS}. After the transfer

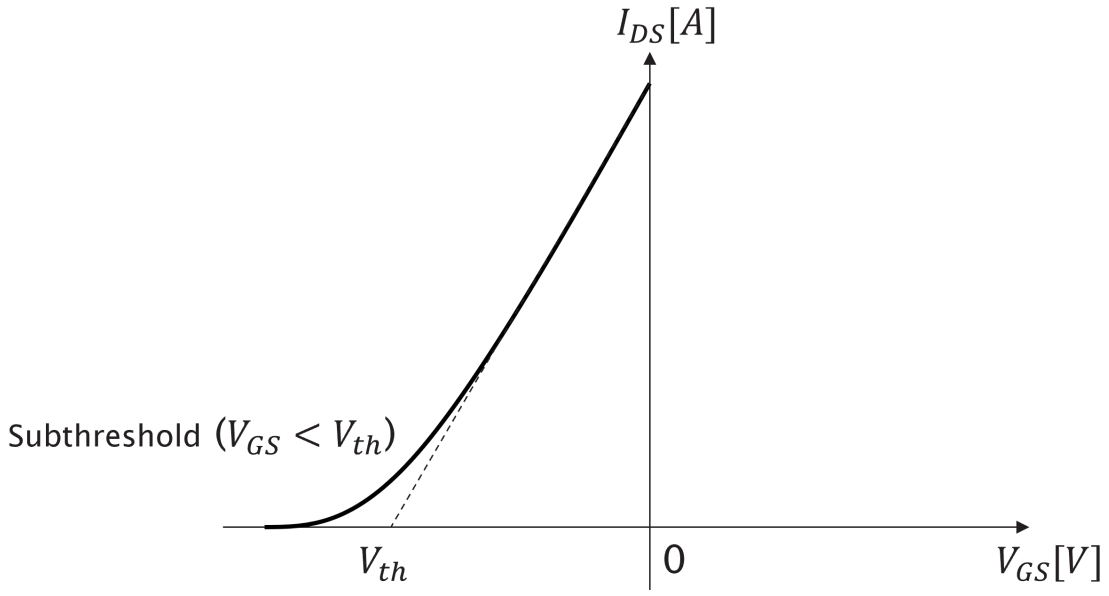

FIGURE 3.8: I_{DS} Vs V_{GS} curve for a typical D-mode n-type TFT with gradient used for threshold voltage.

measurement, V_{th} can be extracted from the I_{DS}–V_{GS} characteristics using a consistent extraction method (e.g., the linear extrapolation method in the linear regime), as illustrated in Fig. 3.8. The devices in this thesis exhibit depletion-mode behaviour, evidenced by a negative extracted V_{th}. This is consistent with a relatively high intrinsic electron concentration in the ZnO film, such that a finite channel conductance exists even at $V_{GS} = 0$ V and a negative gate bias is required to deplete the accumulated carriers and switch the device towards the off-state.

3.2.3 Threshold Voltage Hysteresis (ΔV_{hys})

The threshold voltage hysteresis in TFT is the main issue that affects transistor stability and reliability. The hysteresis is influenced by interface traps, charge trapping and releasing, and oxygen vacanciesJo et al. (2014); Kandpal et al. (2020); Zalte et al. (2021); Murugan and Lee (2022); Zhou et al. (2023); Kim et al. (2025). The charge trapping will increase under conditions of positive bias stress, negative bias stress, and optical measurement, inducing a greater threshold voltage shift and hysteresis. The interface constructed from different semiconductors and oxides, under various processing conditions, can affect the hysteresis phenomenon.
The most common evaluation method of threshold voltage hysteresis is the I-V sweep in both directions (forward and reverse): Directly evaluate the threshold hysteresis from the difference between $V_{th,forward}$ and $V_{th,reverse}$ as shown in figure 3.9 Kwon et al. (2019); De Rosis et al. (2024). Combining the analysis of the C-V characteristic and trap density, the contribution of interface traps to hysteresis could be evaluated.

3.2.4 Interface Trap Density (D_{it})

Interface trap density (D_{it},$cm^{-2}eV^{-1}$) presents a significant effect on TFT performance. An accurate extraction of interface trap density is very important to evaluate the reliability and improve device performance. In recent years, according to thin film transistors with different structures, a number of extraction methods have been presented to evaluate the interface trap density. Subthreshold method: subthreshold slope is a critical parameter to evaluate the switch characteristic; the offset of SS is mainly affected by interface trap density (D_{it}). The extraction D_{it} from SS is the most convenient and straightforward method, as shown in equation 3.9 Zhengfan et al. (2007).

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{SS}{SS_0} - 1 - \frac{C_{dep}}{C_{ox}}\right) \tag{3.9}$$

Under the condition of $C_{dep} \ll C_{ox}$, the equation 3.9 could be simplified as $D_{it} \approx \frac{C_{ox}}{q}\left(\frac{SS}{SS_0} - 1\right)$, where C_{ox} is oxide capacitance per unit area, and $SS_0 = (kT/q)\ln 10 \approx 59.6\text{mV/ dec}$ @300 K. However, some methods such as (Terman method Deen and Champlain (2011), Conductance method Çetinkaya et al. (2024),

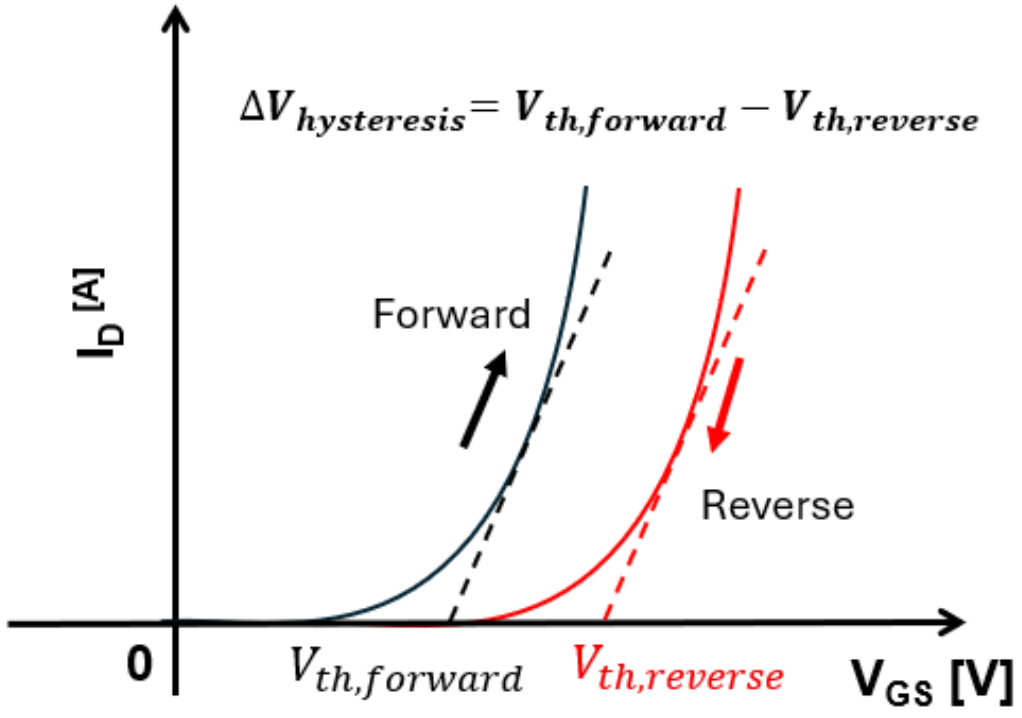

FIGURE 3.9: Schematic of hysteresis extracted from the transfer characteristic. Measuring the forward (black) and backward (red) I_D Vs. V_{GS} transfer characteristic under fixed drain voltage (V_{DS}). The dashed line indicates the linear extrapolation of threshold voltage. The hysteresis is defined as the difference between $V_{th,forward}$ and $V_{th,reverse}$.

Hysteresis/bias stress method Illarionov et al. (2017)) have also been used to extract (D_{it}).

3.2.5 Gate Leakage Current (I_g)

The leakage current is typically defined as the current that leaks between the drain and source when a MOSFET is OFF ($V_{GS} < V_{TH}$). typically, the value of the leakage current is low, at $10^{-12}A$, and this current comes from carrier drift. However, sometimes, people also mention gate leakage and body leakage.
Gate leakage is defined as the unexpected current that passes through the gate oxide to the drain or source. A high gate leakage can cause devices to lose their transistor behaviour. A body leakage current refers to the current from the drain or source to the device's body. Gate leakage and body leakage occur regardless of whether the device is

on or off. The schematic graph is shown in Fig 3.10. Since the body is a TFTs semiconductor, the body leakage is included in the normal leakage.

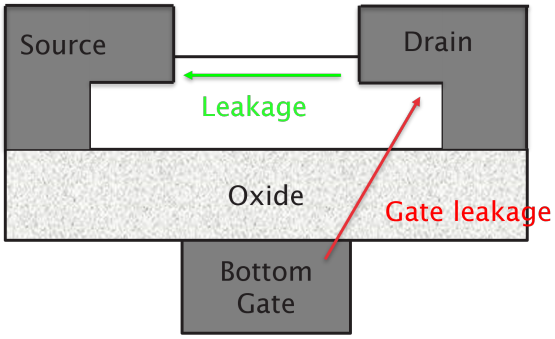

FIGURE 3.10: A schematic shows leakage direction of leakage current in Bottom gate TFTs.

For D-mode TFTs in this work, a gate leakage issue has been identified through simulation and measurement. The detailed analysis is provided in *Chapter 5*, and the solution will be presented in future work.

3.2.6 Field Effect Mobility Extraction (μ_{eff})

The field effect mobility (μ_{eff}) physically denotes how quickly an electron can move through a semiconductor when an electric field is applied. The unit is $cm^2/(V^{-1}S^{-1})$. In the literature report, two types of mobility are generally mentioned. One is hall effect mobility, and the other is field effect mobility. Hall effect mobility can be measured by conducting hall effect measurements. However, hall effect mobility is more accurately described for intrinsic material characteristics. It is limited to showing the effects of the dielectric interface and the source-drain contacts.
Compare with hall mobility. The field effect mobility is better at explaining the available mobility in the entire device. Therefore, if the mobility of a single-layer semiconductor needs to be known, a Hall measurement is required. However, field-effect mobility is a more representative metric for evaluating the overall device performance. Unfortunately, although many groups have mentioned the value of field effect mobility from their devices, not many people have explained how they calculated it. Therefore, the methods introduced in this work are intended solely to compare each device.
To extract the field effect mobility of the device, firstly, the channel conductance (g_d) and transconductance (g_m) can be extracted from the measured I-V transfer

characteristics. Channel conductance is extracted for low-field linear region mobility calculations, and transconductance is extracted for high-field saturation region mobility calculations. The equation and extraction methods are shown in Fig 3.11, where the left one is the $I_{DS} - V_{GS}$ curve for a D-mode TFT, and the right one is the $I_{DS} - V_{DS}$ curve for a D-mode TFT, both with gradients used to extract transconductance (g_m) and channel conductance (g_d).

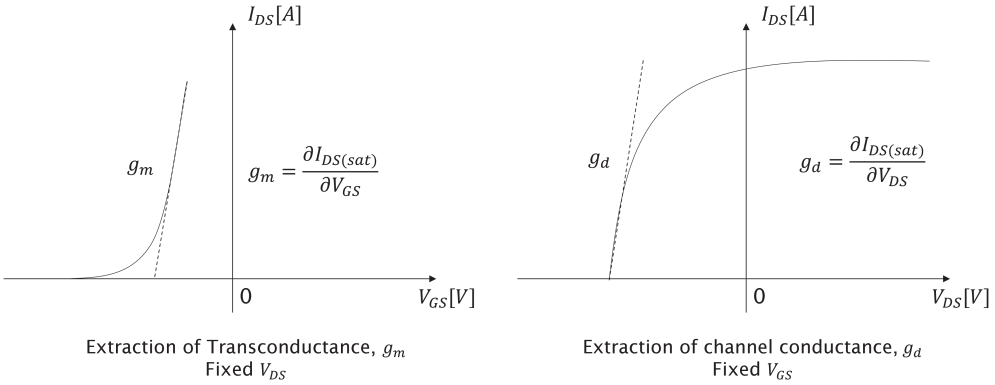

FIGURE 3.11: Two I-V curves with gradient used for the transconductance (Left) and channel conductance (Right) extraction methods.

3.2.6.1 Linear Region ($V_{TH} < V_{DS} < (V_{GS} - V_{TH})$)

For the low-field linear mobility extraction, the value of channel conductance is extracted first. From the I-V transfer characteristic 3.11, the channel conductance can be expressed as equation (3.10).

$$g_d = \left.\frac{\partial I_{DS,linear}}{\partial V_{DS}}\right|_{V_{GS}=constant} \tag{3.10}$$

The linear region has been introduced, and the drain current can be calculated using equation (3.3). Therefore, the channel conductance can be simplified as equation (3.11).

$$g_d = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}=constant} = \mu_{eff} C_{ox} \frac{W}{L}(V_{GS} - V_{th}) \tag{3.11}$$

The low field mobility, $\mu_{eff,linear}$, can be extracted by rearranging this equation, as shown in (3.12). Oxide capacitance can be calculated or measured. Channel conductance can be extracted from I-V measurement data. Dimension size can be

measured using SEM measurements.

$$\mu_{eff,linear} = \frac{Lg_{d,linear}}{WC_{ox}(V_{GS} - V_{th})} \tag{3.12}$$

3.2.6.2 Saturation Region ($V_{DS} > (V_{GS} - V_{TH})$)

The transconductance value is extracted first for the high-field linear mobility extraction. From the I-V transfer characteristic 3.11, Left, for the saturation region (equation (3.7)), transconductance can be expressed as equation (3.13). The field effect mobility can be expressed as (3.14).

$$g_m = \left.\frac{\partial I_{DS,sat}}{\partial V_{GS}}\right|_{V_{DS}=constant} = \mu_{eff}\frac{WC_{ox}}{Lm}(V_{GS} - V_{th}) \tag{3.13}$$

$$\mu_{eff,sat} = \frac{Lg_{m,sat}m}{WC_{ox}(V_{GS} - V_{th})} \tag{3.14}$$

In summary, this chapter explains and links the general background knowledge between general MOSFET and depletion mode TFT of this work. First, the capacitance-voltage curve is introduced, and the operating modes of accumulation, depletion, and inversion are also explained. It also helps people understand how the gate affects the channel. Then, a predicted value of maximum capacitance, 38 pF, and minimum capacitance, 15.2 pF, is calculated. Subsequently, a section named *Thin film transistor behaviour* shows the difference between transitional MOSFET and TFTs. Furthermore, based on the characteristic of the TFT in this work (D-mode n-type TFT), a $I_{DS} - V_{DS}$ plot is shown to explain how the device operates in the linear, parabolic, and saturation regions during drain voltage changes. Some critical parameters are explained, such as SS, threshold voltage, leakage current, and field effect mobility, which are essential for future circuit work. In *Chapter 5*, these values will be compared with the measured results.

Chapter 4

Fabrication and measurements set up for TFTs

This chapter summarizes all the device design, fabrication options, and measurement set up involved in the current PhD project. A total of 3 devices were designed based on different research objectives, including a device with AZO as the gate material and two devices with Si as the gate material.

Devices with AZO (Al-doped Zinc Oxide) as the gate material include dual gate structures (top and bottom gates) (Fig. 4.1 . Devices with p-type Silicon as the gate material are all Global Bottom Gate structures, but they use different dielectric layer materials, specifically silicon oxide (SiO_2) and aluminum oxide (Al_2O_3) (Fig. 4.2 (I.)). 5 different channel widths are designed for each structure, which are 2 um, 5 um, 10 um, 20 um, and 50 um 4.2 (III.). In addition, a scanning electron microscopy (SEM) image of a Global Bottom Gate device with a channel width of 50 μm is provided (Fig. 4.5).

Electrical characteristic measurements are a key step in verifying the performance of these devices. The experimental setup for electrical characteristic measurements is also described in detail in this chapter. The first designed device is a ZnO dual gate TFT. The device demonstrates a step subthreshold swing of 110 mV/dec and a high current On/Off ratio of 10^8. Moreover, with a drain bias voltage of 5 V, the leakage current (I_{gs}) is only $3 \times 10^{-13} A$. However, above a drain bias voltage of 5 V, the gate leakage current starts to increase unexpectedly. (I_{gmax} of $8.5 \times 10^{-7} A$, through multiple verification methods (TEM,FIB, Silvaco simulation), the sharp corner of the bottom

gate is suspected to be the source of this high leakage, which reduces the gate's control over the channel, resulting in a decrease in source leakage current. Therefore, the global bottom gate structure of the ZnO TFT is designed and fabricated. The dielectric material and channel material might be potential reasons that cause this issue. To investigate the optimization strategies for Al_2O_3/ZnO interface and transistor electrical performance, a p-type silicon global bottom gate structure is designed.

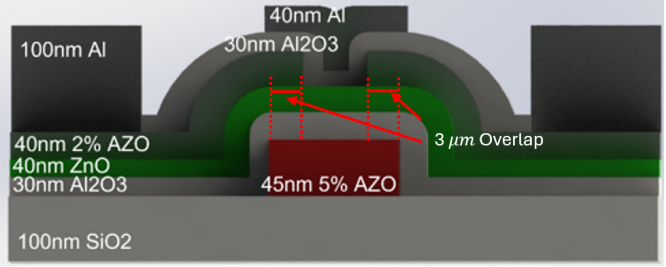

FIGURE 4.1: Cross view for duel-gate device. Layer thickness from bottom to top, 100 nm SiO_2 as Substrate, 45 nm 5% AZO as Bottom Gate(BG), 30 nm Al_2O_3 as BG dielectric layer, 40 nm ZnO as Channel Layer, 40 nm 2% AZO as Source/Drain Layer, 40 nm Al_2O_3 as Passivation Layer, 100 nm Al as Metal Contact.

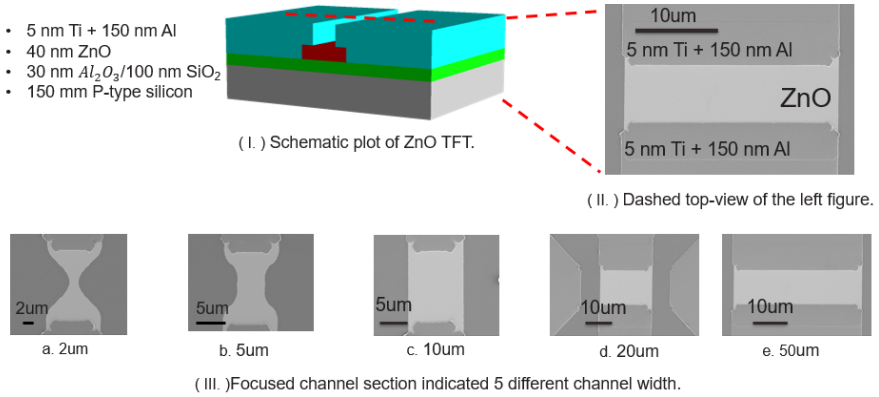

FIGURE 4.2: The schematic plot and SEM image of global bottom gate ZnO TFT device with different channel widths. (I.) 3D schematic plot: from bottom to top are p-type Si (GBG)/ gate dielectric (30 nm Al_2O_3 or 100 nm SiO_2) / 40 nm ZnO channel / 5 nm Ti + 150 nm Al Source/Drain metal. (II.) A zoom in top view of the dashed box area in (I.), showing the overlap between the ZnO channel ($W_{ch} = 50um$) and the source/drain. (III.) SEM top view focused on channel area, 5 different channel widths are presented: 2 um, 5 um, 10 um, 20 um, and 50 um.

For the smallest devices (2–5 μm), the effective width (and thus the effective W/L) is subject to increased uncertainty due to lithography and etch bias/undercut at the channel edges. Therefore, the reported widths for these devices should be interpreted as *design* values rather than precisely metrologically verified dimensions, and any

parameters that scale with W/L (e.g., extracted mobility) may carry a larger systematic uncertainty for the smallest-W devices.

4.1 Fabrication Process

4.1.1 Wafer Preparation

Wafer preparation is always the first step in fabrication Franssila (2010). In this work, a 6-inch 150 nm dummy Si wafer is involved and is cleaned using the standard processing cleaning steps. First, the wafer is immersed in the RCA1 solution ($NH_4OH : H_2O_2 : H_2O - 1 : 1 : 5$) to remove organic residues. The recipe takes 10 minutes and 50 $°C$. The wafer is then first immersed in Fuming Nitric Acid (99.5 $\%HNO_3$) for 10 min to remove oxidized organic residues. After that, the wafer is immersed in RCA2 solution ($HCL : H_2O_2 : H_2O - 1 : 1 : 6$) to remove metal particulates. The recipe is 10 mins and 50 $°C$ as well. Between each step, the wafer is rinsed in deionized water (DI) for 10 min to remove the reactants, and after all the processes, the wafer is dried on the spin machine.
After cleaning, the wafer is immediately placed in a dry oxide machine, and a 100 nm layer of SiO_2 is heated to act as an insulating layer. The recipe is 1000 $°C$ and 260 min.

4.1.2 Fabrication Steps

The fabrication steps in Appendix Table A.1 summarize dual-gate TFTs with an Al top gate. These fabrication steps can also be used for top- and bottom-gate structures, but the fabrication process would be relatively more straightforward. Due to the sharp corner issue, a global bottom gate device has been designed, and the fabrication steps are shown in Appendix Table **??**. In addition, the fabrication process for the Si bottom gate devices is provided in Appendix Table A.3.

4.1.2.1 Dual Gate Fabrication Process

The fabrication process for the preparation of Dual Gate Devices is provided in this subsection, as shown in Appendix Table A.1. The first column of the table is the step number, and the second column provides a detailed description of each step, including the technique used, the materials, and the ratio of chemical solutions. The third column shows a schematic cross section of the device corresponding to the current step, and the last column shows a top view of the current step.

4.1.2.2 Al Doped Zinc Oxide Global Bottom Gate Fabrication Process

The fabrication process for the preparation of AZO Global Bottom Gate Devices is provided in this subsection, as shown in Appendix Table **??**. The table has the same structure as the previous table.Global Bottom Gate avoids the gate sharp corner defect compared to conventional Square Bottom Gate. In terms of fabrication process, because the Global Bottom Gate does not require patterning, the deposition of the dielectric layer can be performed immediately after the deposition of the bottom gate without causing a break in vacuum, resulting in a tighter contact surface between the bottom gate and the dielectric layer.

4.1.2.3 Si Global Bottom Gate Fabrication Process

The fabrication process for the preparation of Si Global Bottom Gate Devices is provided in this subsection, as shown in Table A.3. This preparation process was used to make two devices with different dielectric layer materials: silicon dioxide (SiO_2) and aluminium trioxide (Al_2O_3). Therefore, in Table A.3, step 2 is divided into two parts: the growth of the silica dielectric layer and the deposition of the aluminium trioxide dielectric layer. During aluminium trioxide deposition, in this study four different deposition temperatures (150 $°C$, 200 $°C$, 250 $°C$, and 300 $°C$) were used to investigate the effect of temperature on the dielectric constant of the dielectric layer.

4.1.3 Fabrication: Dual Gate ZnO TFT

4.1.3.1 Step 1: AZO Bottom-Gate

The first layer of TFT is a 45 nm 5% Al doped ZnO layer, which PEALD deposits with Diethyl Zinc (DEZ) and Trimethyl Aluminum (TMA) precursors. A DEZ precursor reacts with H_2O to form ZnO, the reactants are $Zn(C_2H_5)_2/H_2O$ Oviroh et al. (2019), and aluminum is extracted from TMA with H_2O. In this process, every PEALD process is completed via Oxford Plasma Tools' FlexAl machine. Before depositing material, the wafer is heated to 175 $°C$ and kept at this temperature during processing. Proper adhesion can be promoted and the material will have high density and quality. The pressure for DEZ is 150 mTorr, for TMA is 80 mTorr, and for the chamber, the temperature is 15 mTorr. The initial step is plasma O_2 at 300W to clean the chamber for 30 seconds. The structure schematic of AZO is shown in Fig. 4.3. As the schematic graph shows, the AZO is deposited by stacking ZnO and Al, repeatable. To deposit 45 nm 5% AZO, 272 cycles are required, 12 super cycles are included; a super cycle means that 2.76 nm ZnO and 1 nm Al are deposited. The recipe is shown in Table 4.1.

TABLE 4.1: *The recipe of depositing 5 % AZO used Flex AL machine*

Step No.	Chamber Input	Pulse Duration
1	DEZ Burst	125 ms
2	DEZ-purge	3 s
3	H_2O Dose	150 ms
4	H_2O-purge	1s
5	TMA Burst	20 ms
6	TMA-purge	3s
7	H_2O Dose	100ms
8	O_2-purge	1s

The AZO bottom gate is patterned by PL using S1813 Photoresist from MicroPosit. The resist is spun at 5000 rpm (resist thickness $\approx 1\ \mu m$), soft baked at 115 $°C$ for 60 s, then exposed under a Hg-vapor UV lamp without filtering for 2.2 s; the contact mode is soft contact. The exposed resist is developed for 40 s (35 s - 40 s) in the MF-319 developer solution (2.45 % TMAH in H_2O with surfactants). This is the standard recipe for S1813, which is normally used in this fabrication process.

After the pattern process, the bottom gate is wet etched using a 1:1000 solution of 36 % HCl at a mean rate of 2.2 nm/s at room temperature. An etch time of 18 s is required

for 45 nm AZO. This is the standard wet-etch recipe for AZO and ZnO. The result was stripped in NMP for 60 s at room temperature and cleaned with Acetone and IPA.

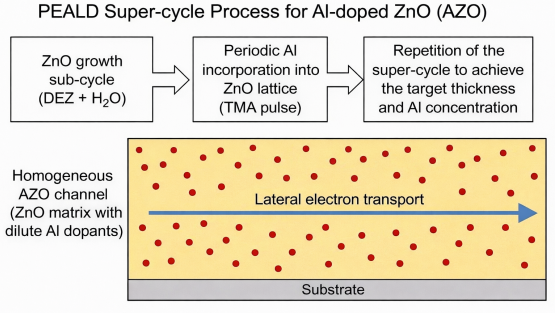

FIGURE 4.3: Schematic illustration of the PEALD super-cycle process used to form 5 % Al-doped ZnO (AZO).

4.1.3.2 Step 2: Al_2O_3 Bottom dielectric layer

The 30 nm Al_2O_3 bottom dielectric layer is deposited by PEALD with a TMA precursor. The TMA is used with an inductively coupled remote O_2 plasma reactant at 300 W. The wafer is preheated to 150 $°C$. The chamber pressure is kept at 15 mTorr. The initial step is O_2 plasma clean for 15 s at 300 W. The mean deposition rate is 0.13 nm/cycle, measured by spectroscopic ellipsometry. For 40 nm film thickness Al_2O_3, 300 cycles are required. The flow of the recipe is shown in table 4.2. Keep the wafer in the chamber and deposit the next layer without breaking the vacuum. A good interface can be obtained.

TABLE 4.2: *The recipe of depositing Al_2O_3 used Flex AL machine*

Step No.	Chamber Input	Pulse Duration
1	TMA Burst	20 ms
2	TMA-purge	3s
3	O_2 pre-flow	4s
4	O_2 plasma 300 W RF	3s
5	O_2-purge	1s

4.1.3.3 Step 3: ZnO channel

Keep vacuum after step 2. The 40 nm ZnO channel layer is deposited by PEALD with a DEZ precursor continuously. The DEZ source is used with an inductively coupled remote plasma reactant O_2 at 300 W. The wafer is preheated to 190 $°C$. This is optimized by Oviroh et al. (2019); A.Borysiewicz (2019); Ghazali (2018). The

deposition temperature not only satisfies the HI requirement (low temperature $< 200°C$), but also has high mobility. The chamber pressure is kept at ten mTorr. The initial step is O_2 plasma clean for 15 s. The mean deposition rate is 0.12 nm/cycle, measured by spectroscopic ellipsometry. For 40 nm film thickness ZnO, 333 cycles are required. The flow of the recipe is shown in table 4.3. After ZnO is deposited, ZnO is patterned by photolithography using the standard recipe from Step 1. Subsequently, the channel layer is wet etched using a standard recipe from Step 1. The dielectric layer can be an etched stop layer because it is highly selective.

TABLE 4.3: *The recipe of depositing ZnO used Flex AL machine*

Step No.	Chamber Input	Pulse Duration
1	DEZ Burst	100 ms
2	DEZ-purge	4s
3	O_2 pre-flow	4s
4	O_2 plasma 300 W RF	2.65s
5	O_2-purge	4s

4.1.3.4 Step 4: AZO Source and Drain Contacts

This step is identical to Step 1 for the global bottom gate deposition. The update is due to the change in Al concentration from 5 % to 2 %. To deposit 40 nm 2 % AZO, 233 cycles are required, and six super cycles are included. It is patterned by PL using AZ2020 negative photoresist and lifted off in NMP at room temperature.
The spinning speed for AZ2020 is set to 2000 rpm for a mean thickness of 3 μm. After spinning resist, a soft oven of 110 $°C$ is required for 60 s. The resist was then exposed to an Hg vapor UV lamp with an I-Line (365 nm) filter for 20 s. Subsequently, the resist is baked after exposure at 110 $°C$ for 60 s. The resist is developed in AZ726 developer solution (2.38 % TMAH in H_2O with surfactants) for 35 s, cleaned by rinsing with DI water and dried with N_2 gun. This is the standard PL process for the lift-off process. A 2.5 % Al-doped ZnO (AZO) layer was selected as the source/drain electrode because it provides the lowest contact resistance while maintaining stable transistor operation Rowlinson et al. (2022a).

4.1.3.5 Step 5: Al_2O_3 Top dielectric Blanket

This step is identical to step 2 for the deposition of the dielectric blanket of the bottom gate.

4.1.3.6 Step 6: Vias Etch

TMAH is used to wet-etch Al_2O_3 above the bottom gate of AZO and the source and drain of AZO. Although even Al_2O_3 above the bottom gate and source/drain have different thicknesses, due to the highly selective difference between Al_2O_3 and AZO Sun et al. (2014), AZO can act as a stop layer. A 1:100 resolution of 25 % TMAH in water is the etching etchant, and the mean etch rate is 1.25 nm/s at room temperature. It is patterned through the standard S1813 recipe from Step 1.

4.1.3.7 Step 7: Al Contact Pads

100-nm Al contact pads are deposited by evaporation at a rate of 1 $Å/s$ as the final layer. The negative photoresist AZ2070 from MicroChemicals is used for patterning. The recipe of PL is identical to step 4 for Source and Drain Contacts. The detail is shown in table 4.4.

Table 4.4: Al evaporation recipe (example run).

Parameter	Value
Material	Al
Target thickness	100 nm
Soak 1	5 min
Soak 2	8 min
Initial deposition rate	0.1 Å/s
Stable deposition rate	1.0 Å/s
Stable power	8.2%
Estimated deposition time at stable rate	≈ 1000 s (≈ 16.7 min)
Estimated total time (soaks + deposition)	≈ 29.7 min

4.1.4 Fabrication: P-Type Silicon Global Bottom Gate (p-Si GB) ZnO TFT

Due to the sharp corner issue in the measurement (discussed in *Chapter 5*), to prevent the defect from fabrication and to establish a correlation model linking deposition conditions, interface quality, and device performance for deep understanding of Al_2O_3/ZnO interface, a P-Type Silicon Global Bottom Gate (p-Si GB) ZnO TFT is designed and fabricated. The fabrication process has six main steps: Step 1: global gate preparation, 150 mm P-type silicon as substrate while also as the global bottom gate. A classic surface clean process will be done in this step. Step 2: PE-ALD gate insulator, plasma enhanced atomic layer deposition (PE-ALD) is used to grow 30 nm Al_2O_3 as the gate dielectric. 4 different deposition temperatures are considered here to investigate the influence of deposition temperature of Al_2O_3 to Al_2O_3/ZnO interface. For the device with SiO_2 gate dielectric, this step would be thermal oxidation under 900 $\circ C$.

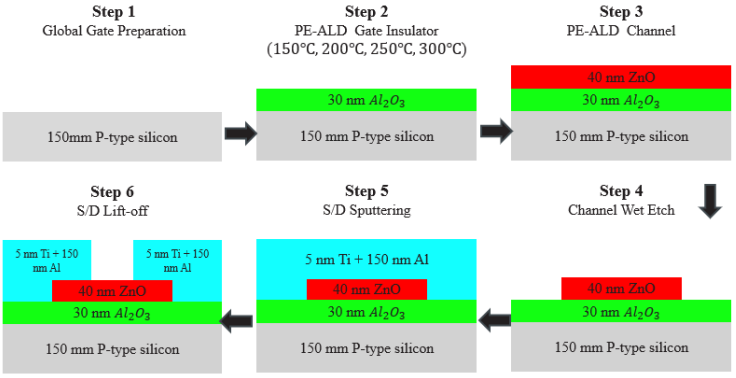

FIGURE 4.4: Fabrication process flow of the global bottom-gate ZnO thin-film transistor (TFT). Four different temperatures (150°C, 200°C, 250°C, and 300°C) were applied during the Al_2O_3 gate dielectric formation in Step 2. The ZnO channel layer is deposited immediately after the Al_2O_3 layer without breaking the vacuum.

Step 3: PE-ALD channel, 40 nm ZnO, as channel layer, is continuously deposited on the Al_2O_3 without break vacuum to ensure the interface quality. Step 4: channel wet etch, considered same recipe with the dual-gate device. Step 5: S/D RF sputtering, a 5 nm + 150 nm Al stacked layer is sputtered as the source/drain. 5 nm Ti improves adhesion and contact with ZnO, while also reducing the contact resistance. This step is full-sheet deposition process, followed by lift-off formation.

4.1.5 Post-Process steps

After the completion of all TFT fabrication processes, the wafer is scribed into $30mm \times 40mm$ chips. One wafer can be scribed into 15 chips. Before scribing the wafer, a 5 µm layer of S1813 positive resist is spun on (2000 rpm) the wafer to create a perfect surface. After scribing, the resist S1813 is stripped in NMP for 5 minutes at room temperature and rinsed with Acetone, then IPA, ready for measurement.

4.1.6 Scanning Electron Microscope (SEM)

The SEM image of the Global Bottom Gate device is shown in Fig. 4.5. The position of the global metal pads of the bottom gate is shown in Fig. 4.5 (left), and the channel area is zoomed in and shown in Fig. 4.5 (right). The channel is marked in a red rectangle, and the source and drain are marked in two yellow rectangles. The SEM image shows good alignment.

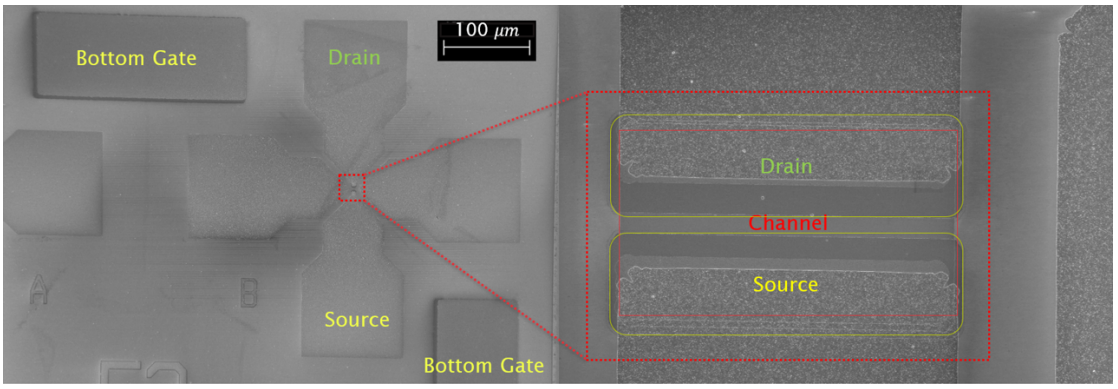

FIGURE 4.5: SEM image for (**Left**) global bottom gate device (**Right**) zoomed in channel part, that shows clear alignment.

4.2 Measurement Set Up

4.2.1 I-V Measurement Set Up

A 4 probe I-V measurement station is set to perform Current-Voltage measurements. Two KEITHLEY 2636B SYSTEM SourceMeters are used as power supply units to provide drain and gate bias voltages. The measurement station schematic is shown in Fig. 4.6. The black box prevents light because ZnO is a light-sensitive material. The

scribed chip is placed on the wafer holder and then on the vacuum pump to prevent the chip from moving. Once again, make sure the chip is fixed and does not move. The probes are then adjusted, and the metal pads are touched. This process should be performed slowly and gently to avoid surface damage to the chip.

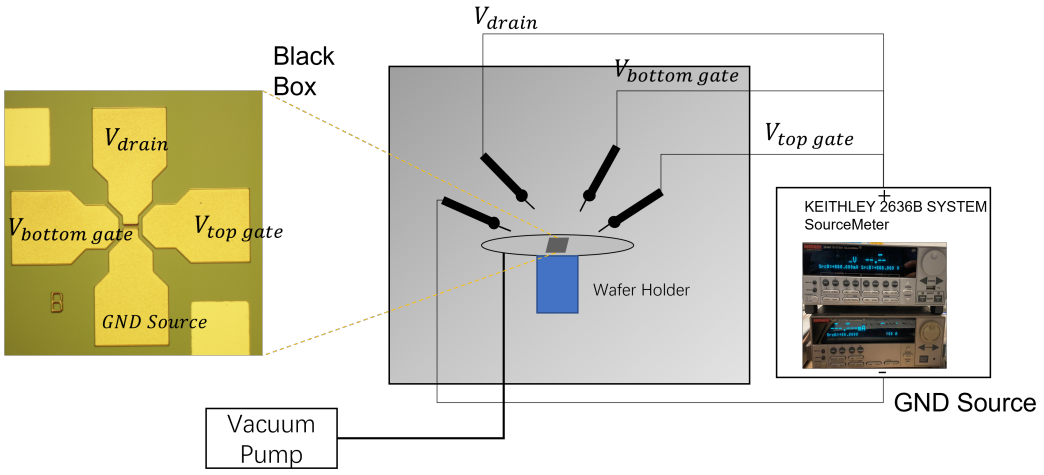

FIGURE 4.6: The schematic of I-V Measurement station.

4.2.2 C-V Measurement Set Up

A 2 probe C-V measurement station is set to perform the capacitance-voltage curve measurement. A C is used. This C-V analyser supports two measurement frequencies: 1 kHz and 1 MHz. In this measurement, two measurement modes are series mode and parallel mode. The measurement setup is quite similar to the I-V measurement station, as shown in Fig. 4.7.

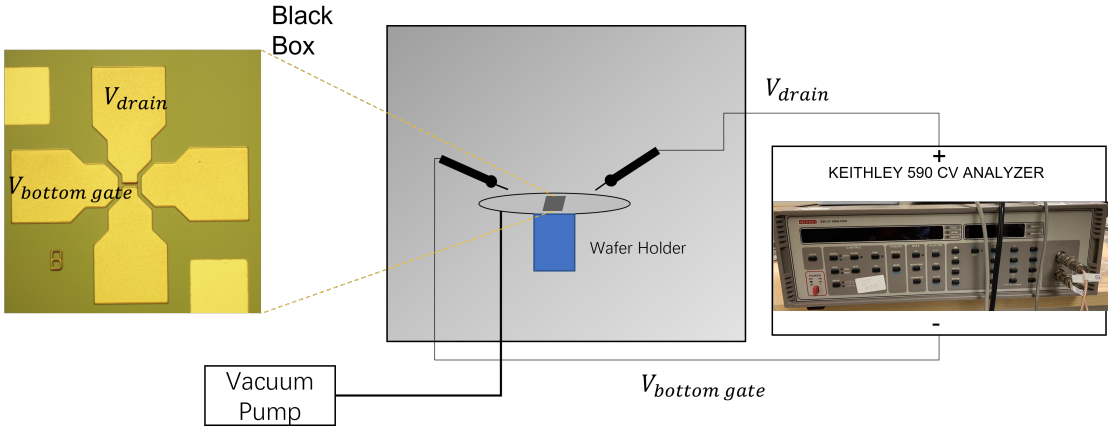

FIGURE 4.7: The schematic of C-V Measurement station.

The user manual does not explain the difference between the two measurement modes. However, from the other work Omar et al. (2015); Bae et al. (2023); Lee et al. (2011a), the difference between the two modes is how the capacitance in the oxide layer and parasitic resistance connection, as shown in Fig. 4.8, affects the way the C-V ANALYSER extracts the resistance from the measurement result. In this work, the series equivalent circuit model was adopted for extracting the oxide capacitance in the accumulation regime, where the influence of series resistance is significant. In contrast, the parallel model was employed for interface trap analysis using the conductance method, as it more accurately represents the loss mechanisms associated with interface states.

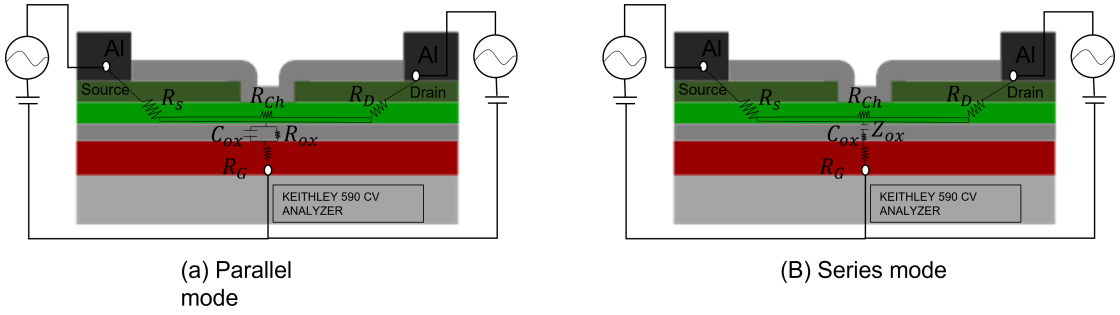

FIGURE 4.8: A difference schematic of C-V Measurement mode.

4.2.3 Optical Bias Stress Measurement Set Up

Optical PBS/NBS measurement station and the top view of the measurement setup. (a) The schematic of monochromatic illumination system, controlled by Keysight 1500. A whole optical bias stress measurement consists of 3 steps: initial measurement, double-direction I-V sweep, and bias stress. For the I-V sweep, the monochromatic illumination system is turned off and the device will be measured under a drain voltage of 1 V and gate voltage sweep from (-10 V to +10 V). Under the stress step, a gate bias voltage of $\pm$ 5 V or $\pm$ 10 V and a drain voltage of 1 V are applied for a stress time of 60 s. LED pulsed signal setup is : period 2500 μs, on time 5 μs and duty cycle is 0.2 % (400 Hz). A light spot with a diameter of about 300 μm is formed on the device surface by the optical fiber ($A_{spot} \approx 7.1 \times 10^{-4} cm^2$), which covers the whole channel area. Those setups are determined to maximize the excitation of the device. All experiments kept the same optical setup for relative comparison and the instantaneous power of the electric drive is about 0.2 W. The average electric power is

about 0.4 mW by considering the duty cycle of 0.2 % (this is the electric power, not the actual optical power).

4.2.4 Measurement Process Flow Chart

Once the chip is loaded correctly, the following process is to set the measurement mode and specify the voltage to drain and gate. All of those are handled by editing the script in MATLAB. Subsequently, the measurement was completed and data was collected in MATLAB. Finally, process the data and extract relative parameters from the measurement results. The flow chart of the data process is shown in Fig. 4.10, the measured I-V curve and the extracted parameters are discussed in *Chapter 5*.

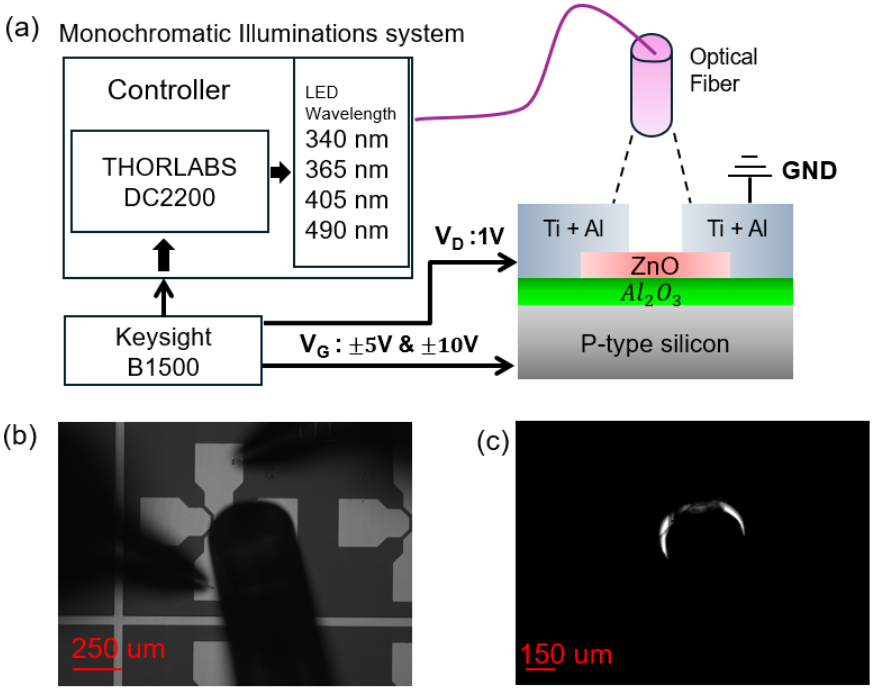

FIGURE 4.9: Optical PBS/NBS measurement system. Keysight 1500 is controlling the illumination system. Once the signal is received from Keysight 1500, THORALDS DC2200 sends the electric signal (1 V / 200 mA) to different wavelength LED emitters (340 nm, 365 nm, 405 nm, and 490 nm). Then light is applied to the device via the optical fiber. LED pulsed signal setup is : period 2500 μs, on time 5 μs, and duty cycle is 0.2 % (400 Hz). All measurements are operated under room temperature. All experiments kept the same optical setup for relative comparison. Device structure: P-type Si/Al_2O_3/ZnO, metal pads are Ti/Al. (b) Microscope image during measurement with scale bar of 250 μm. (c) Light spot image with scale bar of 150 μm shows all channel areas are covered.

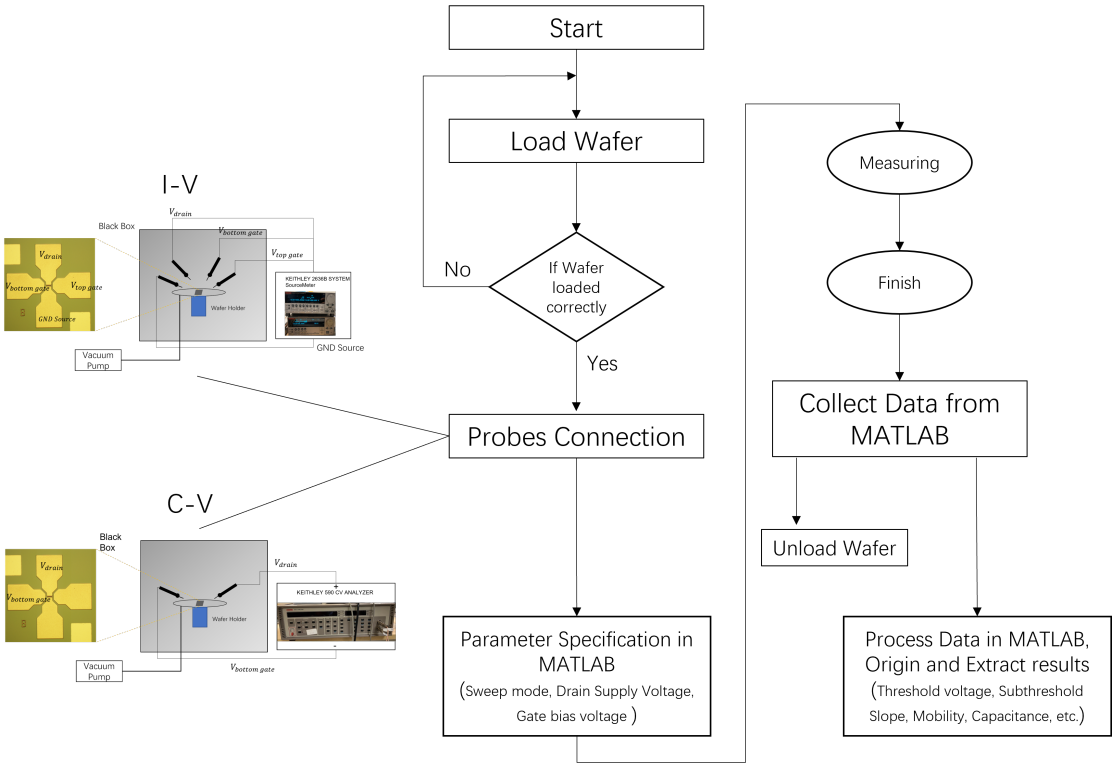

FIGURE 4.10: The schematic of Measurement process flow chart.

Chapter 5

Investigation of Gate Sharp Corner Effects

5.1 Introduction

The current–voltage (I–V) curve analysis can get the most fundamental property of thin-film transistors (TFTs). Systematic analysis of transfer ($I_D - V_G$) curves can be used to extract device parameters, e.g., the threshold voltage (V_{th}), field-effect mobility (μ_{eff}), subthreshold swing (SS), on/off current ratio (I_{on}/I_{off}). Such parameters determine whether the device is operating in enhancement or depletion mode and have a direct influence on gate controllability and switching speed, which has been discussed in *Chapter:3*. A clear knowledge of these baseline I–V properties is the critical point needed to interpret abnormal electrical behaviour under structural defects or high-field stress.

For sharp corners in the gate structure, pronounced electric field accumulation, which is detrimental to device reliability. Field enhancement of this magnitude can cause a threshold voltage shift, deterioration of gate control, and gate oxide dielectric breakdown Palumbo et al. (2020). To rationalize this phenomenon, the percolation model Palumbo et al. (2020); Raghavan et al. (2014b) has been widely adopted: under strong localized electric fields, certain regions within the insulating dielectric can temporarily behave as conductive paths, facilitating leakage and accelerating breakdown. In my earlier work with Dr.Ben on ZnO TFTs Rowlinson et al. (2022a),

we identified a gate leakage current as high as 2.7 μA and a loss of gate bias control at drain bias above 9 V as direct evidence of gate oxide breakdown.
Based on these results, we first perform a systematic I–V characterization of typical ZnO TFTs with AZO bottom gates, which helps to establish the baseline characteristics of their electrical performance. We next concentrate on the extraction of breakdown voltage-related electrical parameters such as gate current growth and threshold voltage shift and relate them to the threshold of gate dielectric failure. Finally, the experimental results are used in conjunction with electrostatic simulations of the fabricated gate structure to determine the contribution of sharp corner defects to field localization and breakdown initiation. By combining the transmission electron microscopy (TEM) evidence with the simulated field distributions, this work clearly proves the crucial role of geometrical defects in determining gate oxide reliability and presents design and process optimization methodologies to suppress structural disorder for enhancing the reliability of ZnO TFT-based 3D heterogeneous integrated circuits in the future Zeng et al. (2023).

5.2 Literature Review

Sharp corner effects at the gate electrode have been a long recognised reliability issue in advanced MOSFET structures, because of the local increasing of the electric field that increases the rate of charge injection, trap formation and dielectric breakdown Li et al. (2025); Sun et al. (2024a). The same has also been observed in oxide semiconductor thin-film transistors (TFTs). Indicatively, initial research on polysilicon TFTs found that deviant hump behaviours in the transfer curves were present due to localised trap occupancy and uneven field distribution at the oxide/semiconductor interface as the electric fields increased along gate and channel edges Qi et al. (2017); Zhang et al. (2025). These edge effects are directly associated with degradation of reliability in the form of leakage currents, threshold voltage drift and mobility degradation.
In the case of oxide-based TFTs, the problem is more pronounced since the low-temperature fabrication and wet-etch process can be associated with the creation of the gate-edge roughness or undercut corners, which are also proved by TEM cross-sectional observations. These sharp geometries enhance the concentration of the electric field at the ZnO/Al_2O_3 interface leading to two adverse effects. To begin with,

localized field stress enhances the initial breakdown of the dielectric insulation of the gates in the form of Al_2O_3 at high drain bias, boosting the leakage and lifetime depreciation. Second, the increased trapping and de-trapping between the corner regions exacerbates trapping and de-trapping threshold-voltage instabilities and abnormal capacitance behaviour recollections of the hump effects previously reported by other polysilicon TFT works Valletta et al. (2008). Such results emphasize the point that field crowding caused by sharp corners was initially demonstrated in MOSFETs, but it is also quite significant with oxide TFTs and needs to be optimized by providing careful gate patterning and edge engineering.

5.3 Sample Preparation

The ZnO thin-film transistors (TFTs) were prepared on a 100 nm SiO_2 isolation layer thermally grown on a 150 mm silicon substrate. The bottom-gate electrode was first deposited by thermal atomic layer deposition (ALD) at 175 $^{\circ}C$ to form a 40 nm layer of 5 % Al-doped ZnO (AZO). An HCl-based (35 % HCl : DI water = 1:1000, etching rate is about 1.1 nm/s) wet-etching procedure was then used to pattern the gate, wherein undercut and sharp-corner reliefs may occur at the edges of the electrode. A 30 nm Al_2O_3 gate dielectric and a 40 nm ZnO channel layer were then deposited contiguously by plasma-enhanced ALD (PEALD) without breaking vacuum between the two processes. This was a process that provided a clean interface between the dielectric and the channel Rowlinson et al. (2022a). Selective wet etching was used to define both layers to attain the desired device geometry.

After the channel was formed, PEALD are used to deposit a 30 nm layer of Al_2O_3 passivation at a deposition temperature of 150 $^{\circ}C$ to wrap the channel and prevent contamination by the ambient. Wet etching to allow S/D (source/drain) vias to pass through the passivation was then performed selectively Rowlinson et al. (2022a). The thermal ALD was used to deposit a 40 nm film of 2 % AZO, which was patterned to form the ohmic contact layer to the S/D regions, and which provides a low-resistance interface to the ZnO channel Rowlinson et al. (2024a). Lastly, the S/D metallization was completed by thermal evaporation of 100 nm aluminum electrodes and patterned using a lift-off process.

This fabrication sequence is shown schematically in Fig. 5.1, but it comprises a sequence of thermal ALD and PEALD steps combined with wet-etching patterning steps. The methodology allows us to establish a very clear bottom-gate ZnO TFT, and also identify possible reliability issues of wet-etch induced corner defects at the gate electrode. The process that causes this undercut is suspected as wafers are immersed in deionized (DI) water after the etching process. For the gate wet etch process, due to the fast etch rate ($\backsim$2.2 nm/s), the etch process is not stopped immediately. Therefore, the diluted etchant solution continues etching the gate and forms a sharp corner.

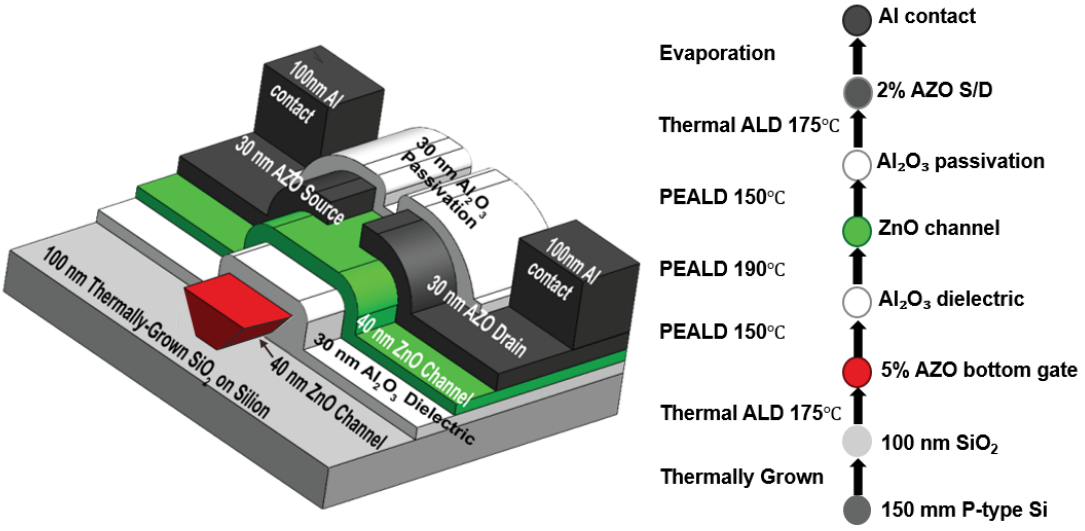

FIGURE 5.1: Schematic illustration of the fabrication process flow for the ZnO thin-film transistor (TFT). The device is fabricated on a 150 mm p-type Si wafer and a 100 nm thermally grown SiO_2 isolation layer. A bottom gate of 40 nm 5% Al-doped ZnO is deposited by thermal ALD at a temperature of 175 $^{\circ}C$ and patterned using HCl wet etching. A 30 nm Al_2O_3 gate dielectric, 40 nm ZnO channel are then deposited sequentially by PEALD without vacuum release then followed by wet-etch patterning. PEALD forms a 30 nm Al_2O_3 passivation layer at 150 $^{\circ}C$, and vias are opened selectively through wet etching. The source/drain contact layer is a 40 nm 2% AZO layer deposited using thermal ALD. Lastly, the S/D metallization is completed by using thermal evaporation and lift-off to form 100 nm Al electrodes. The corresponding layer-by-layer fabrication sequence is demonstrated in the right panel.

5.4 Experiment

In this work, we examine the effect of gate sharp corners on the electrical performance and reliability of bottom-gate ZnO thin-film transistors (TFTs). The experimental

measurement system and module are described in **Chapter 4**. By comparing the transfer and output characteristics at different drain biases, the effect of increasing lateral and vertical electric fields on the mechanism of electrostatic gate control is evaluated. Especially, it is emphasized that the gate leakage and dielectric breakdown are strongly induced in the localized high field region around the gate sharp corner. In order to get a quantitative understanding, the experimental results are compared to device simulations performed in SILVACO, where idealized structures without sharp-corner geometry are represented. By mapping the simulated breakdown field to the experimentally measured channel control degradation, threshold voltage shift and gate leakage current, the deleterious role of gate sharp corners on the reliability of Al_2O_3-based dielectric is explained. The result of this combined experimental-simulation approach is proof that corner-induced field crowding speeds the collapse of a device.

5.4.1 Transfer Characteristic of ZnO Thin Film Transistor

In our previous studies Rowlinson et al. (2022a), ZnO thin-film transistors (TFTs), shown in figure 5.2(a), were fabricated at a low deposition temperature of 190 $°C$, with channel widths ranging from 5 μm to 50 μm. The electrical characterization demonstrated that the device performance strongly depends on the channel width. In particular, the TFT with a 50 μm channel width (figure 5.2 (b)) exhibited superior performance, including a stable threshold voltage around -9 V during operation, a steep subthreshold swing (SS) of 120 mV/dec, a low off-state current of 10^{-13} A, an on/off current ratio exceeding 10^{10}, and a high saturation field-effect mobility of 5 cm^2/Vs. The previous work confirmed that scaling the channel geometry significantly influences the device switching characteristics, and wide-channel devices yield enhanced electrical stability and current-driving capability.
With the reduction of channel width, the threshold voltage (V_{th}) shows a positive change as demonstrated in figure 5.2 (a). This behaviour is due to the fact that carriers in the narrow channels are more susceptible to interface traps and edge-related defects that become important as the perimeter-to-area ratio is increased. The increased trapping of carriers by traps reduces the amount of free carriers available for conduction for a given gate bias. Hence, the trap-induced charge loss and the channel inversion need a higher gate voltage, thus leading to a higher (V_{th}) Hsueh et al. (1988);

Wang (1978); Majima et al. (2000). This narrow channel effect offers a plausible explanation for the large threshold voltage enhancement that is observed in the 5 μm device vs. that of wider channel devices.

Notably, a pronounced increase in V_{th} occurs when the channel width is reduced to 5 μm, whereas devices with channel widths of 10 μm and above exhibit relatively similar threshold voltages. This behavior suggests the presence of a critical channel width below which edge-related effects become dominant.

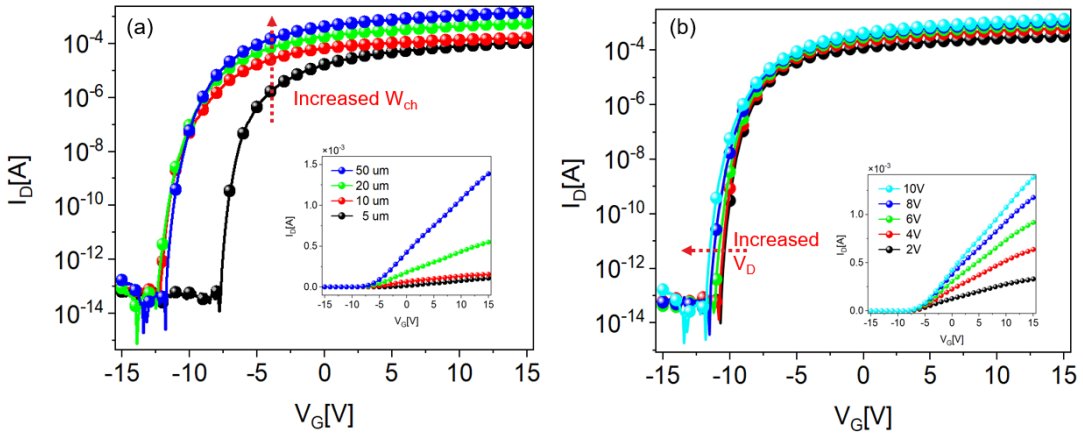

FIGURE 5.2: Logarithm plot transfer characteristic ($I_D - V_G$) of ZnO TFTs fabricated at 190 $^{\circ}C$. (a) Comparison of devices with difference channel widths (W_{ch} = 5,10,20, and 50 μm) measured at I_D = 15 V, showing improved current drive and stable threshold with increased channel width. (b)Logarithm plot transfer curves of the 50 μm channel width device measured at different drain voltages (V_D = 2 - 10 V, increment 2 V). The inset plot indicate corresponding linear plot transfer characteristic ($I_D - V_G$).

5.4.2 Gate Sharp Corner Issue

In the ZnO TFT having a channel width of 50 μm, we observed a threshold shift phenomenon when $I_D - V_G$ sweep is performed under high drain bias. Once V_{DS} was about 9.3 V, (see Figure 5.3, green curves), the device showed an abnormal threshold voltage fluctuation. Furthermore, for the after measurements at the higher drain voltage, such as VDS=9.4 V, the device always exhibited a significant positive threshold voltage shift with a decrease in the on-state current. This indicates that a single high electric field stress in the drain-side channel region induced an irreversible degradation process and made the device harder to turn on. A number of mechanisms may explain this phenomenon. From the physical point of view, when V_{DS} becomes

large (larger than 9 V) a strong lateral electric field and local pinch-off are produced near the drain end of the channel. Electrons can then have enough energy to be injected vertically into the gate dielectric/interface and trapped Andreev et al. (2021); Tsai et al. (2014). In n-type devices, trapping of electrons results in net negative charges, and a higher positive gate bias is needed to produce the same channel carrier density, resulting in a positive V_{th} shift.

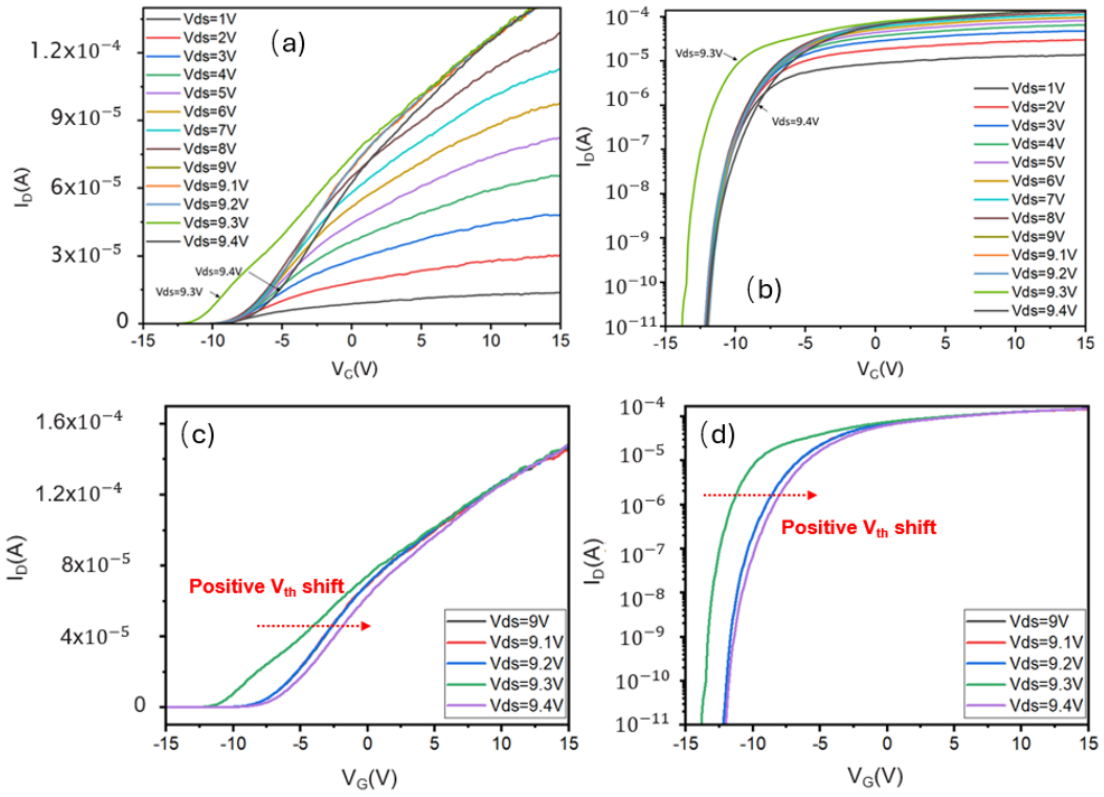

FIGURE 5.3: Transfer curves of the channel of 50 μm ZnO TFT at various drain biases. (a) Linear-scale $I_D - V_G$ curves and (b) semi-logarithmic plot for the emergence of an anomalous fluctuation at $V_{DS} = 9.3$ V. (c,d) Focused plot shows transfer curve that around drain voltage of 9.3 V. It is observed a decrease in the on-state current and an increase in the threshold voltage, which can be attributed to the irreversible device degradation caused by stress at high fields near the drain region.

More electrical measurements showed that once the abnormal transition point occurred, the gate gradually lost its efficient way of controlling the channel and the transistor eventually lost its switching characteristics. As shown in figure 5.4. (a), the transfer curves under high drain bias cannot be clearly identified as on/off behaviour, which indicates severe degradation of gate control. In addition, the device shows an increase of gate leakage current under high electric fields applied, as shown in figure

5.4. (b), which strongly indicates the occurrence of soft breakdown. This can be explained by the appearance of local percolation paths in the gate dielectric or at the interface and the formation of conducting transport channels. Because the gate leakage current is increasing gradually with higher applied external electric field. This meets the conditions for the formation of a percolation path. Once such percolation paths are formed, the leakage path is self-sustaining and irreversible, which means the leakage current will increase whenever a high electric field is applied, and this defect is leading to the collapse of transistor performance. These results show the importance of dielectric integrity and interface quality for transistor reliability, particularly for working at high electric field stress conditions.

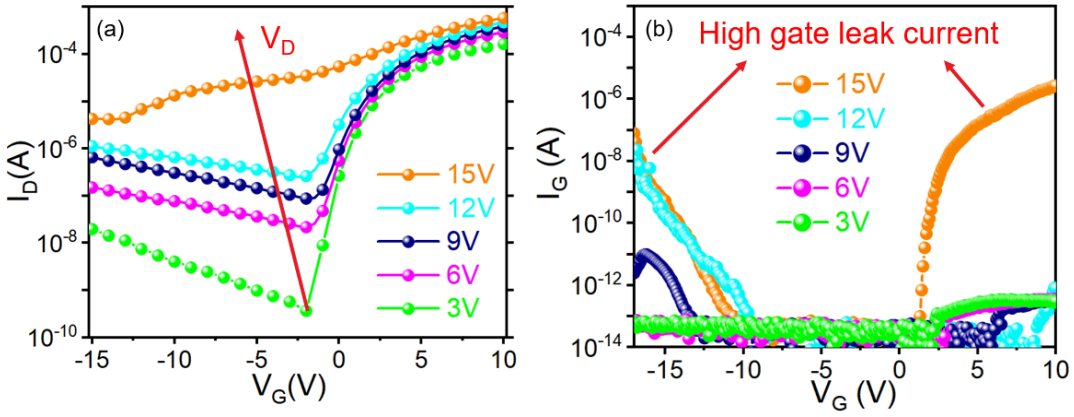

FIGURE 5.4: (a) Transfer characteristics of the ZnO TFT under varying drain bias indicating gradual loss of gate control and vanishing of switching behaviour at high V_D of 15 V. (b) Gate leakage current, which shows a sharp rise under intense electric field indicating the onset of soft breakdown, which is presumably due to formation of percolation paths in the gate dielectric.

In the cross-sectional TEM images of the ZnO TFT structure, a distinct sharp corner feature can be observed near the gate edge. Careful process analysis suggests that this defect originates from the wet etching of the 45 nm AZO electrode. Under the applied HCl:DI (1:1000) etchant, the measured etching rate for AZO is approximately 2.2–2.5 nm/s. Ideally, this process should produce a smooth and uniform sidewall profile. However, due to the inherently isotropic nature of wet etching, material removal occurs simultaneously in both vertical and lateral directions. In addition, the etching rate near the AZO/SiO_2 interface can be affected by local variations in grain structure, dopant distribution, and stress concentration, which results in uneven sidewall

recession. Consequently, instead of a vertical sidewall, the etching leaves behind a recessed geometry with a pronounced sharp corner.

The presence of such sharp corners is highly undesirable for device operation and long-term reliability. First, the corner geometry induces local electric field crowding, which can enhance carrier injection into the gate dielectric and accelerate dielectric breakdown. Second, the non-ideal interface formed around the sharp corner may introduce additional interface states and trap sites, thereby degrading channel conduction. These effects collectively manifest as positive threshold voltage shifts, mobility degradation, and increased device-to-device variability. Therefore, the observed sharp corner is not only a structural imperfection caused by the wet etching process but also a critical reliability concern that must be addressed in the optimization of ZnO TFT fabrication.

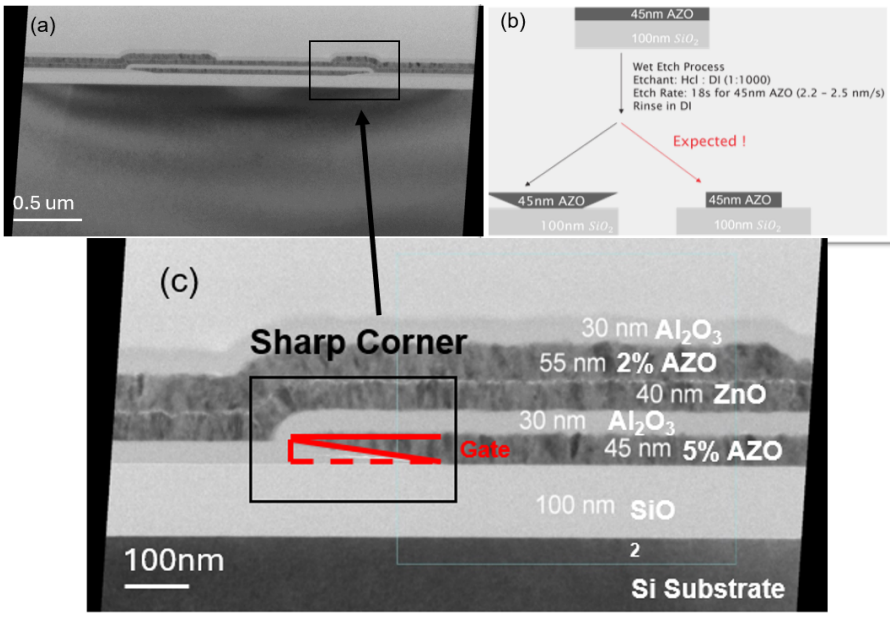

FIGURE 5.5: TEM Cross-sectional images of ZnO TFT structure. (a) Schematic diagram of the multilayer stack comprised of the entire device. (b) Schematic illustration of the wet etch profile of the AZO layer with 45 nm thickness. (c) Enlarged view of the gate region with non-ideal etch forming a gate sharp corner that can affect the distribution of electric fields and device reliability.

In oxide thin-film transistors, percolation breakdown is defined as the phenomenon where a large fraction of randomly distributed imperfections or traps in the gate dielectric are filled or activated upon a sufficiently high electric field (usually 5-10 MV/cm) Stathis (1999); Lee et al. (2011b); Krausmann et al. (2018). Once these localized states are linked, a conducting pathway is established and the local dielectric

becomes a local conductor. The manifestations are usually a rapidly increasing leakage current and loss of gate control. Although the mechanism mostly occurs in high V_D, positive V_G, it can also be activated under the large negative gate bias. In this case, the direction of the electric field is reversed, but the strong crowding of the local electric field still appears, especially at sharp corners of the gate electrode. Moreover, oxygen vacancies and impurity-related traps at the Al_2O_3/ZnO interface and/or in the bulk dielectric may also contribute to trap-limited conduction or Poole-Frenkel emission that facilitates the activation of the connection of even more traps into a percolation chain Ko et al. (2025); Lee et al. (2011b); Fregolent et al. (2023); Raghavan et al. (2014a). Experimentally, when $V_G = 15$ V, the gate current reaches 10^{-6} A, signalling the onset of a soft-breakdown state conduction path. However, the leakage behavior under negative bias does not fully mirror that under positive bias. While a significant increase in gate current is observed at +15 V, similar enhancement is not evident at −9 V or −12 V. This suggests that although local electric-field crowding may exist under both polarities, the carrier injection efficiency into the dielectric is strongly polarity-dependent. Under positive gate bias, electron accumulation at the ZnO/Al_2O_3 interface facilitates electron injection into the dielectric, promoting trap filling and percolation path formation. In contrast, under moderate negative bias, electron depletion in the channel suppresses injection, delaying the onset of percolation-related leakage. Only when the negative gate bias is sufficiently large (e.g., −15 V) does the injected carrier density become high enough to activate similar breakdown behavior. Figure 5.6 shows the mechanism of percolation failure of the ZnO/Al_2O_3 gate dielectric stack. Under high electric field stress, localized field crowding can activate defect sites in the dielectric, accelerating charge trapping and the formation of percolation paths. These localized defect sites fill or activate as the bias is increased. As the number of trapped charges increases enough to create a continuous conduction path from the gate electrode to the ZnO channel, it is indicated by the red dashed region in the figure. The dielectric becomes a locally conductive area along this percolation path, causing a drastic increase in the gate leakage current and the ultimate loss of electrostatic gate control. Further, the schematic highlights the stochastic nature of defect generation and the field-enhanced localization at the gate-drain overlap region where breakdown is most likely to grow.

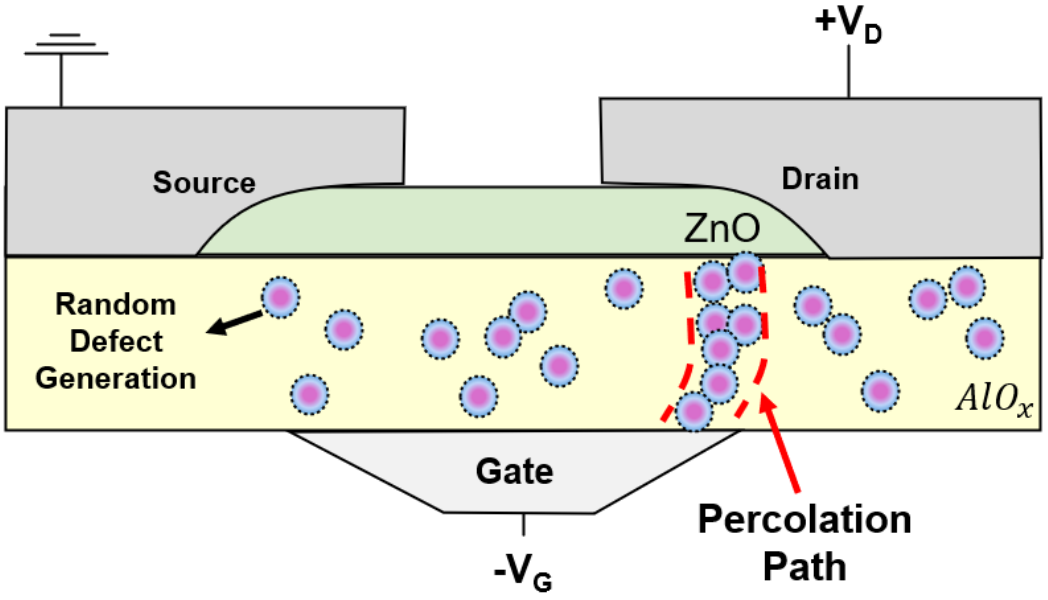

FIGURE 5.6: Schematic diagram of the percolation breakdown mechanism in ZnO/Al_2O_3 gate stack. With the applied high electric field stress, randomly generated defects in the dielectric are accumulated and form a continuous conduction path (red dashed line) from the gate to the channel, leading to increased gate leakage and loss of gate control.

Given these experimental observations and the identified role of gate-corner-induced electric field crowding in aiding percolation breakdown, we then used SILVACO simulations to quantitatively examine the electric field distribution and validate the impact of the sharp-corner geometry on device reliability.

5.5 Simulation

In order to quantitatively investigate the impact of gate-corner geometry on the electric field distribution, two-dimensional device simulations have been performed here using SILVACO TCAD. Cross-sectional view of the simulated ZnO TFTs is displayed in Figure 5.7. The model consists of a 100 nm thermally grown SiO_2 buffer layer on Si substrate, a 40 nm 5 % AZO bottom gate, a 30 nm Al_2O_3 dielectric, and a 40 nm ZnO channel layer, followed with 100 nm Al source/drain electrodes. Two different architectures were considered: (i) Figure 5.7 left, a device with an undercut sharp corner at the AZO gate edge, corresponding to the experimentally observed profile due to wet etching, and (ii) Figure 5.7 right, an idealized device without

undercut, having a smooth vertical sidewall. Such a comparative investigation allows for a direct assessment of the impact of the sharp-corner defect on the local electric field enhancement and its role in the onset of the dielectric breakdown and threshold voltage instability.

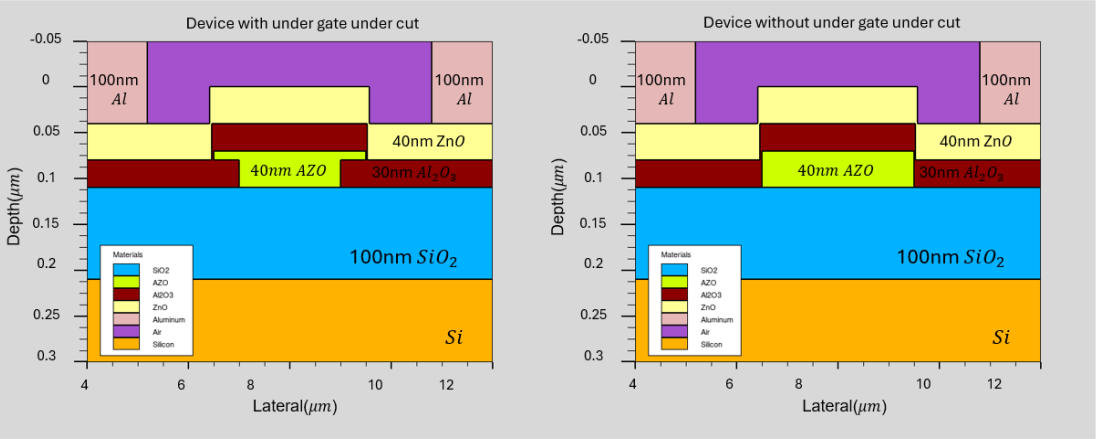

FIGURE 5.7: SILVACO TCAD models of ZnO TFTs with (left) and without (right) an undercut sharp corner at the AZO gate edge, used to evaluate electric field crowding and its impact on dielectric breakdown. All material thickness are set according to actual thickness.

Figure 5.8 shows a comparison of the transfer curves of ZnO TFTs with a normal gate and an undercut gate at V_{DS}=1 to 5 V. The V_{TH} shift and the Id of the undercut gate device are negative and smaller than those of the normal gate. From the current equation, 3.3 in the linear region, and 3.7 in saturation, the lower I_D is due to several factors: Due to the undercut gate edge, the electric field distribution is altered, causing the field to crowd, and increasing the carrier injection into the traps. This trapping effect decreases the free carrier density and effective mobility μ_{eff}, thus decreasing I_D. At the same time, trapping of electrons near the undercut region causes the threshold voltage to shift over toward the negative direction since fewer carriers are needed to turn on the channel. The high field conditions can also create percolation paths in the Al_2O_3 dielectric, which will cause a portion of the gate bias to be conducted in leakage current, further undermining gate control. The combined effects account for the observed negative V_{TH} shift and decreased on-state current of the undercut gate device.

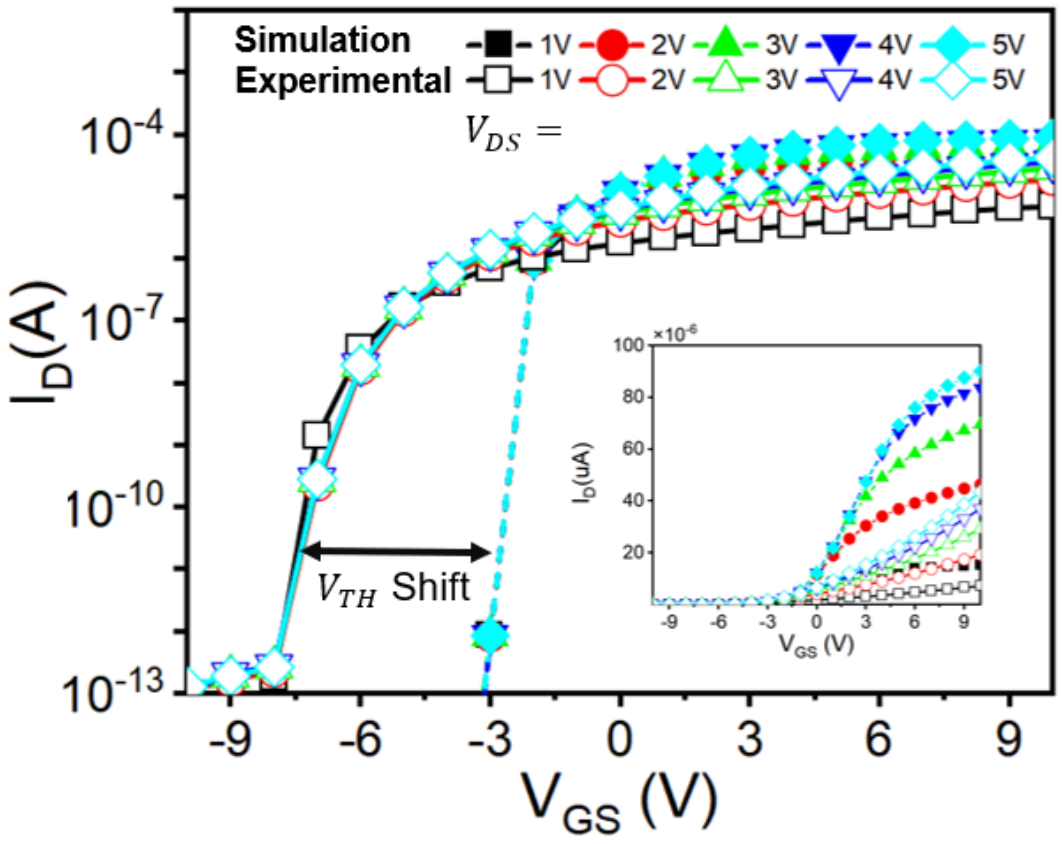

FIGURE 5.8: Simulated transfer characteristics of ZnO TFTs with a normal gate and an undercut gate at V_{DS}=1 to 5 V. The undercut gate device exhibits decreased Id and a negative V_{TH} shift relative to the normal gate, which can be explained by field crowding, enhanced trapping, and leakage due to percolation that degrade gate control and suppress channel conduction, respectively.

Figure 5.9 shows the simulated electron concentration profile for the ZnO TFT having an undercut gate corner. The colour map shows the carrier density, from low density (purple) to high density (red). It is found that electrons accumulate clearly at the corner of the recessed gate, where the local electric field is strongly enhanced due to geometrical field crowding De Michielis et al. (2011). Not only is this local carrier crowding effect expected to alter the channel conduction, but also to further enhance electron injection to the dielectric as a means of enhancing the rate of charge trapping and percolation path nucleation. The inset shows the structural location of the undercut corner in the device cross-section and verifies that this non-ideal geometry is the source of the observed high-field concentration and reliability degradation.

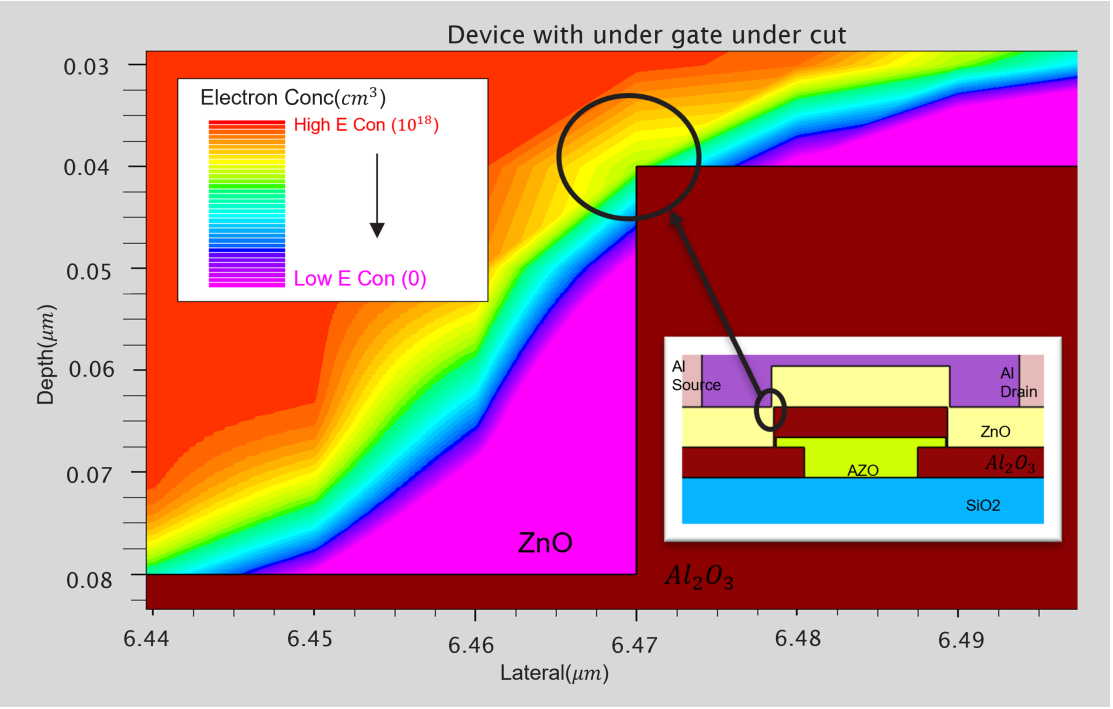

FIGURE 5.9: Simulated electron concentration in a ZnO TFT with an undercut gate corner. The colour map shows the carrier density, from low density (purple) to high density (red). Strong carrier accumulation appears at the recessed corner due to local electric field crowding, which enhances trapping and increases the risk of dielectric breakdown.

The electron accumulation will indicate a high electric field. Figure 5.10 illustrates the simulated electrical field distribution of ZnO TFTs with (left) vs. without (right) an undercut gate geometry defect. The field maps are normalised to highlight the relative distribution. A marked field crowding effect is found in the devices with the undercut gate: at corners of the buried gate area, the local field intensity is much higher than in the normal gate structure. This result shows that the undercut geometry acts to increase the electrostatic localization and produces a point for carrier injection. According to the previously reported results, the traditional Al_2O_3 starts to accumulate defects after the electric field has exceeded $\backsim$ 8.7 MV/cm Sharma et al. (2019). The measured increase in the field intensity at the undercut corner therefore supports a physical understanding of the experimentally observed device degradation since flaws and percolation path formation are more probable to be initiated from this high-field region.

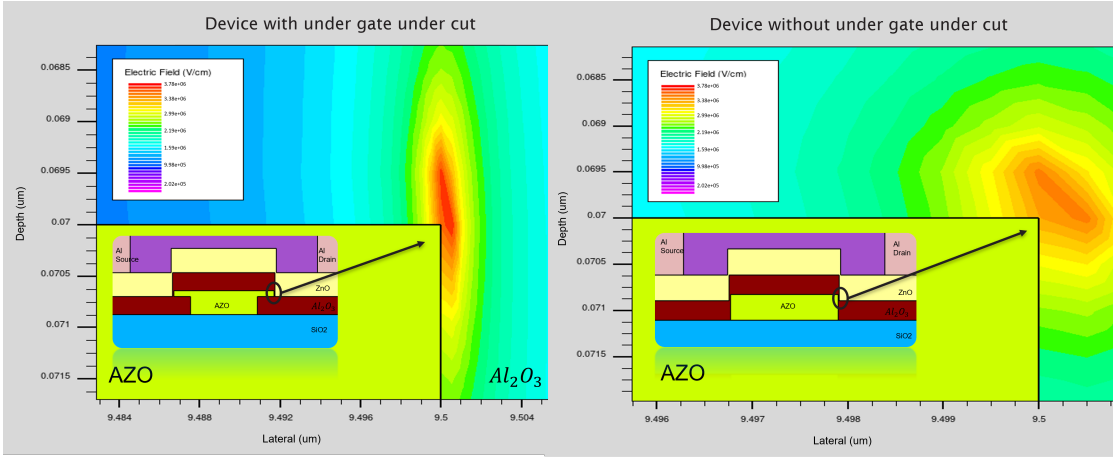

FIGURE 5.10: Simulated electric field distribution of ZnO TFTs with (left) and without (right) an undercut gate defect. The undercut geometry induces strong field crowding at the corner, where the local field approaches the defect-formation threshold of Al_2O_3 $\backsim$ 3.78 MV/cm under drain voltage of 5 V).

Figure 5.11 shows the simulated electric field distribution of the ZnO TFT with a gate undercut structure as the gate–drain potential difference (V_{gd}) increases from 2 V to 24 V. In this analysis, V_{gd} is used as the control parameter because the electric field crowding responsible for breakdown is primarily localized at the gate–drain overlap region. Although the channel formation is governed by V_{gs}, the local dielectric stress near the drain edge is determined by the potential difference between the gate and drain electrodes. Therefore, V_{gd} provides a more physically relevant metric for evaluating drain-side field enhancement and reliability concerns. At a low bias V_{gd}=2 V, the electric field is uniformly distributed with a slight enhancement localized around the corner of the AZO gate in the region of the gate. This means that under normal operating conditions the dielectric is still capable of holding the field applied without any significant tunneling. When V_{gd} is raised to 10 V, however, the simulation shows a clear growth in size of the high-field region extending into the Al_2O_3 dielectric. A partial conducting length is reached, which corresponds to the initial stage of localized electric field crowding and defect activation. This partial path is an indication that carriers may begin to interact with already present traps or structural defects at the interface, which represents the beginning of a potential reliability issue. As V_{gd} is increased to 24 V, the field distribution changes significantly. A conductive high-field path with a magnitude of more than 5 MV/cm is obtained throughout the dielectric, directly connecting the ZnO channel and AZO gate electrode. Importantly,

this critical bias is simulated to occur close to the experimentally observed threshold of soft breakdown in the device. Based on the high correlation between simulation and experiment, it is directly shown that the abnormal electrical behaviour in the form of the threshold voltage shift, leakage current increase, and ultimate loss of gate control is triggered by the localized field concentration at the undercut gate corner.

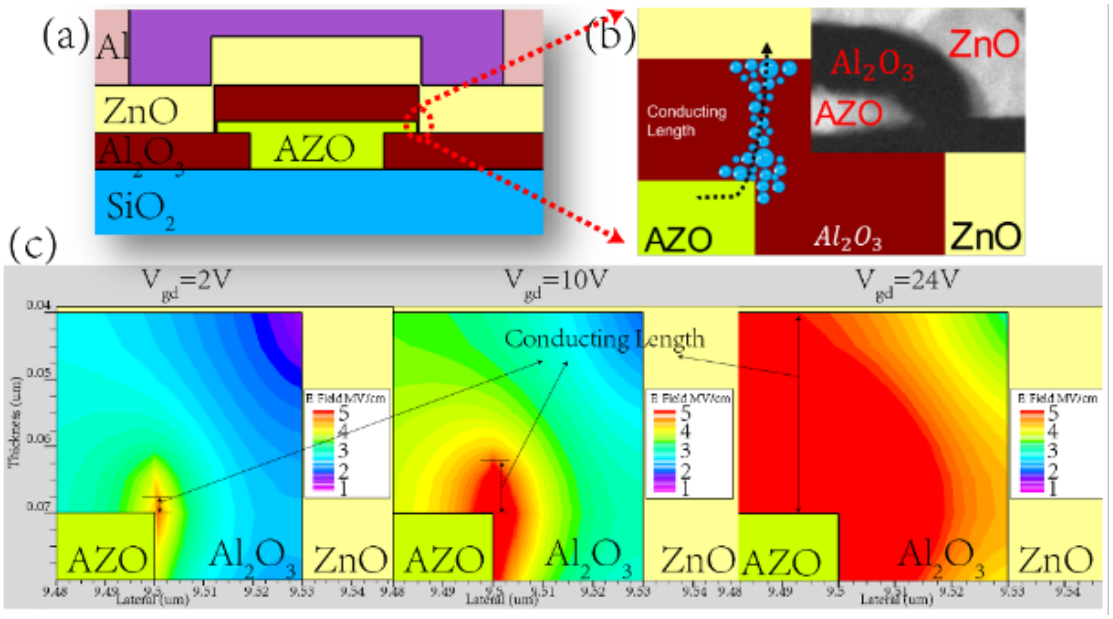

FIGURE 5.11: The simulation model with a gate sharp corner. (b) Schematic diagram of the conducting path across the Al_2O_3 layer (inset: TEM of the AZO gate) (c) The simulation result on electric field distribution in the dielectric layer showing a conducting length grow with a higher applied voltage.

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These results clearly show that the gate presence not only modifies the device electrostatics, but also generates a geometrical hot spot, in which the electric field can approach the defect-formation threshold reported for Al_2O_3 (approximately 8−9 MV/cm in literature Sharma et al. (2019)). It should be noted that the reported breakdown field depends strongly on the structural phase and defect density of the dielectric. While crystalline Al_2O_3 can sustain higher electric fields, amorphous ALD-grown Al_2O_3, as used in this work, typically exhibits a slightly lower breakdown strength due to its higher density of structural imperfections. Once the local electric field approaches this critical range, defect states may grow and interconnect to form percolation paths, leading to irreversible soft failure. Therefore, the simulation supports the experimental results and highlights that in undercut geometries the

effective dielectric robustness of the deposited Al_2O_3 film becomes the limiting factor for high-field operation.
At the same time, since the defect-formation threshold is fundamentally governed by the intrinsic material quality, increasing the structural and chemical perfection of Al_2O_3 (by optimizing the deposition conditions) is another feasible strategy to increase device robustness under high electric field stress.

5.6 Conclusion

In this chapter, we systematically examined the electrical behaviour of ZnO thin-film transistors, in particular the effect of gate sharp-corner defects that were introduced during AZO electrode wet etching. From transfer and output I-V measurements, we found unexpected threshold voltage shifts, gate-leakage current enhancement, and ultimate loss of gate control under high drain bias, which are direct effects of dielectric failure. The experimental results indicated that an abrupt transition point at VDS $\backsim$ 9.3 V was related to the onset of irreversible degradation which coincided with the formation of soft failure mechanisms. The percolation model gave a physical description of this effect: as the local electric field increases beyond the threshold for defect formation of Al_2O_3, randomly generated traps gather and form conductive percolation paths, which destroy the insulating nature of the gate dielectric.
In order to confirm this mechanism, SILVACO TCAD simulations have been performed by comparing ideal and undercut gate geometries. It was confirmed that the sharp corners lead to severe field crowding with localized enhancement of electron accumulation and dielectric field stress. With the increasing simulated gate-drain potential (Vgd) a high-field domain was gradually enlarged through the Al_2O_3 layer, and at $Vgd = 24$ V, a continuous conducting path was found – in good agreement with the experimentally observed soft breakdown voltage. These results show that geometrical imperfections (e.g., undercuts) strongly speed up the device degradation and indicate two key directions for reliability enhancement: (i) structure optimization to avoid field crowding at the corners and (ii) material optimization to improve intrinsic defect tolerance of Al_2O_3.
Having gained this insight, the next chapter turns away from structural geometry and towards the intrinsic material properties of Al_2O_3. Through a systematic study of the

impact of deposition temperature on the Al_2O_3/ZnO interface and dielectric integrity, we seek to understand the relationship between processing conditions, defect density, breakdown threshold and ultimately long-term reliability of ZnO TFTs.

Chapter 6

Investigation of the Deposition Temperature of Al_2O_3

6.1 Introduction

Aluminium Oxide (Al_2O_3) is one of the most actively researched high-k dielectric materials and is used in thin film transistors (TFTs) and metal-oxide semiconductor field-effect transistors (MOSFETs). It has excellent material characteristics including wide bandgap, excellent thermal stability and interface characteristics. Those advantages make it an interesting material to be adapted in the next-generation gate insulators. In addition, the Al_2O_3 dielectric constant is moderate compared to the traditional SiO_2 and provides superior controllability of the gate without extra parasitic capacitance. These are of particular concern when dealing with oxide semiconductors in which the quality of the gate dielectric is a major determinant of the stability of threshold voltage, field-effect mobility, and reliability of the device.
In addition to these features, Al_2O_3 possesses some important technological advantages with respect to thermal sensitive systems, such as flexible electronics, transparent equipment, and low-temperature oxide semiconductors. One of the key enabling factors is its compatibility with plasma-enhanced ALD (PEALD) processes, enabling high quality Al_2O_3 to be deposited at lower temperatures below 200 $^{\circ}C$, a temperature scale which can be applied to polymeric or glass substrates in flexible electronics. However, the deposition temperature nonetheless remains a process determinant that

clearly defines the microstructure, density, defect density, and surface morphology of Al_2O_3 films.

Many experiments have been carried out in a systematic way in order to know the material quality of the Al_2O_3 thin films deposited over non-reactive substrates of different temperatures Kim et al. (2022); Botzakaki et al. (2018); Groner et al. (2004). Experiments on such works have shown that low temperature deposition typically provides high density defect films, and higher temperatures can provide high stoichiometry at the expense of crystallisation or structural instability. Even though these results are helpful, in cases where dielectric films are investigated alone, it still does not guarantee that those results can be adapted from material to device level. The long term goal of introducing Al_2O_3 as a gate dielectric is to enhance the overall performance of TFTs and MOSFETs, and it follows that the deposition conditions must be taken into account both with regard to their impact on the dielectric itself, and with regard to the interface with the semiconductor channel.

To address this issue, some of the techniques rely on annealing the deposited interface to improve the quality of the interface and remove the trap states. However, high temperature thermal treatments are not typically compatible with thermally sensitive or flexible device platforms. The effect of deposition temperature, in isolation, on the electrical properties of Al_2O_3 based devices, requires a more detailed discussion due to this technological shortcoming. In particular, at a viable process window of 150-300 $^{\circ}C$, defect suppression, interface quality, and dielectric integrity have become critical issues to take into account in the design of high-performance low-temperature oxide electronic devices.

This work aims at addressing this gap in knowledge by answering the explicit question of establishing thin-film transistors. To achieve this motivation, no surface passivation process was involved during the device structure design to expose the ZnO channel and conduct subsequent optical PBS/NBS tests to quantify the Al_2O_3/ZnO interface quality. In this chapter, the effect of the deposition temperature on the dielectric quality, interface conditions, and stability of the device is discussed in detail through a combination of electrical characterization with I-V and C-V analysis and structural and chemical analyses with XPS and AFM. Lastly, the findings do provide guidance regarding process optimization in the manufacturing of next-generation low-temperature oxide electronics.

To answer these questions, this chapter is divided into a few sections. First, the fabrication process and experimental design are outlined, which shows how the temperature of deposition was varied systematically with other process parameters held constant. SEM and AFM structural and surface analyses are then described to assess morphology and uniformity, and XPS to assess chemical bonding and stoichiometry. C-V measurements are used to examine the quality of the dielectric, and then transistor-level performance is examined using I-V transfer and output characteristics, and extracted device parameters such as V_{TH}, mobility, SS, and gate leakage. With these complementary methods, this chapter provides a direct relationship between deposition temperature, dielectric/interface quality, and device performance and forms a solid base on the further optical PBS/NBS stress experiments in the following chapter.

6.2 Literature Review

Aluminium oxide (Al_2O_3) has found extensive use as a high-k gate dielectric due to its relatively high dielectric constant ($\backsim$ 9), broad bandgap ($\backsim$ 8.7 eV), high thermal stability, and compatibility with atomic layer deposition (ALD) and plasma-enhanced ALD (PEALD). Al_2O_3 is also of interest in oxide semiconductor thin-film transistors (TFTs) in that it can be deposited at relatively low temperatures, allowing it to be used in flexible and transparent electronics. Nonetheless, many experiments have demonstrated that the electrical and interfacial characteristics of Al_2O_3 films are highly sensitive to deposition temperature Kim et al. (2006); Kang et al. (1990); Hom-on et al. (2016); Ylivaara et al. (2014); Batra et al. (2015); 202 (2024). The temperature of deposition determines the chemical composition, defect density, interfacial reactions, and morphology of the films, which influence in turn the gate control, threshold-voltage stability, and dielectric breakdown.

6.2.1 PEALD Chemistry and Reaction Mechanism

O_2 plasma precursors are generally used with trimethylaluminum (TMA, $Al(CH_3)_3$) in PEALD. The growth occurs in two half-reactions that are self-limiting, as shown in

process 6.1 and process 6.2 Langereis et al. (2008):

$$\mathrm{AlOH}^* + \mathrm{Al}\left(\mathrm{CH_3}\right)_3(g) \rightarrow \mathrm{AlOAl}\left(\mathrm{CH_3}\right)_2^* + \mathrm{CH_4}(g) \tag{6.1}$$

$$\mathrm{AlCH_3^*} + 4\mathrm{O}(g) \rightarrow \mathrm{AlOH}^* + \mathrm{CO_2}(g) + \mathrm{H_2O}(g) \tag{6.2}$$

in which O_2 plasma is typically employed as an oxidant to substitute ligand-exchange reactions, offers greater process flexibility Profijt et al. (2011a). In particular, the ability to deposit high quality thin films at lower temperatures and avoid hard to purge H_2O oxidant. Also, the O_2 plasma is deemed a useful oxidant owing largely to the characteristic of stripping organic ligands (by O-radical driven combustion-like reactions at the surface) and is well established to strip carbon impurities off the substrate surface. According to the report from Y.Ren Ren et al. (2023), PEALD-deposited Al_2O_3/polycarbonate (PC) films are characterized by a slow densification behaviour with a temperature range of (80 - 160$^\circ C$), although the change in surface roughness finally defines the performance of the films. At deposition temperatures lower than the glass transition temperature (T_g) of the PC substrate (T_g $\geq$ 140 $^\circ C$) the film surface is smooth and free of cracks and the interfacial stress is low, hence exhibiting excellent gas-barrier properties. But as deposition temperature approaches T_g of 160 $^\circ C$, surface roughness increases drastically and cracks develop due to thermal expansion and shrinkage of the substrate which subsequently reduces the barrier performance.

6.2.2 C-V hysteresis and physical significance

A direct consequence of charge trapping and de-trapping in the dielectric and at the dielectric/semiconductor interface is called capacitance voltage (C-V) hysteresis Polyakov et al. (2007); Kalon et al. (2011). The high value of the hysteresis window implies that there are many active trap states, which trap and release carriers on forward and reverse voltage sweeps, and the low value of the hysteresis window implies that there are fewer traps, and the interfacial conditions are more stable. A change in the flat-band or threshold voltage in C-V hysteresis loops can be quantitatively associated with the net trapped charge density via $\Delta V = Q_trap/C_{ox}$ with ΔV being

the hysteresis width and C_{ox} being the oxide capacitance per area Kalon et al. (2011). As such, C-V hysteresis is a sensitive evidence of interface quality and dielectric reliability, larger hysteresis corresponds to higher trap density and more pronounced charge-storage effects, smaller hysteresis corresponds to larger electrostatic stability of the device.

6.2.3 X-ray Photoelectron Spectroscopy (XPS) and Atomic Force Microscopy (AFM)

X-ray photoelectron spectroscopy (XPS) provides us with information regarding the chemical composition of the Al_2O_3 films as well as the bonding environmentGreczynski et al. (2023). The relative intensities and position of the Al 2p and O 1s peaks can not only identify the stoichiometric $Al-O$ bonding but also defect-related species such as hydroxyl groups ($-OH$), carbon impurities or oxygen vacancies, which are tightly coupled with charge trap centres. Surface roughness can also be quantitatively determined with atomic force microscopy (AFM), giving quantitative values of root mean square (RMS) roughness, a critical parameter to determine uniformity and compatibility with deposition of semiconductor channelsXu et al. (2015). The rough and smooth surfaces generally suggest good quality dielectrics, and roughness or non-uniformity of the surface can contribute to interface scattering, mobility loss, and may cause unstable device operation.
Electrical (C-V) and physical (XPS, AFM) techniques are used with I-V measurement to provide a tool for intrinsic quality, defect landscape, and interfacial reliability of Al_2O_3 dielectrics in TFT applications.

6.3 Sample Preparation

The ZnO TFTs , shown in figure 6.1, were fabricated on a 150 mm p-type silicon wafer. A 30 nm Al_2O_3 gate insulator (225 cycles) and a 40 nm ZnO channel layer (333 cycles) were consecutively deposited by plasma-enhanced atomic layer deposition (PE-ALD) without breaking the vacuum Zeng et al. (2023), using trimethylaluminum (TMA) as the precursor for Al_2O_3 and diethylzinc (DEZ) for ZnO. Then, the ZnO channel was patterned by wet etching in 1:1000 $HCL:H_2O$. Finally, 5 nm of titanium

(Ti) and 150 nm of aluminium (Al) were deposited by RF magnetron sputtering and patterned using a lift-off process to form the source/drain (S/D) electrodes. The detailed information could be found in table A.3.

Notably, the Al_2O_3 films were deposited by varying the deposition temperature (150 $°C$, 200 $°C$, 250 $°C$, and 300 $°C$) to investigate the effect of deposition temperature on the quality of the dielectric material and interface properties in a systematic way. Since the amount works shows annealing process can enhance the surface quality of Al_2O_3 You et al. (2024); Theeuwes et al. (2021) , thus, a study of temperature deposition window is required in those applications that need low process temperature. The change in deposition temperature will impact not only the intrinsic film density and stoichiometry of Al_2O_3 , but also the surface morphology that is critical in determining the interface trap density and controllability of the gate.

It should be noted that a thin native SiO_2 layer (typically 1–2 nm) is inherently present on the silicon substrate surface. In this work, no intentional oxide removal was performed prior to ALD deposition. However, due to its ultrathin thickness compared to the 30 nm Al_2O_3 dielectric layer, its contribution to the overall gate capacitance and electric field distribution is negligible. Therefore, the electrical behavior is dominated by the Al_2O_3 dielectric layer.

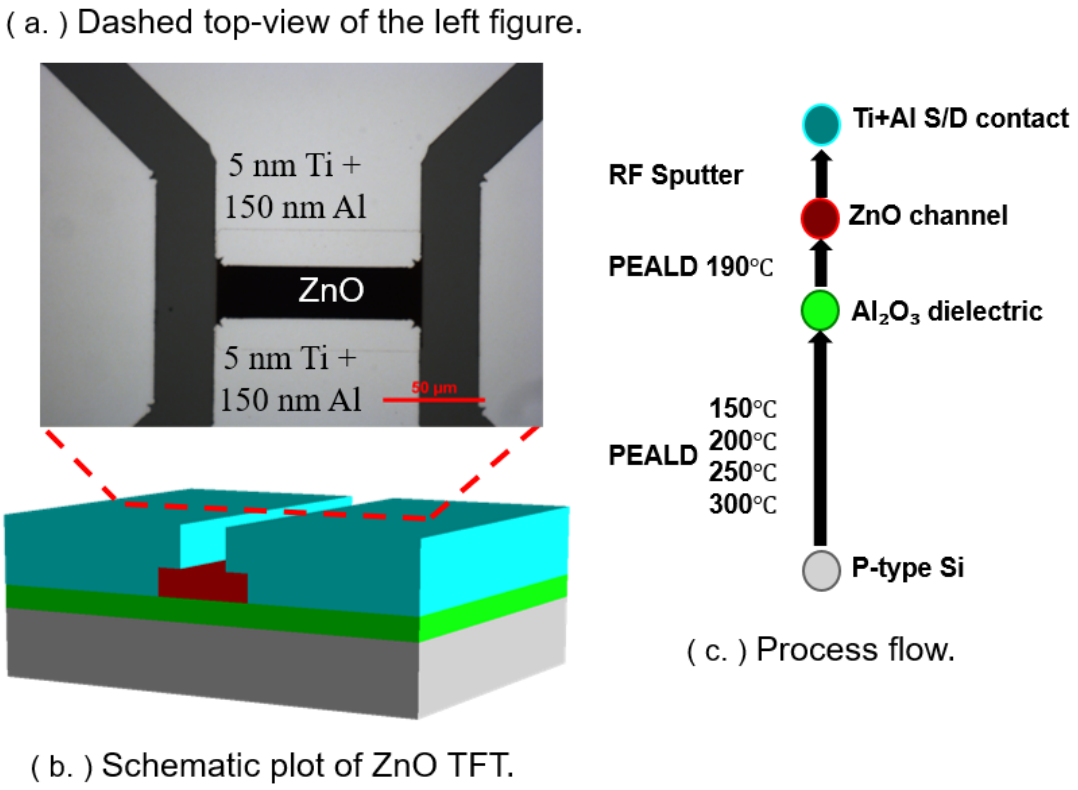


FIGURE 6.1: schematic illustration of the fabricated ZnO thin film transistor. The device uses Ti/Al bilayer (5 nm/150 nm) as source/drain contacts and Al_2O_3 dielectric on the gate deposited through plasma-enhanced atomic layer deposition (PEALD). To examine how thermal conditions affect the dielectric quality, surface morphology, and interface properties and allow a systematic study of their effects on device performance and reliability, the Al_2O_3 films were deposited at various deposition temperatures (150 $°C$, 200 $°C$, 250 $°C$, and 300 $°C$).

The sequence of fabrications offers a controlled platform to assess the correlation between electrical performance and reliability of ZnO TFTs and deposition temperature of Al_2O_3 . The temperature range of Al_2O_3 deposition can be varied systematically to assess the influence of temperature on critical Al_2O_3 deposition parameters (leakage current, hysteresis, interface quality, and surface roughness), providing useful information on the optimization of the dielectric layer in oxide semiconductor devices.

6.4 Experimental

The material and electrical properties are defined in this section, to explain how the deposition temperature of Al_2O_3 affects ZnO thin-film transistors. Structural and morphological features analysed by scanning electron microscopy (SEM) and atomic force microscopy (AFM) have supplied information on the uniformity of the film, its roughness, and exterior quality. Both the chemical composition of the Al_2O_3 layers and their bonding states were determined by X-ray photoelectron spectroscopy (XPS) to establish stoichiometry and the formation of defects. The electrical behaviour was explored and the principal device parameters having threshold voltage, mobility, and subthreshold slope were obtained by taking the current-voltage (I-V) measurements. In parallel with this, capacitance - voltage (C-V) characterisation has also been carried out to obtain the dielectric properties, hysteresis behaviour and tap density at the interface. All factors taken into consideration, give us a general picture of how deposition temperature affects the quality of materials of Al_2O_3, and ZnO TFTs stability during operation.

6.4.1 SEM Analysis

In figures 6.2 (a-e), SEM images of ZnO TFTs are shown with various channel widths (W_{ch} = 2-50 μm) at constant channel length, L_{ch} = 10 μm. Figure 6.2 (f-k) and Figure 6.2 (l-p) are used to visualize the images of the device structures, high-contrast processed images, and zoom-in images of the channel regions, respectively. It is noted that with the narrower channel, the channel edges become more irregular. The reason for this effect relies on the wet etching process, in which the etchant-surface interactions dominate the morphology of edges at feature sizes near the micrometre scale Gosálvez and Nieminen (2003). However, the dimension of the actual channel is in agreement with the designed values, which proves that the etching rate is well controlled and highly reproducible. This shows that the wet etching method is very reliable when it comes to attaining accurate channel geometry, even when the channel width is as small as 2 μm.

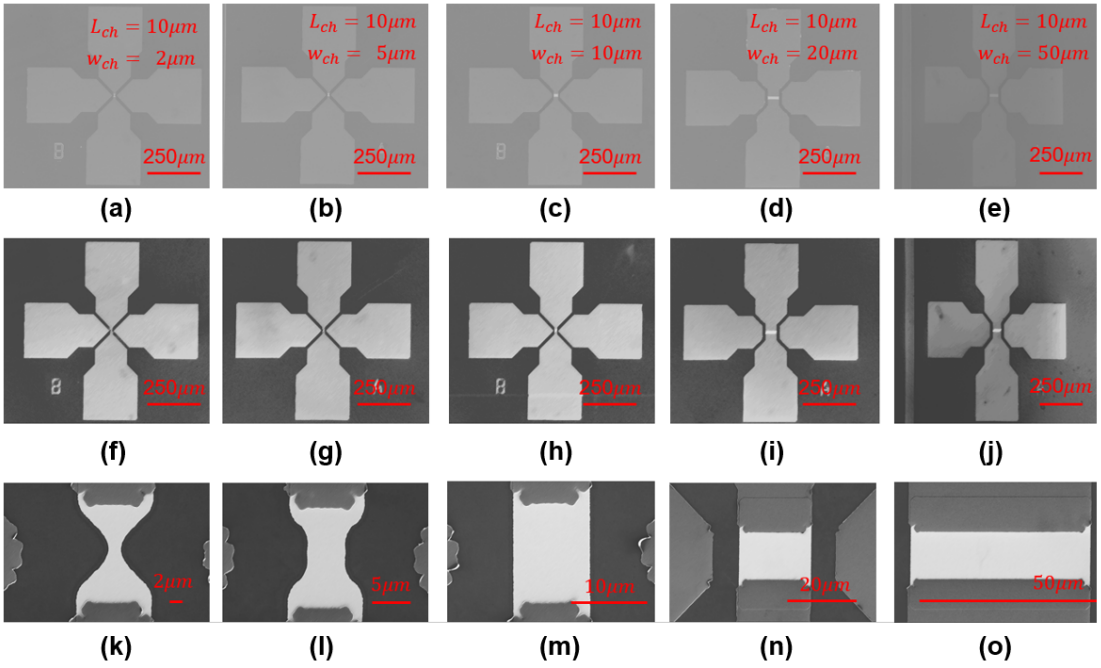


FIGURE 6.2: SEM plot of ZnO TFTs of varying channel widths at $L_{ch} = 10\mu m$.(a-e) original SEM images, (f-k) high-contrast processed images with highlight on the structure of the devices, and (l-p) zoom-in regions of channels. As channel width is reduced, edge roughness increases as a result of the wet etching process, under this defect, the channel dimensions are obtained as expected size, which means the etching rate has been controlled very well.

6.4.2 AFM Analysis

Figure 6.3 shows the AFM images of the deposited Al_2O_3 thin films at various temperatures (150–300 °C) over a scan area of 3×3 μm^2, with a height scale ranging from −15 nm to +15 nm. Two roughness parameters were extracted: the root mean square roughness (R_q), which is more sensitive to large surface deviations, and the arithmetic average roughness (R_a), which reflects the overall surface smoothness. At 150 °C, the film exhibits a smooth and uniform surface with a low roughness ($R_q = 0.579$ nm). When the deposition temperature increases to 200 °C, the surface roughness increases significantly ($R_q \approx 1.75$ nm), accompanied by the appearance of localized protrusions, indicating enhanced surface instability during growth. At 250 °C, the roughness decreases slightly ($R_q \approx 1.40$ nm), suggesting partial surface relaxation. Further increasing the deposition temperature to 300 °C results in a smoother surface ($R_q \approx 0.90$ nm), implying improved film densification and surface uniformity at higher temperature.

These results demonstrate that the surface morphology of Al_2O_3 films is strongly dependent on deposition temperature. The intermediate temperature range (200–250 °C) exhibits enhanced roughness, while higher temperature deposition promotes surface smoothing rather than grain growth, consistent with the amorphous nature of ALD-grown Al_2O_3.

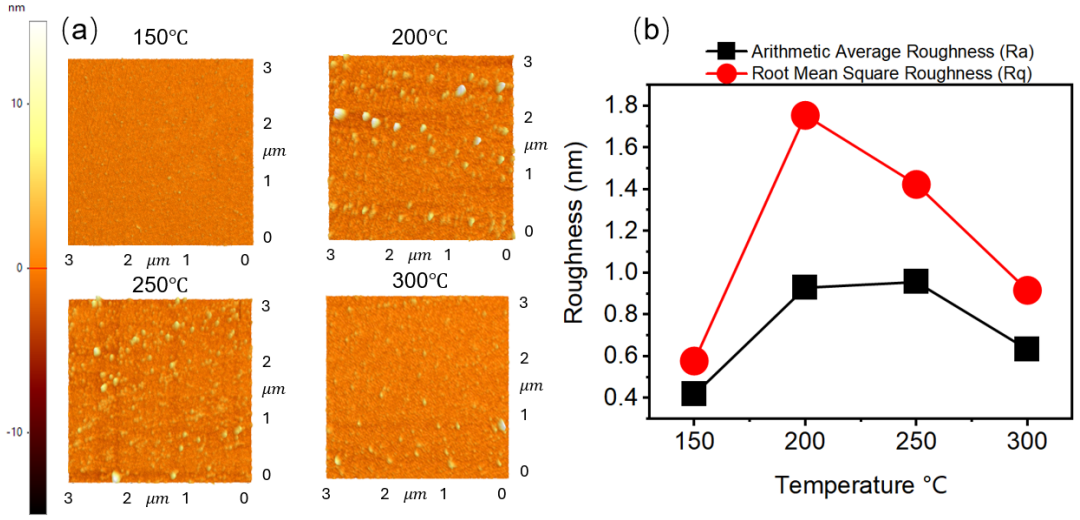


FIGURE 6.3: (a) Atomic force microscopy (AFM) topography images of PEALD-deposited Al_2O_3 films grown at 150 °C, 200 °C, 250 °C, and 300 °C (scan area: 3 μm × 3 μm). The surface morphology exhibits a clear temperature-dependent evolution, with more pronounced grain-like features appearing at intermediate deposition temperatures. (b) Extracted surface roughness parameters, including arithmetic average roughness (Ra) and root mean square roughness (Rq), as a function of deposition temperature. The roughness increases at 200 °C and 250 °C and decreases at 300 °C, suggesting improved surface uniformity at higher deposition temperature.

6.4.3 XPS Analysis

Figure 6.4 the survey spectra of Al_2O_3 thin films deposited were obtained at 150-300 $^{\circ}C$, and the spectra of the surface (a) were obtained and the bulk (b) were obtained after surface Ar etching. The main components identified are oxygen (O 1s, O KLL) and aluminium (Al 2s, Al 2p), which are the anticipated components of Al_2O_3. Besides this, there is also a C 1s peak on the surface with a strong peak on the 150 $^{\circ}C$ sample. This contamination of carbon may be due to residual organic ligands or adsorbates on the surface and is much lower at higher deposition temperatures, 200-300 $^{\circ}C$, indicating more thorough removal of the precursor-related species Van Meter et al. (2023). The bulk spectra (figure 6.4 (b)), on the other hand, indicate that the carbon

content at all deposition temperatures is negligible, and it is only present on the surface of the films and not within the films. The O 1s peak appears much stronger than the Al 2p signal, which can be attributed to the higher atomic ratio of oxygen in Al_2O_3 and the larger XPS sensitivity factor of O 1s. Moreover, the enhanced O 1s intensity at 150 $°C$ reflects the presence of hydroxyl groups and adsorbed oxygen. Moreover, the intensity of the O 1s and Al 2p peaks as compared to each other changes with temperature. At low temperature (150 $°C$), oxygen signal is dominant, which is typical of oxygen-rich or hydroxyl-rich environments. The signal of O 1s is reduced pronouncedly at higher temperature ($\geq$ 250 $°C$) indicating a shift towards slightly Al-rich films. These findings show that the deposition temperature has a significant impact on the surface cleanliness as well as bulk film composition.

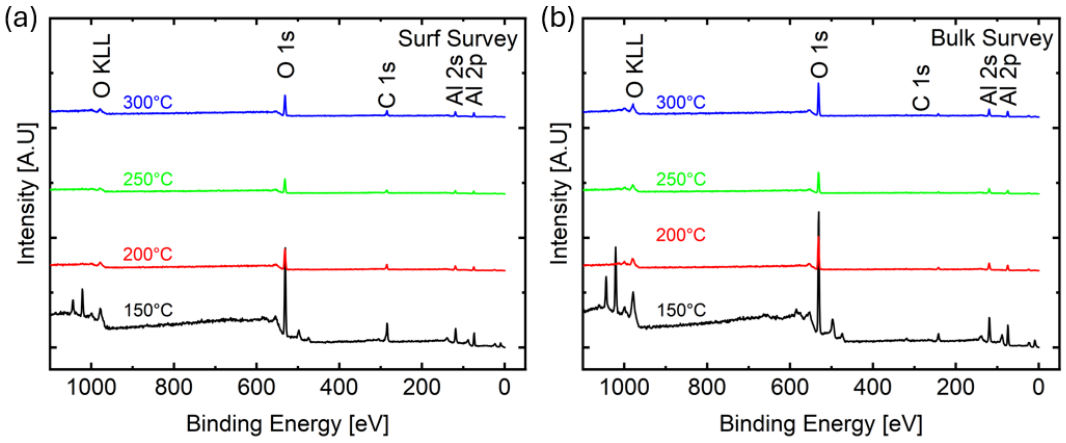


FIGURE 6.4: XPS survey spectra of Al_2O_3 films deposited at different temperatures: (a) surface survey and (b) bulk survey after sputtering. The dominant peaks correspond to O 1s, C 1s, Al 2s, Al 2p, and O KLL Auger transitions.

Figure 6.5 (a) shows that on the surface, the oxygen concentration reduces to around 49 % at 150 $°C$, then to about 43 % at 200 $°C$, then levelling out to about 42-43 % at 250-300 $°C$. The concentration of Al rises between 150 $°C$ and 200 $°C$ to about 30 %, slightly declines to about 28 % at 250 $°C$ and then again to about 32 % at 300 $°C$. The carbon concentration does not change monotonically: it is almost constant between 150 $°C$ and 200 $°C$ (almost 27 %), slightly increases to about 28 percent at 250 $°C$, and only decreases substantially to about 25 % at 300 $°C$. This suggests that during the temperature region of 200-250 $°C$, although there are material densification and partial removal of ligands, the surface is still hydroxylated or more reactive to

adsorbing carbon-containing species in the environment. The loss of surface hydroxyl groups and adsorbates at 300 $°C$ causes a significant decrease in the C concentration. The variation between 150 $°C$ and 200 $°C$ lies within the error bars. However, the variation at 250 $°C$ and the following decline at 300 $°C$ is out of the error margins, indicating that they are statistically relevant.

Figure 6.5 (b) shows that in the bulk, the oxygen content is reduced to about 62 % by 150 $°C$ to about 57 % by 200 $°C$, and is virtually constant over the range 250-300 $°C$, at approximately 56-57 %. Conversely, the concentration of the Al decreases to about 38 % at 150 $°C$ and rises to about 43 % at 200 $°C$ and remains constant at 43-44 % thereafter. The 150 $°C$ sample is slightly oxygen-rich, but the films deposited at $\geq$ 200 $°C$ are slightly Al-rich (oxygen-deficient) and can be stored without further temperature increase.

Figure 6.5 (c) shows the O/Al atomic ratio in the bulk decreases continuously with the deposition temperature, starting with a value of about 1.65 at 150 $°C$, then 1.33 at 200 $°C$, and then 1.29-1.30 at 250-300 $°C$. This shift to slightly oxygen-deficient films is entirely consistent with the bulk-concentration data in Figure 6.5 (b), and suggests that high deposition temperatures not only favour the removal the ligands and densification of films, but also tend to drive the films toward sub-stoichiometric Al-rich conditions.

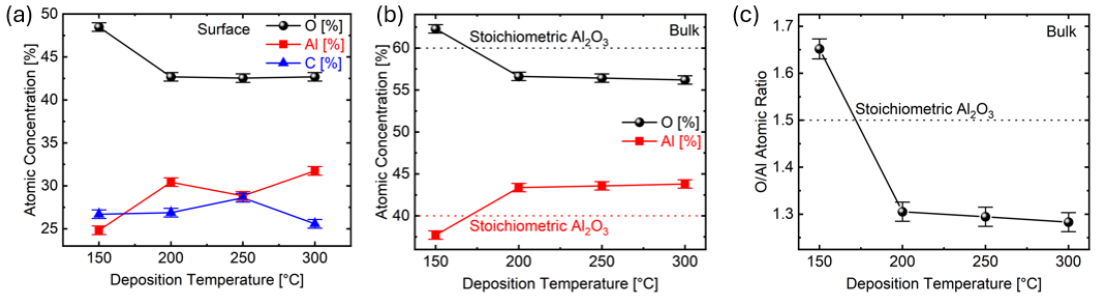


FIGURE 6.5: Atomic concentrations of Al_2O_3 films deposited at different temperatures extracted from XPS survey spectra: (a) surface chemical composition of O, Al, and C. (b) Bulk chemical composition of O and Al compared with stoichiometric Al_2O_3, and (c) O/Al atomic ratio in the bulk as a function of deposition temperature.

In general, these findings point to two mechanisms: at temperatures of 150-200 $°C$, the films are richer in oxygen and heavily contaminated with hydroxyl and carbon species on the surface. At temperatures of 250-300 $°C$, the films are cleaner and chemically more ordered, although the bulk is generally slightly oxygen-deficient. According to

the reaction of PEALD Al_2O_3 (equation 6.1, equation 6.2). This phenomenon is mainly attributed to the more thorough reaction of the Al precursor and more complete ligand removal at high temperature, but the supply of reactants such as oxygen or the reaction efficiency may be insufficient, resulting in an increase in oxygen vacancies and a tendency of Al enrichment in the film Ren et al. (2023).

Figure 6.6 presents the high-resolution O 1s spectra of Al_2O_3 thin films as a function of deposition temperature, recorded on the surface (figure 6.6 (a)) and in the bulk after Ar surface etching (figure 6.6 (b)). On the surface, the dominant peak at ∽531 eV corresponds to lattice O-Al bonding. A higher binding energy shoulder at ∽533 eV, assigned to hydroxyl groups or adsorbed oxygen species, is most pronounced at 150 $°C$, gradually weakens at 200-250 $°C$, and nearly disappears at 300 $°C$. This evolution indicates that at low-temperature deposition, the relative contribution of hydroxyl or adsorbed oxygen species is more pronounced, while higher deposition temperatures reduce these components and enhance the dominance of the lattice O–Al signal. In the bulk spectra, the main O–Al peak is also located at ∽531 eV and remains stable with temperature. However, two additional components are evident: a high-BE peak at ∽533-534 eV and a low-BE peak at ∽529-530 eV. The high-BE component reflects residual oxygen-related species or interstitial O, while the low-BE component is hard to declare. The influence of factors such as sputtering-induced reduction or spectral line fitting background cannot be ruled out. However, we suspect the low binding energy (BE) component (about 529–530 eV) may be related to local under-oxygenated or sub-oxidized coordination Rao et al. (1995). That low binding energy component is associated with oxygen-deficient or sub-oxide environments. The relative intensity of the low-BE peak increases slightly with deposition temperature, consistent with the compositional analysis in figures 6.5 (b-c), which showed a decreasing O/Al ratio and a shift toward Al-rich films. Taken together, the O 1s spectra confirm that increasing the deposition temperature improves surface cleanliness by removing hydroxyl and adsorbed oxygen.

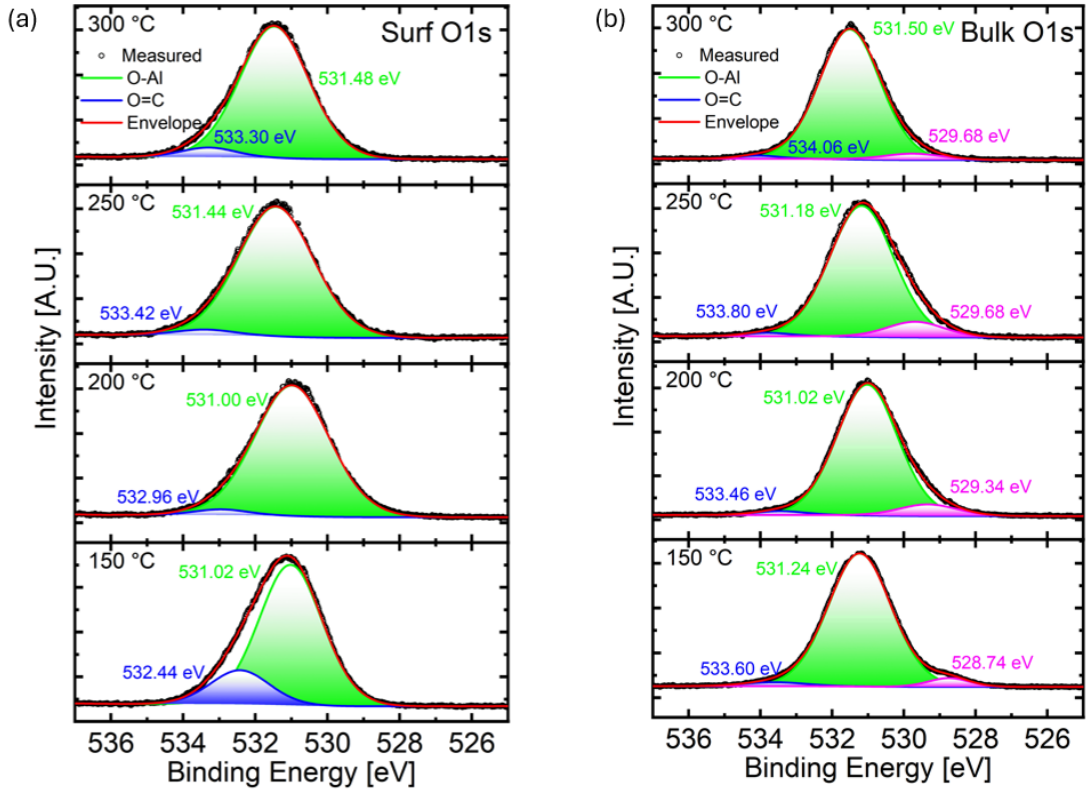


FIGURE 6.6: High-resolution O 1s spectra of Al_2O_3 films deposited at different temperatures: (a) surface and (b) bulk after sputtering. The spectra are showing peaks of lattice O-Al (∽531 eV), hydroxyl/adsorbed oxygen (∽533 eV), and low binding energy components (∽529-530 eV).

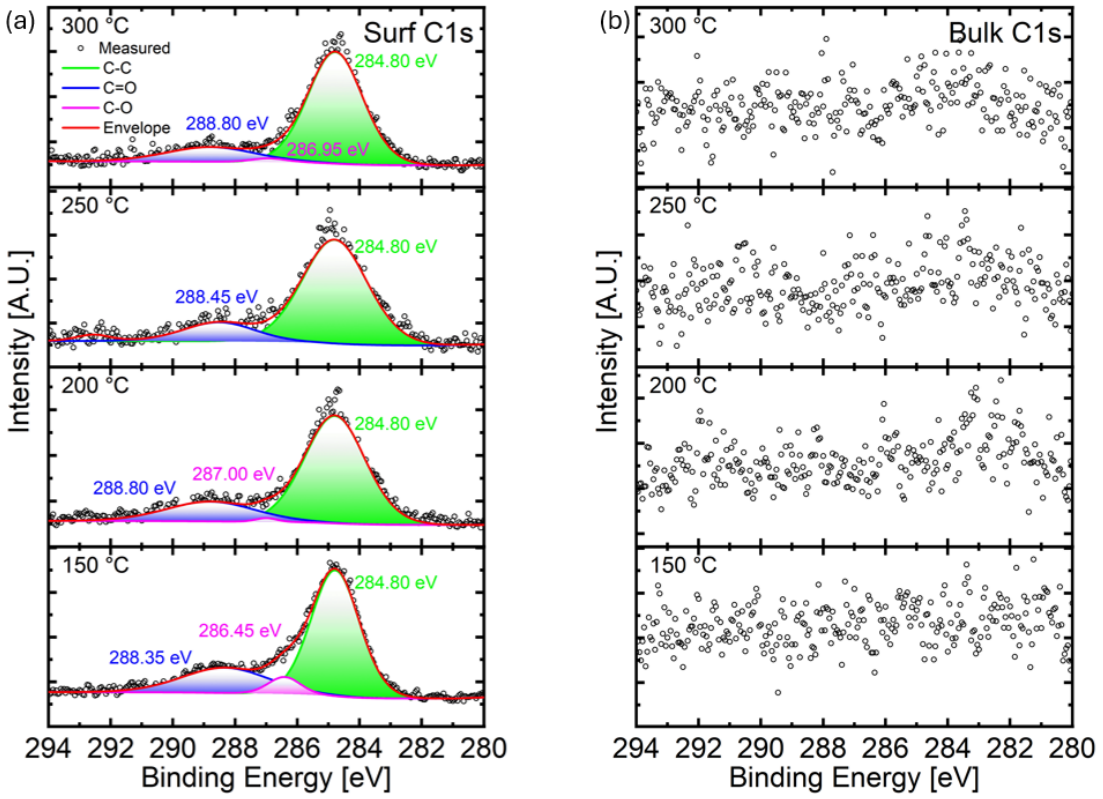


FIGURE 6.7: High-resolution C 1s spectra of Al_2O_3 films deposited at different temperatures: (a) surface and (b) bulk after surface etching. Surface spectra in surface are fitted with components centred $\backsim$ 284.8 eV (C-C/C-H), $\backsim$ 286.5-287.0 eV (C-O), and $\backsim$ 288.3-288.9 eV (O-C=O/carbonate-like). Bulk spectra show no clear C 1s peak within the signal-to-noise of the measurement.

Figure 6.7 presents the high-resolution C 1s spectra of Al_2O_3 thin films as a function of deposition temperature, recorded on the surface (figure 6.7 (a)) and in the bulk after Ar surface etching (figure 6.7 (b)).

Figure 6.7 (a) Surface C 1s: C 1s signal at the surface is not only dependent on deposition temperature as the temperature varies between 150 and 300 $°C$. The primary feature is at around 284.8 eV, which is usually C-C/C-H bonding, with higher binding energy shoulders at around 286.5-287.0 eV and 288.3-288.9 eV, usually C-O and O-C=O/carbonate-like, respectively. The overall intensity at 150 $°C$ is quite high, as well as at 200 $°C$. A small improvement or repacking of components is evidenced at 250 $°C$, especially in the 286-289 eV region, and at 300 $°C$ the total intensity is reduced significantly. It is worth noting that these assignments are chemical environment indicators based on peak fitting, but cannot be straightforwardly converted to quantitative concentrations of individual functional groups. The

determined temperature change is in line with the survey data, indicating carbonaceous or oxygenated adsorbates are still important at 150-250 $°C$ but are reduced significantly at 300 $°C$.

Figure 6.7 (b) Bulk C 1s: C 1s features are not visible in the 280-294 eV region after surface etching, and the signal is still at the noise level. This suggests that the amount of carbon in the bulk is less than the threshold of detection at the current conditions. This does not mean that the bulk is free of carbon altogether.

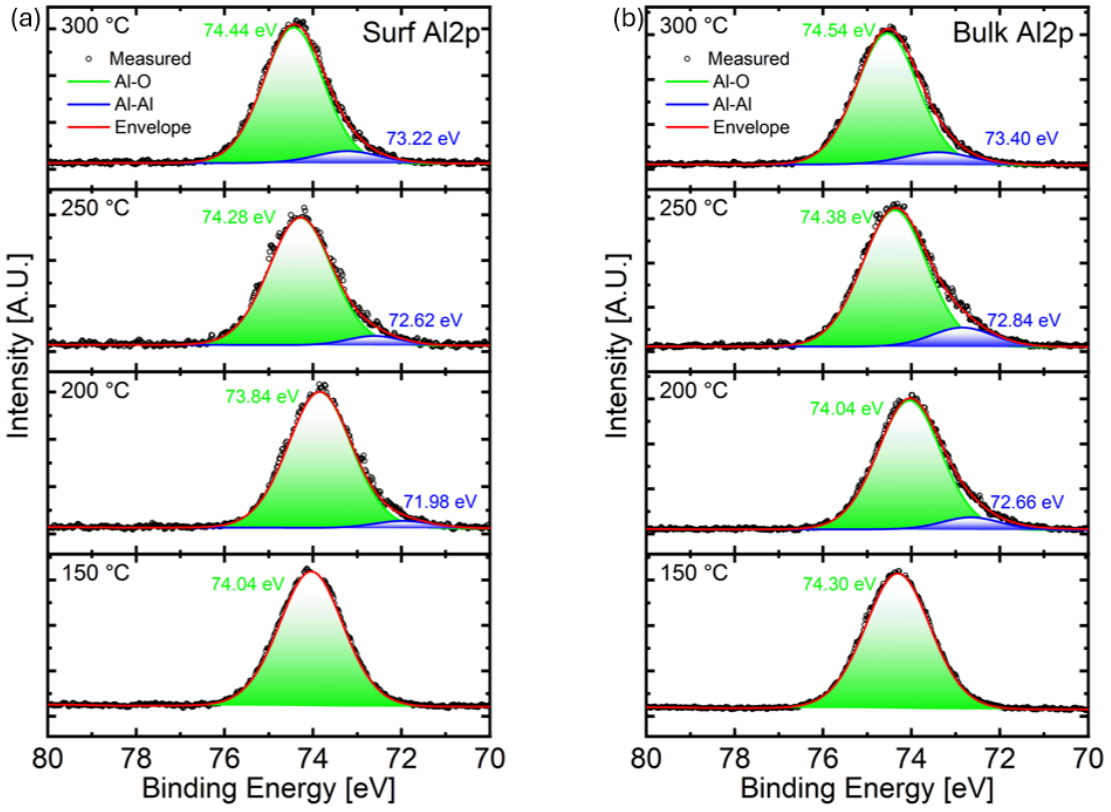


FIGURE 6.8: High-resolution Al 2p spectra of PE-ALD Al_2O_3 films at different deposition temperatures: (a) surface and (b) bulk after surface etching. Spectra are fitted with a main Al-O component ∽ 74.0-74.6 eV and a weaker low-bending energy (BE) shoulder (∽72.0-73.4 eV).

Ar^+ etching can also selectively etch carbon species near the surface or cause a reduction/redeposition effect, and absolute quantification can be affected by energy calibration conditions and charge compensation conditions Greczynski and Hultman (2020). The fact that no resolvable bulk C 1s signal was observed then implies that carbon is largely restricted to surface adsorbates or residual ligands and that any bulk carbon, where it exists, is at very low levels. Therefore, when combined with the O 1s

high-binding-energy components and the atomic concentrations of the survey spectra, the C 1s data show that increased deposition temperature decreases the relative portion of surface carbonaceous species and oxygen-containing functional groups, resulting in a cleaner surface. For the figure 6.8 (a) surface Al 2p: The primary peak is at 74.04 eV in the 150 $°C$ sample and moves slightly to higher binding energy, to 73.84 eV at 200 $°C$ and to 74.44 eV at 300 $°C$. This positive change can be linked to film densification. A weak low-BE shoulder is observed between approximately 71.98 eV (200 $°C$) and approximately 73.22 eV (300 $°C$). This property may be associated with oxygen-deficient or sub-oxide coordination, but may also be due to the constraints of fit or surface-related state and we should consider this shoulder a general indicator of non-stoichiometric local environments, to be interpreted together with the trend of O/Al ratio.
For the figure 6.8 (b) bulk Al 2p: The principal peak is moved to 74.54 eV (300 $°C$) as compared to 74.30 eV (150 $°C$), which is in agreement with the data on the surface. Between the range of $\backsim$ 72.66 eV and 73.40 eV, there is also a weakening of the shoulder on the low-BE side. Its development is, nevertheless, in line with the declining O/Al ratio, which was observed in the compositional analysis, and shows slight Al richness. Overall, the Al 2p spectra show a slight positive shift of the main peak with increasing deposition temperature and a slight enhancement of the low-BE shoulder. A reasonable interpretation is that higher temperature promotes film densification while also introducing a minor increase in non-stoichiometric local environments. Considering the O 1s results, it could be an Al rich situation Rao et al. (1995).

6.4.4 Film Density

As summarised in figure 6.9 and table 6.1, the growth per cycle (GPC) and the density of the Al_2O_3 deposited by PEALD clearly rely on the deposition temperature. As figure 6.9 indicates, the GPC gradually reduces with the rise in temperature. It is 0.121 nm/cycle at 150 $°C$ to 0.0876 nm/cycle at 300 $°C$. This decrease suggests that increased deposition temperatures make the film more dense Ren et al. (2023), and is usually explained by the fact that increased deposition temperature increases the rate at which the surface hydroxyl group is desorbed and the rate of surface reaction that reduces incomplete ligand exchange Khosla et al. (2021).

On the contrary, the film density, which was calculated by the following equations 6.3:

$$\rho = \frac{M_{\mathrm{Al_2O_3}}}{\mathrm{GPC} \cdot N_A} \tag{6.3}$$

Where $M_{Al_2O_3} = 101.96\ g/mol$ and $N_A = 6.022 \times 10^{23}\ /mol$ is the Avogadro's constant, exhibits the reverse tendency, and is shown in Figure 6.9 (b). The density rises gradually, 3.41 g/cm^3 at 150 $°C$ to 3.91 g/cm^3 at 300 $°C$, and is close to the reported bulk density of crystalline Al_2O_3 (3.95-4 g/cm^3)Pei et al. (2009). According to this trend, the lower the temperature at which the film was deposited, the higher the number of structural defects and residual hydroxyl impurities, resulting in a reduced packing density. When the temperature increases, the films get denser as the incorporation of volatile species decreases, and the atomic rearrangement is better, and the structural compactness of the amorphous Al_2O_3 network is improved.

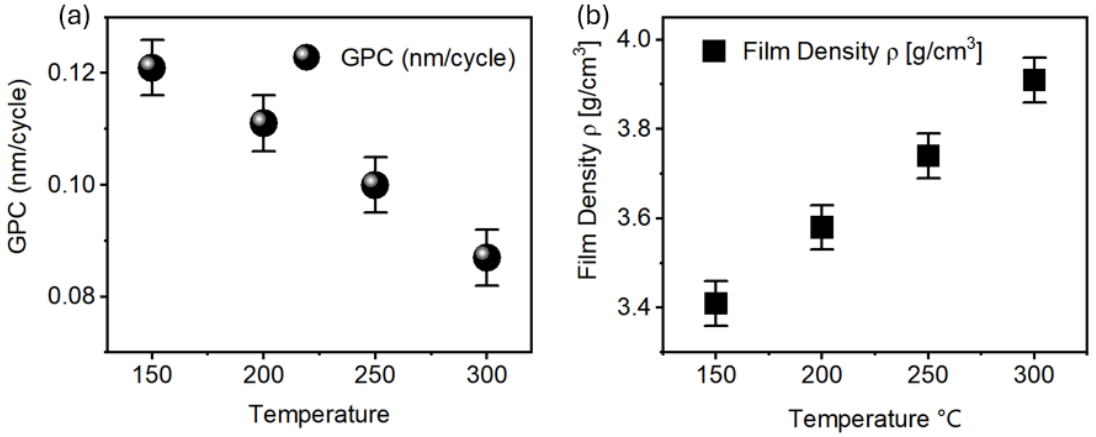


FIGURE 6.9: (a) PEALD Al_2O_3 growth per cycle (GPC) with deposition temperature. The GPC is lower at 300 $°C$ (0.0876 nm/cycle) than at 150 $°C$ (0.121 nm/cycle), which reflects a slower growth rate at higher temperatures. (b) Density of the film calculated by using the values of molecular weight of Al_2O_3 and Avogadro's constant calculated by the GPC. As temperature rises, the density rises to 3.91 g/cm^3, but close to the bulk density of crystalline Al_2O_3.

TABLE 6.1: *Summary of the thickness, calculated growth per cycle (GPC), and film density of PEALD Al_2O_3 films deposited at different substrate temperatures (150–300 $°C$). The results show a clear trend of decreasing GPC and increasing film density with higher deposition temperature.*

Temperature [$°C$]	**Avg. Thickness [nm]**	**Grow Per Cycle (GPC) [nm/cycle]**	**Film Density** ρ [g/cm^3]
150	36.29	1.21×10^{-8}	3.41 ± 0.05
200	33.31	1.11×10^{-8}	3.58 ± 0.05
250	29.94	9.98×10^{-9}	3.74 ± 0.05
300	26.29	8.76×10^{-9}	3.91 ± 0.05

In summary, the negative relationship between GPC and film density is a sign of a trade-off in the growth of PEALD Al_2O_3: the higher the temperature, the slower the growth rate per cycle, the faster the growth of the film to a dense film and possibly a film of higher quality dielectric. This is one of the reasons why post annealing can improve the quality of Al_2O_3 interface. These data are in agreement with the overall knowledge that low-temperature ALD will prefer higher GPC but yield less dense films because surface reactions have not occurred to completion, but high temperatures improve the quality of the film at the cost of decreased deposition efficiency.

6.4.5 Current-Voltage (I_D-V_G) Linear Transfer Characteristic Analysis

Figure 6.10 shows the transfer curves ($I_D - V_G$) that were all measured at room temperature as forward sweeps at a constant channel length (10 μm). The channel length in the devices is fixed to 10 μm, channel width was adjusted between 2 and 50 μm which represents the W/L ratios between 0.2 and 5. The gate voltage was swept between -5 V and $+5$ V with an increment of 0.1 V and the drain voltage was adjusted to 1 V, 7.5 V. In all cases I_D increases with increased V_G, though the off-state current is near the baseline.

Increasing channel width increases the drain current at that bias, as expected with increasing W/L, and increasing V_D increases the current level, and increases the separation between the transfer curves of different deposition temperatures. The current of the drain is ordered by the same rule in all device dimensions and all bias, with the 250 $^\circ C$ sample having the highest current, and the 150 $^\circ C$ sample having the lowest current. The temperature dependence is more pronounced as the channel width and the drain voltages increase.

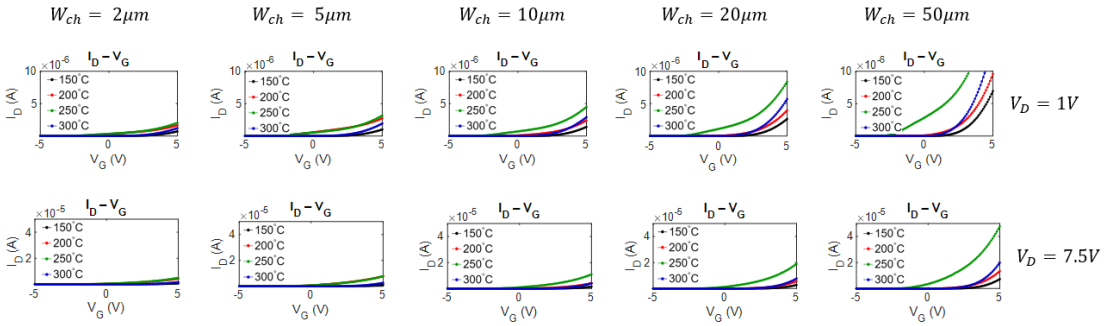


FIGURE 6.10: Forward transfer properties ($I_D - V_G$) of ZnO TFTs deposited at various Al_2O_3 deposition temperatures (150 °C: black, 200 °C: red, 250 °C: green, 300 °C: blue).

Although Fig. 6.10 presents the forward transfer sweeps for clarity and direct comparison of current levels, forward–backward hysteresis was also measured for the same devices and bias conditions. The hysteresis voltage (ΔV_{Hys}) is discussed separately in Chapter 7, where the dependence on deposition temperature and device geometry is quantified.

6.4.6 Logarithm Current-Voltage (Log I_D-V_G) Linear Transfer Characteristic Analysis

In order to observe the device properties in the subthreshold region further, the transfer curves are re-plotted in the logarithmic current scale. Although the linear-scale $I_D - V_G$ plots clearly show the overall current versus channel width and drain bias, the logarithmic scale gives a view of the current in the off state and the subthreshold region 6.11. This enables a better extraction of important device features including threshold voltage (V_{TH}) and subthreshold slope (SS).

The drain current has a longer platform region than the threshold region in the logarithmic transfer curves at V_D = 1 V and 7.5 V. This platform is found at 10^{-10} A and is very similar to all deposition temperatures and channel widths. The form of the behaviour indicates that the measured current is not due to channel conduction, but is dominated by the noise floor of the baseline or a leakage path that does not depend on the presence or absence of a gate. A platform of this type is commonly identified with the sensitivity limit of the measurement system and perhaps with residual substrate or contact leakage. As a result, intrinsic switching properties of the devices are not

manifested in this region, and significant differences between deposition temperatures can only be observed when approaching the threshold region.

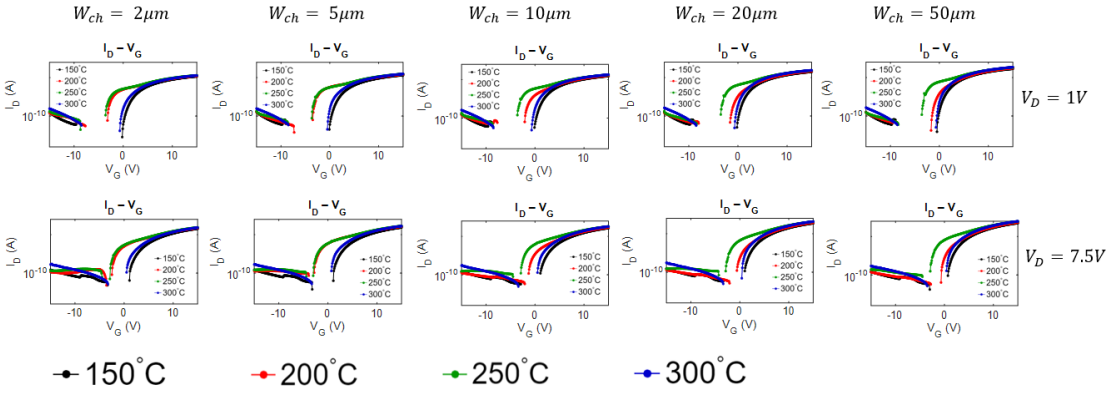


FIGURE 6.11: Log-scale transfer characteristics ($I_D - V_G$) of ZnO TFTs with channel lengths L_{ch} = 10 μm and channel widths of 2, 5, 10, 20 and 50 μm. The rows were set to drain voltages V_D = 1, 7.5 V, forward sweeps were done at room temperature and V_G was swept between −15 V and +15 V.

In the case of the devices deposited Al_2O_3 at 200 °C, there is a significant shift in the threshold voltage with the increasing channel width. This can be seen more clearly in the change in W = 5 μm to W = 10 μm where the apparent turn-on voltage is pushed to more positive values. The shift is always reproducible at other drain biases, which implies that the shift is not a measurement artefact. Conversely, the other deposition temperatures display quite constant threshold positions with respect to channel width. This width-dependent V_{TH} shift implies that the 200 °C films can be sensitive to channel geometry-related effects, including the interface states that are non-uniformly distributed over the channel area, or the contact resistance that affects the results at intermediate widths. The observation that this unusual behavior does not occur in devices deposited at 150 °C and 250 °C suggests a temperature-dependent sensitivity of the interface properties. In these samples, improved surface morphology and chemical uniformity, as indicated by AFM and XPS analysis, are consistent with enhanced dielectric stability. By contrast, the devices fabricated at 200 °C exhibit a stronger dependence of V_{TH} on channel width, implying that the interface formed at this deposition temperature may be more susceptible to geometry-related effects and scaling-induced non-uniformities.

6.4.7 Current-Voltage (I_D-V_D) Output Characteristic Analysis

Although threshold voltage behaviour and switching behaviour are important in the transfer characteristic, the output characteristics ($I_D - V_D$) are needed to assess charge transport at different drain bias values and to determine whether the devices have attained appropriate linear-to-saturation transitions.

The output properties ($I_D - V_D$) of ZnO TFTs at channel lengths $L_{ch} = 10\ \mu m$ and varying channel widths between 2 and 50 μm. The current at the drain increases monotonically with V_D at every width and tends to reach a near-saturation region as the drain bias rises. Both the level of current and the difference between deposition temperatures are more pronounced as the channel width increases. Specifically, the 250 $^{\circ}C$ devices have higher I_D than the 150 $^{\circ}C$ and 200 $^{\circ}C$ counterparts, and the 300 $^{\circ}C$ devices have competitive or larger currents at wider channels ($\geq$20 μm). With the widest devices (50 μm) the drain current is in the 10^{-4} A range, and varies with channel width, which proves that the conduction of current is directly proportional to the W/L ratio. No abnormal crowding of currents or negative resistance is recorded between the measured limits of bias. It should be noted that, due to lithographic and etch bias during device processing, the effective channel width may differ from the design value and was not independently metrologically verified for each device, therefore, the widths quoted in this section should be interpreted as nominal values.

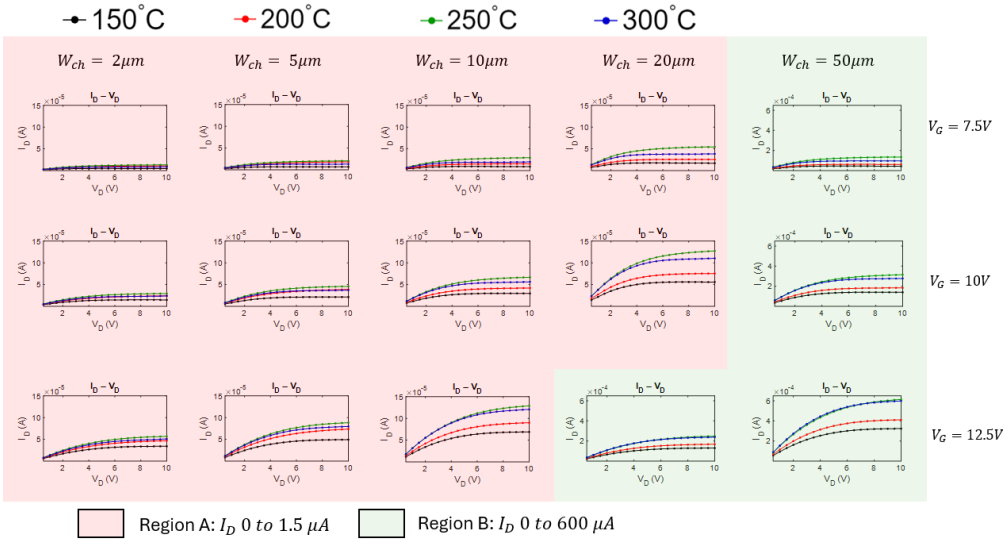


FIGURE 6.12: Output characteristics ($I_D - V_D$) of ZnO TFTs deposited at 150 °C (black), 200 °C (red), 250 °C (green) and 300 °C (blue), channel length L_{ch} = 10 μm and channel widths of 2, 5, 10, 20 and 50 μm. However, the drain current is proportional to channel width and V_D and tends to near saturation at large drain bias. At small widths the currents are small and the temperature effects less pronounced, but at broader channels the 250 °C and 300 °C devices provide the highest drive currents.

6.4.8 Parameter Extraction and Comprehensive Analysis

Figure 6.13 is a summary of the electrical parameters (threshold voltage I_D, trap density N_{trap}, field effect mobility μ_{FE}, maximum gate leakage current I_{Gmax}, and changes in I_D and SS ΔV_{TH} and ΔSS) that were extracted by depositing Al_2O_3 of the devices at 150-300 °C and using channel widths of 2 to 50 μm.

At low drain bias (V_D = 1 V) both linear and logarithmic scale transfer characteristics showed that the 200 °C devices had an unexpected positive I_D shift, and this was especially shown as the channel width was increased between 5 μm and 10 μm. This is in line with the parameter plots where ΔV_{TH} and ΔSS have maxima at 200 °C, indicating poor interface stability in this deposition condition. In comparison, the 150 °C devices exhibit comparatively constant values of I_D at low ΔV_{TH} and ΔSS, which implies strong switching with reduced absolute drain current.

On the logarithmic $I_D - V_G$ curves at higher drain bias (V_D = 7.5 V and 15 V) the 250 °C and 300 °C devices slowly lost gate control, with reduced subthreshold slopes and increased off-state currents. This can be seen in the extracted parameters: N_{trap} and ΔSS steeply increase at 300 °C, and I_{Gmax} is the highest value ($\sim 10^{-9}$ A), which is a

sign of degraded dielectric performance. Although the 250 $°C$ group offers the highest on-current in the $I_D - V_G$ and $I_D - V_D$ plots, it also has a greater variability in ΔV_{TH} and ΔSS under high drain bias indicating that the apparent performance gain is achieved at the expense of stability.

The devices characterised by 150 $°C$, however, exhibit the same behaviour during all analyses. They have obvious switching and no abnormal turn-on behaviour in the $I_D - V_G$ and log $I_D - V_G$ plots. The current in the $I_D - V_D$ characteristics is predictable with the channel width, but does not exhibit the anomalies at 200 $°C$ or the high-field degradation at 300 $°C$. The 150 $°C$ devices in the extracted parameter plots have the lowest ΔV_{TH} and ΔSS at $V_D = 1$ V and 15 V, and also have the lowest gate leakage currents. Their absolute μ_{FE} and drive current are a little less than the 250 $°C$ devices, but their switching stability and reliability are better in general.

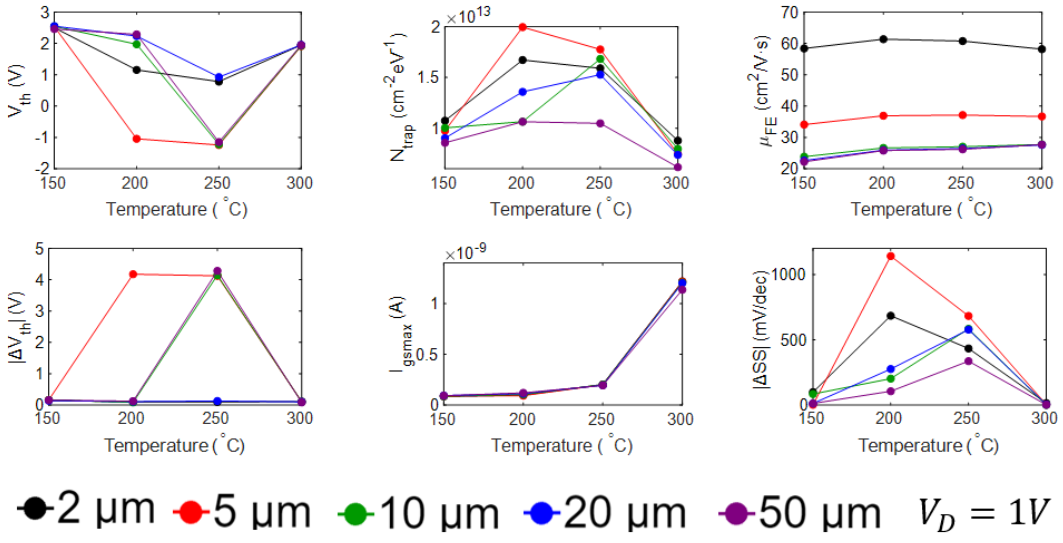


FIGURE 6.13: Parameters of the extracted devices versus Al_2O_3 deposition temperature and channel width at $V_D = 1$ V.

A combination of the outcomes of $I_D - V_G$, log $I_D - V_G$, $I_D - V_D$, and parameter extraction proves that the 250 $°C$ condition is optimal in terms of drive current, whereas the 150 $°C$ condition is the most stable of all. This trade-off highlights that the deposition temperature is a determinant of whether the device will be more performant or more reliable. The most stable and reliable condition found is the deposition temperature of 150 $°C$, with low threshold voltage change, small hysteresis and strong gate control at all channel widths and drain biases.

It should be noted that uncertainties in the extracted FET parameters may arise from several sources related to the Al_2O_3 gate dielectric. Although identical deposition recipes were employed, the physical thickness (T_{ox}) of Al_2O_3 films deposited at different temperatures can vary due to temperature-dependent growth kinetics. In this work, the gate capacitance (C_{ox}) used for parameter extraction was obtained from MIS capacitor structures fabricated with Al_2O_3 films of corresponding thickness. However, it is also important to note that the channel width-to-length ratio (W/L) used in the calculations was based on the designed, ideal device dimensions. In practice, edge defects and process-induced non-idealities become increasingly significant for small-geometry devices, leading to additional uncertainty in the extracted electrical parameters. As a result, the parameters derived for small-dimension devices, particularly the field-effect mobility, should be interpreted as effective values intended for comparative trend analysis rather than as absolute transport parameters.

6.4.9 C–V Characteristics and Hysteresis Behaviour

Although transfer characteristics, output characteristics and extracted parameters may offer useful information about device switching behaviour and stability, they are mostly measures of channel transfer properties. Thus, capacitance-voltage (C- V) measurements can give a better understanding of the quality of the dielectric and investigate the contribution of interface states directly.

The high-frequency C-V characteristics of Al_2O_3/p-Si Metal-Insulator-Semiconductor (MIS) capacitors deposited at 150-300 $°C$ are shown in figure 6.14 (a). The curves are p-type characteristics as the p-type silicon substrate is adapted. When the negative gate bias is applied, holes will pile up at the semiconductor-oxide interface, and the highest capacitance will be achieved due to the T_{dep} being lowest. With a positive sweep of the gate bias, the surface is pushed into depletion and trying to inversion, but because of the highly doped p-type silicon, there are not many electrons for inversion, and the measured capacitance decreases substantially. The consecutive accumulation - depletion process verifies the p-type nature of the substrate and forms the basis of the interpretation of the hysteresis behaviour.

The forward and reverse sweeps show different hysteresis windows at all deposition temperatures. The deposition temperature increases the width of the hysteresis, implying that the dielectric or interface is trapping charges much easier. The devices

with the highest accumulation capacitance (~1.9 x 10^{-7} F/cm^2) and the smallest hysteresis window ($\Delta V_{TH} \approx 0.6$ V) are the 150 °C devices, which show comparatively steady dielectric behaviour. In comparison, the 300 °C films have the greatest accumulation capacitance (~2.6 x 10^{-7} F/cm^2) and the greatest hysteresis (ΔV_{TH} up to 1.8 V), suggesting that there are more trapping centres. These two extremes are in between the 200 °C and 250 °C samples with intermediate capacitance values and hysteresis widths.

Figure 6.14 (b) also measures this trend by plotting hysteresis shift ΔV_{TH} vs. capacitance, the orange window, that is marked in figure 6.14 (a). ΔV_{TH} increases with deposition temperature in a systematic way across the whole capacitance range, which is in agreement with more vigorous charge trapping in films deposited at higher temperatures. This observation is in good agreement with the degraded subthreshold swing and higher density of interface traps based on the I-V measurements.

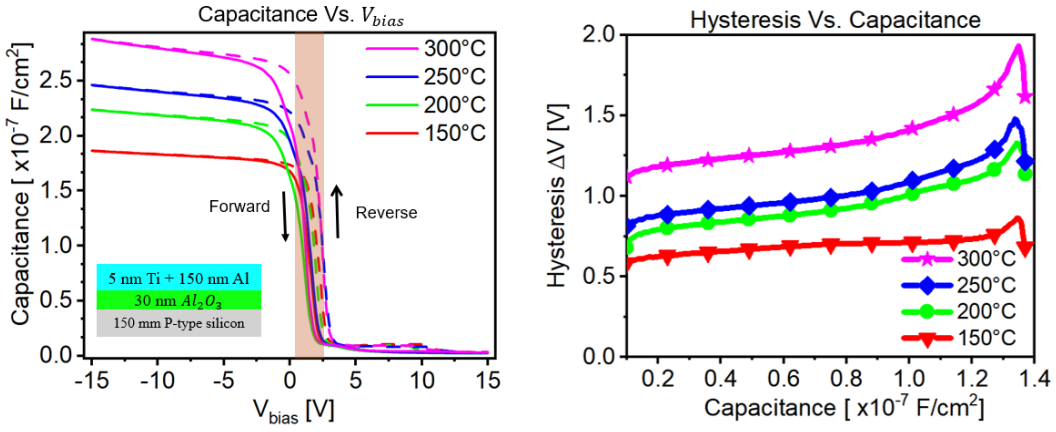


FIGURE 6.14: (a) The capacitance voltage (C-V) characteristics of Al_2O_3/p-Si Metal-Insulator-Semiconductor (MIS) capacitors deposited at 150, 200, 250, and 300 °C at high frequency. Forward and reverse sweeps show windows of hysteresis that rise with deposition temperature. (b) Hysteresis voltage shift (ΔV_{TH}) vs. accumulation capacitance, with a systematic rise in ΔV_{TH} with accumulation capacitance between 150 °C and 300 °C.

6.5 Results and Conclusion

We have developed a detailed correlation in this chapter between the deposition temperature of Al_2O_3, its structural and chemical characteristics, and the electrical behavior of ZnO TFTs. The GPC-density measurements showed that the

growth-per-cycle (GPC) decreases with the deposition temperature, but the film densification increases, meaning that more compact dielectric layers are formed at higher temperatures. This trend was also supported by XPS, which revealed that low-temperature films are hydroxyl-rich, but higher-temperature films are oxygen-deficient, and AFM revealed that the 150 $°C$ films have the smoothest surface morphology and that roughness increases with deposition temperature. Even these material-level observations already indicated that there was a trade-off between chemistry defects and dielectric performance, and that trade-off was systematically presented in the electrical measurements.

Based on the transfer characteristics ($I_D - V_G$), it was realized that devices deposited at 250 $°C$ have the highest drive currents, whereas those deposited at 150 $°C$ run with lower conduction currents, but with more stable switching. The logarithmic $I_D - V_G$ plots also revealed two major anomalies: a flat current platform at around 10^{-10} A of $V_D = 1$, 7.5 V due to the measurement floor or the gate-independent leakage, and progressive loss of switching ability of the 250 $°C$ and 300 $°C$ samples at $V_D = 15$ V, indicating reduced gate control in high electric fields. Output characteristics (I_D-V_D) demonstrated that current scales predictably with channel width, up to the 10^{-4} A range at W = 50 μm, and the 250 $°C$ and 300 $°C$ devices are better driven in wide channels, although the 150 $°C$ devices are more consistent across all geometries. An especially dramatic instability was noticed in the 200 $°C$ group, as a strong shift in V_{TH} appeared as the channel width changed between 5 and 10 μm, which is indicative of a geometry-sensitive distribution of interface states.

These differences were further supported by parameter extraction. Field-effect mobility and on-current reached their maximum at 250 $°C$, and both δV_{TH} and δSS increased more with higher drain bias, which indicated a loss of stability. I_{Gmax} and N_{trap} increased sharply at 300 $°C$, and were associated with reduced subthreshold slopes and higher leakage, as would be expected of oxygen-deficient environments of the type found with XPS. Conversely, the 150 $°C$ devices all had the lowest δV_{TH} and δSS, low leakage currents, and constant threshold locations with respect to width and biases, and showed the most predictable behaviour in reduced current levels.

This interpretation was supported by the dielectric-level analysis based on C-V measurements. The p-type characteristics of the Al_2O_3/p-Si MIS capacitors were observed as the accumulation at negative bias and depletion at positive bias. More to the point, the systematically increasing hysteresis window with deposition

temperature, between about 0.6 V at 150 $°C$ and about 1.8 V at 300 $°C$, was a direct consequence of the growing amount of trap-assisted charge storage. These measurements were performed on p-Si instead of ZnO, but this methodological decision was necessary to extract C_{ox}, hysteresis and trap-related shifts reliably, as they cannot be reproducibly extracted through thin ZnO channels because of leakage and parasitic conduction. Since the Al_2O_3 layers were deposited in the same conditions as in the TFTs, the C-V results can be directly applied to the device gate dielectric, to complement the I-V analysis, and to ensure the trends found in the electrically measured devices can be traced to intrinsic dielectric and interface properties.
Collectively, all measurements lead to one and the same conclusion: deposition temperature determines a trade-off between performance and reliability. The 250 $°C$ condition maximizes the drive current and mobility, at the cost of increased instability under bias. The 300 $°C$ condition is further degraded by the oxygen-deficient environments. The 200 $°C$ condition is degraded by anomalous threshold instabilities due to geometry issues, but the 150 $°C$ condition is the best by the most stable operation with the lowest hysteresis, low leakage, and strong gate control. This shows that 150 $°C$ is the most dependable deposition temperature condition in low-temperature oxide electronics where the stability of the device is of greatest importance.
However, the analyses so far have been made on static, dark measurements which mainly describe behaviour without environmental interference. They fail to demonstrate clearly the dynamics of charge trapping and defect activation under operating stress. Defect states in wide-bandgap ZnO systems have been known to be responsive to electrical bias and photon excitation, and light can activate sub-gap states and speed up changes in threshold voltages Castillo-Saenz et al. (2022b). In order to fill in the mechanistic picture and put to the strict test the stability of these devices in realistic circumstances, the following chapter introduces optical positive and negative bias.

Chapter 7

Optical Bias Stress Instability of ZnO Thin-Film Transistors with Al_2O_3 Gate Dielectrics Deposited at Different Temperatures

7.1 Introduction

Stability of oxide semiconductor thin-film transistors (TFTs) during operations remains one of the most urgent concerns regarding their real-world applications in display backplanes, sensors, and flexible electronic bases Kang et al. (2025). More precisely, the long-term positive (PBS) or negative (NBS) gate bias stress instability (through changes in threshold voltage, V_{TH}) in ZnO-based TFTs has been a common phenomenon and is typically attributed to the trapping of charges in gate dielectrics and interface states Daus et al. (2025); Castillo-Saenz et al. (2022b); Li et al. (2022). Despite the enormous progress in the optimization of device geometries and channel deposition methodologies, the gate dielectric and its interface with ZnO are still factors that can determine the device reliability Zhang and Cho (2024); Jeon et al. (2020); Wang et al. (2024).

Normally, these devices are working in complex environments rather than stable, dark. The optical effect of the device is a non-negligible case that needs to be paid attention

to. The optical excitation includes the fact that photon energy similar to or lower than the bandgap of a semiconductor (∼3.3 eV) can drive defect states within the semiconductor or at the dielectric interface Scolfaro et al. (2018). Electron–hole pairs generated by ultraviolet illumination above the bandgap increase the rate of charge trapping, whereas sub-bandgap excitation can interact with oxygen vacancies and hydroxyl-related defect states, modifying their charge states and leading to persistent photoconductivity or additional instability Cabral et al. (2020). Consequently, light irradiation / electrical bias interaction, also called optical bias stress, is an important reliability issue of oxide TFTs.

Atomic layer deposition (ALD) or plasma-enhanced ALD (PEALD) Al_2O_3 is widely employed as a gate dielectric due to its moderate permittivity (∼ 9), low leakage current, and compatibility with ZnO interfaces Oh et al. (2024); Calzolaro et al. (2022). Previous studies have reported that the dielectric properties of ALD-grown Al_2O_3 are sensitive to deposition temperature, which can influence hydroxyl incorporation, oxygen-vacancy-related defects, and overall film density Nam et al. (2016); Zhang et al. (2011); Weber et al. (2011). In particular, low-temperature deposition has been associated with increased residual –OH groups and structural imperfections, whereas higher deposition temperatures are generally reported to promote film densification and reduced defect-related charge trapping Castillo-Saenz et al. (2022b).

In this chapter, we discuss the optical PBS/NBS instability of ZnO TFTs and Al_2O_3 dielectric deposited at different temperatures (150-300 $°C$). Four wavelengths of illumination (340, 365, 405 and 490 nm) are used to probe the interaction of photon excited carriers with dielectric- and interface-related defects. The significant focus is to describe the stability of the devices when the identical optical stress conditions are applied to them by changing the relative dielectric quality through deposition temperature. The results are also discussed in connection with the previously obtained material and electrical description (XPS, AFM, C-V, and I-V analyses) to establish a unified understanding of the defect environment of the Al_2O_3/ZnO interface.

7.2 Literature Review

Oxide semiconductor thin-film transistors (TFTs) have received much focus with regard to their great potential in display, sensors, future flexible electronics and

applications using back end of line (BEOL) process due to the reliability they present Zhang et al. (2022); Petti et al. (2016); Zhang et al. (2019a). Among the other reliability problems, the instability of bias stress, as a result of changing the threshold voltage under long-duration gate bias, is one of the most important problems Na et al. (2024); Yang et al. (2022a). Moreover, the optical excitation adds additional complexity, because the carriers and defect states generated by photo-processes interact with the trapping processes caused by the bias, and this induces increased degradation Yang et al. (2022a). The past research has examined bias stressing Sun et al. (2024b), fundamental defect physics of ZnO Rowlinson et al. (2024b), optical bias stress in oxide semiconductors and the influence of Al_2O_3 gate dielectrics Castillo-Saenz et al. (2022a). Nevertheless, there is still limited systematic knowledge on the effect of dielectric deposition temperature on optical bias stress stability of ZnO TFTs. The pertinent literature is reviewed in this section starting with bias stress instability in oxide TFTs, optical excitation and defect states in ZnO, optical bias stress phenomena, and the influence of the deposition temperature of Al_2O_3, before pointing to the knowledge gap that underlies the current research.

7.2.1 Bias Stress Instability in Oxide TFTs

One of the most significant reliability concerns of oxide thin-film transistors (TFTs) is widely known as bias stress instability. Devices tend to shift threshold voltage, mobility and hysteresis when exposed to long-term gate bias, and these effects severely restrict their stability in operation Na et al. (2024); Yang et al. (2022a); Rowlinson et al. (2024b). The positive bias stress (PBS) typically causes trapping of electrons at the dielectric/channel interface or in the gate dielectric, which causes a positive shift in the value of V_{TH} without much deterioration of subthreshold slope (SS) or mobility Daus et al. (2025) . Negative bias stress (NBS), in comparison, is more complicated and highly relates to device set-up, geometry, and dielectric characteristics. The NBS frequently causes negative shifts in the V_{TH}, decreases in the mobility and develops the hump-like features of the transfer curves Castillo-Saenz et al. (2022b) . Compared to PBS, NBS is more complex because it involves multiple processes such as hole capture, interface state generation, and carrier diffusion.

7.2.2 Optical Excitation, Defect Physics in ZnO and Interface States from Al_2O_3

It is the interactions of intrinsic defects in ZnO with interface-based defect states due to the Al_2O_3 gate dielectric that strongly dictate the response of ZnO thin-film transistors to optical excitation. ZnO is a wide-bandgap semiconductor ($\sim$ 3.3 eV), and therefore very sensitive to ultraviolet and sub-bandgap photons, which may excite donor- and acceptor-like defect levels. These defect states affect carrier generation, recombination and trapping dynamics and hence determine the extent of threshold voltage instability on optical PBS and NBS conditions.

Native point defects in ZnO, such as oxygen vacancies (V_{O}) and zinc interstitials (Zn_{i}), are frequently described as donor-like defects in certain charge states, although their exact contribution to intrinsic n-type conductivity remains under debate Bandopadhyay and Mitra (2015). Photoluminescence studies have associated violet-blue emission bands with Zn_{i}-related states and green-orange visible bands with oxygen-vacancy-related defects; however, the microscopic origin of these emissions is still actively discussed in the literature. These defect states can be photo-ionized under illumination, generating excess free carriers and contributing to persistent photoconductivity (PPC), which may enhance positive threshold voltage shifts during PBS Bandopadhyay and Mitra (2015).

Acceptor-like defects, including zinc vacancies (V_{Zn}) and oxygen interstitials (O_{i}), introduce deep levels within the bandgap and are typically associated with broad visible emission bands. Such defect centres can act as recombination centres under sub-bandgap excitation and have been linked to negative threshold shifts and hump-like behaviour during NBS Cabral et al. (2020). Moreover, extended Urbach-tail states near the band edges can be excited by low-energy photons, enabling sub-gap photoconductivity and metastable electrical responses under illumination Scolfaro et al. (2018).

More complicated defect configurations are also significant. According to density functional theory (DFT) calculations, oxygen vacancies are deep-seated double donors, and Zn interstitials and anti-site defects can be shallow donors, which together explain the challenge of obtaining p-type ZnO Vidya et al. (2011). Also, irradiation and disorder can cause more defect complexes to form that reduce the effective bandgap and increase photon conduction Han et al. (2024). Figure 7.1 shows the representative

energy-level diagram of ZnO intrinsic defects such as oxygen vacancies, zinc interstitials, zinc vacancies and oxygen interstitials along with optical excitation and trapping/de-trapping process of these defects. This diagram is a modification of Han Han et al. (2024), which highlights the role of sub-bandgap states in persistent photoconductivity, visible emission, and bias-stress-induced instability. Collectively, the above works show that ZnO and its intrinsic defect range plus disorder-related defect range are very sensitive to optical excitation and capable of responding significantly to its bias-stress behaviour. The irradiation-induced excitation in the near-surface had various types of defect states, and the defects led to the appeal of various electronic levels within the bandgap and to the electronic transitions between the various levels. The luminescence intensities related to the concentration of defect states were effectually encouraged, which indicated the surface defect states hinder excitons from being trapped, contriving the elevated possibility of exciton radiative transitions Han et al. (2024).

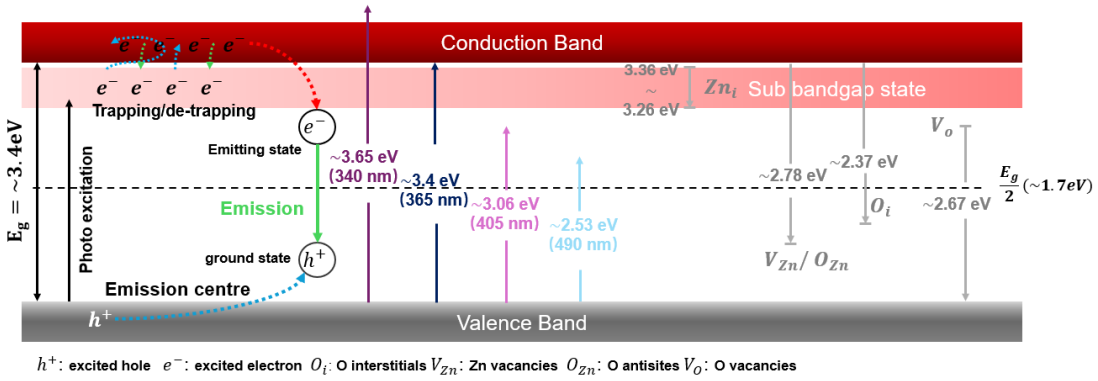


FIGURE 7.1: Schematic energy-band diagram of ZnO showing intrinsic defect states and their optical transitions. Shallow donor-like states (Zn_i) lie near the conduction band minimum (3.12 eV to 3.21 eV), whereas oxygen vacancies (V_O) are deeper donor-like states that can induce green luminescence and persistent photoconductivity. Zinc vacancies (V_{Zn}) and oxygen interstitials (O_i) generate deep acceptor states close to the valence band, giving rise to orange–red emissions and enhanced instability under NBS. The schematic also indicates sub-bandgap states and trapping/de-trapping processes that govern threshold voltage shifts under PBS/NBS. Adapted from Han Han et al. (2024).

Together, the above works demonstrate that ZnO with its intrinsic and disorder-induced defect spectrum is highly sensitive to optical excitation and it can respond substantially to its bias-stress behaviour.

Simultaneously, the dielectric layer and interface provide other routes of charge trapping and de-trapping. Figure 2.4, in **chapter 2**, shows that the ALD or PEALD deposited Al_2O_3 is associated with various kinds of intrinsic and extrinsic defects, such as oxygen vacancies (V_O), aluminium vacancies (V_{Al}), interstitials and unoccupied hydroxyl groups (-OH). Such defects do not only serve as charge trapping centres in the bulk oxide, but also affect the electrostatic environment at the interface between Al_2O_3/ZnO. Specifically, the presence of border traps due to oxygen vacancies may trap photo-generated carriers and cause long-term instability during PBS, and aluminium vacancies and interstitials add to fixed charges to change the flat-band condition. Meanwhile, hydroxyl groups, more common in low-temperature, Al_2O_3 can serve a dual purpose: hydrogen-related states can passivate states at the ZnO interface, yet excess -OH may create metastable centres that can be occupied by donors and increase threshold voltage changes during illumination Nam et al. (2016); Weber et al. (2011); Zhang et al. (2011).

Al_2O_3 prepared by the atomic layer deposition (ALD) or plasma-enhanced ALD contains oxygen vacancies which serve as border traps, trapping photo-generated electrons, and leading to long-term instability in PBS Weber et al. (2011). The presence of aluminium vacancies and interstitials also causes fixed charges, which shift the electrostatic potential at the ZnO/dielectric interface, and thus change the threshold voltage Zhang et al. (2018). Remaining hydrogen and hydroxyl groups (-OH), especially those that remain after low-temperature Al_2O_3 films, can have dual effects: on one hand, hydrogen incorporation has been shown to passivate interface defects and enhance device properties. On the other hand, excess hydroxyl (–OH) groups incorporated during low-temperature deposition have been suggested to introduce metastable defect states that can participate in photo-assisted charge trapping or detrapping processes under illumination Zhang et al. (2018); Nam et al. (2016). Rather than acting as direct donors, these hydrogen-related species may modify the local defect environment and influence the charge state dynamics of nearby traps. It has also been reported that higher hydrogen incorporation in low-temperature Al_2O_3 films can contribute to partial passivation of interface states at the ZnO/Al_2O_3 interface, potentially leading to improved transistor characteristics compared to films deposited at higher temperature Nam et al. (2016). However, the effectiveness of such passivation depends on the hydrogen configuration and stability, and may vary with deposition conditions.

The positive bias stress under conditions of positive bias captures photo-generated electrons by ZnO donor-like states as well as by Al_2O_3 border traps, resulting in a net positive shift of the threshold voltage. Acceptor-like defects in ZnO and positively charged centres at the ZnO/Al_2O_3 interface are triggered under negative bias stress, resulting in negative threshold shifts and, in certain instances, hump characteristics in the transfer characteristics Qi et al. (2017).
The relative abundance of these processes is directly dictated by the deposition temperature of Al_2O_3: low-temperature coatings have increased densities of hydroxyl-related and oxygen-related defects, which increase photon-assisted charge trapping, whereas high-temperature Al_2O_3 coats are more stoichiometric, and hence reduce the abundance of active traps. This renders the temperature of deposition of dielectric as a key parameter in the stability of optical PBS/NBS.

7.2.3 Optical Bias Stress in Oxide TFTs

The optical bias stress is the synergistic effect between light excitation and electrical bias and has been widely examined in oxide semiconductors. The optical stress due to bias is especially large in wide-bandgap oxides such as ZnO, where ultraviolet (UV) photons can easily populate defect states. In the case of amorphous IGZO, it has been reported that hump phenomena and large threshold shifts can be induced by illumination during NBS because of carrier diffusion and defect activation Zhang et al. (2025). Instabilities in ZnO TFTs are also found, but since the coupling of band-edge absorption to intrinsic oxygen-related defects is stronger, they are even easier to optical excitation Cabral et al. (2020). Especially, optical bias stress effects are sensitive to not just photon energy and intensity, but also dielectric quality and interfacial defect density, which highlights the need to optimize dielectric.

7.2.4 Role of Al_2O_3 Gate Dielectrics and Deposition Temperature

The popular dielectric in oxide TFTs is Al_2O_3 due to its moderate dielectric constant, good interface quality, and low leakage current. But, its electrical characteristics are sensitive to deposition conditions, particularly temperature. Investigations into ultra-thin ALD-grown Al_2O_3 films have shown that the density of defects, such as pinholes and oxygen vacancies, reduce in direct proportion to both better nucleation

and higher deposition temperature Zhang et al. (2011) . Native defect studies also indicate that oxygen vacancies in Al_2O_3 form gap states that serve as border traps, and that vacancies in aluminium and interstitials play a role in fixed charge and scattering centres Weber et al. (2011) . Also incorporating hydrogen in low-temperature growth can be advantageous, and it passivates defect states and enhances device performance, but too much hydrogen or -OH groups can also form metastable states activated in the presence of light Nam et al. (2016). Thus, the Al_2O_3 deposition temperature has a direct relationship with the equilibrium between the trap passivation and film densification, and, subsequently, optical bias stability of ZnO TFTs.

7.2.5 Research Gap

Although the fact that the bias stress instabilities, the ZnO defect physics and the dielectric properties have been researched extensively, there is no systematic knowledge regarding the influence of Al_2O_3 deposition temperature on the optical PBS/NBS stability of ZnO TFTs. Past studies have either been biased-illumination-stress device studies or material-level studies of ZnO or Al_2O_3 alone. Therefore, the interaction of deposition temperature, dielectric defect conditions, and optical excitation to ZnO TFT stability is not fully studied. The need to fill this gap is the main objective of this work, which reports the systematic investigation of ZnO TFTs with Al_2O_3 gate dielectrics deposited at various temperatures (150-300 $°C$) under controlled optical PBS and NBS conditions.

Overall, it has been shown that both channel defects and dielectric-related states are the main causes of bias stress instability in oxide TFTs. These instabilities are further enhanced by optical excitation which can activate intrinsic ZnO defects including oxygen vacancies, zinc interstitials, deep-level centres and interface states that Al_2O_3 brings. Deposition temperature of Al_2O_3 has been demonstrated to strongly affect dielectric quality and defect density, but its direct effect under optical PBS/NBS conditions in ZnO TFTs has not been systematically investigated. This gap demonstrates the necessity of a detailed study of how the temperature of dielectric deposition regulates the optical bias stress stability. The next section thus presents experimental methodology used in this work device fabrication, optical stress condition and measuring procedures to answer these open questions.

7.3 Experiment

Thin-film transistors (TFTs) were used in this study with the gate dielectrics of Al_2O_3 being deposited at 150, 200, 250 and 300 $°C$. The fabrication stages of the devices are described in the previous chapter. All devices utilized a bottom-gate format with a constant drain bias of 1 V in electrical measurements.

A semiconductor parameter analyser was used to carry out electrical characterizations. Drain current (I_D) was continuously monitored under various stresses. Dark transfer curves were also obtained to determine the performance in the dark before illumination tests were performed.

In optical bias stress experiments, the devices were lighted at the ZnO channel side and the Si substrate optically shaded. The main excitation wavelength was selected as a 365 nm LED source, which matches with the near-band-edge absorption of ZnO Han et al. (2024). Both positive and negative bias stress (PBS and NBS) were used at each Al_2O_3 deposition temperature with a total of 3600 s of continuous illumination and a gate voltage of ±10 V and ±5 V. I_D(t) and I_G(t) were measured during stress in order to trace the evolution with time.

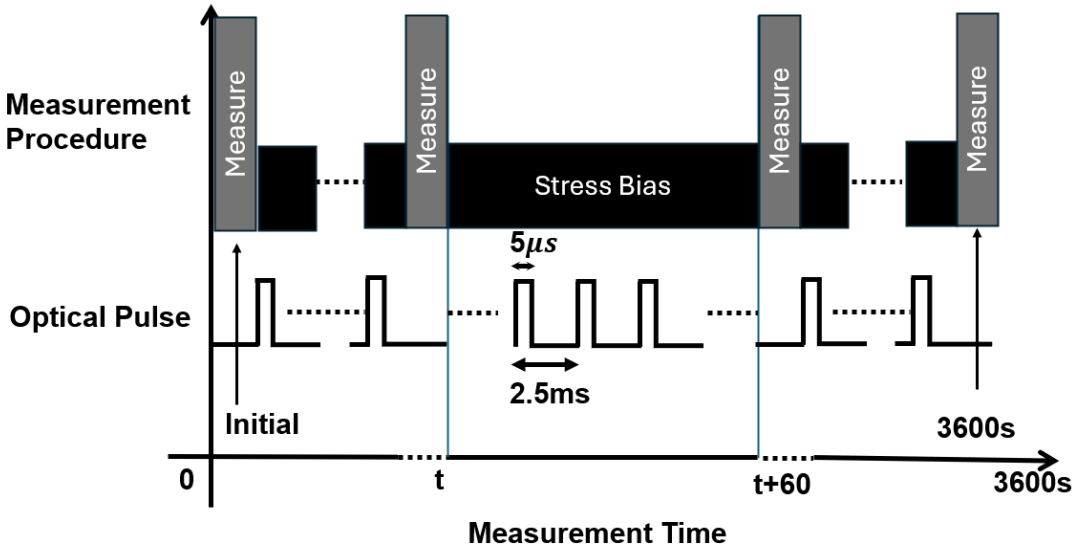


FIGURE 7.2: Measurement flow chart of optical bias stress experiments. A baseline transfer curve was obtained at t = 0 and then continuous stress bias was applied during the 3600 s under illumination. Measurements of transfers were re-measured after 60 s throughout the stress-test period, but drain currents were recorded continuously, allowing both transient and long-term drift behaviour to be studied.

Figure 7.2 shows the stress and measurement sequence. Measurements of the transfer were made initially at a point when there was no bias applied followed by the continuous application of the stress bias. Periodic measurement of transfer characteristics (after every 60 s) was then done throughout the 3600 s stress period, supplemented by continuous monitoring of I_D and I_G. The protocol enabled the rapid initial transients as well as slow long-term drift processes to be recorded with the same operating conditions. Besides shifting V_{th} and degrading μ_{FE}/SS, the applied bias stress also modifies the off-state leakage. Under PBS, the dominant response is typically a positive V_{th} shift, so the apparent I_{OFF} at a fixed negative V_{G} is often unchanged or slightly reduced. In contrast, NBS—particularly for the higher deposition temperatures tends to increase I_{OFF} (in some cases by around an order of magnitude), which is consistent with the pronounced subthreshold broadening and the emergence of an elevated leakage "tail" in the negative-V_{G} regime. This behaviour indicates that negative stress promotes the activation/charging of interfacial and near-interfacial trap states that weaken gate control in weak inversion and facilitate trap-assisted leakage.
In order to investigate the wavelength dependence, further measurements of the 150 $^{\circ}C$ devices under the light of 340, 405, and 490 nm were performed at the same biasing and stress period. For every new stress sequence, new devices were set up with the new conditions to start measurement.
The maximum transconductance method was used to extract threshold voltage (V_{TH}) and the shift ΔV_{TH} induced by the bias was determined relative to the dark base of the same device. Characteristics of gate current were also recorded to determine potential leakage-assisted degradation or charge injection contributions.
The 60 s measurement interval was picked as a stress period between the need to capture the rapid initial transients and the need to have stable long-term monitoring without excessively adding in measurement overhead. Smaller intervals would add more data but would expose the sample to extra heating and photo-excitation when scanning often, whereas longer intervals would not help to study the early-stage drift dynamics that are so important to the kinetics of trap filling. These rapid initial changes were observable by using a 60 s interval and a total stress time of 3600 s, which could have enabled reliable monitoring of the slow approach to quasi-saturation.
Figure 7.3 shows the scheme of the bias step measurement under 365 nm light and the resultant drain current response of ZnO TFTs with Al_2O_3 deposited at various temperatures (150-300 $^{\circ}C$). At stress, $V_{GS(stress)} = +10$ V, the periodic bias step will

cause current pulses to be overlaid on the steady-state drain current, which are the direct indication of the dynamic trapping and de-trapping processes caused by photoexcitation. The transient current spikes, as seen in the magnified plots of each of the devices, are always present in all the deposition conditions, yet the amplitude and the baseline level of the transient current spikes are highly dependent on the deposition temperature. Devices deposited at high temperatures (250-300 $°C$) have larger steady drain current values and devices deposited at a lower temperature (150-200 $°C$) have lower current levels. Current spikes under optical bias stress show that photo-generated carriers are repeatedly recombined and recreated by defect states, which is in agreement with the defect-related instability mechanisms as described in previous sections. The information about the LEDs (supplier, model no. etc.) has been provied in table 7.1.

TABLE 7.1: LED sources and measured fiber outputs.

Item	Color	Nominal wavelength	200 μm Core Fiber output	400 μm core fiber output
M340F4g	Deep UV	340 nm	0.16 mW	0.75 mW
M365FP1g	UV	365 nm	5.29 mW	15.5 mW
M405F3g	UV	405 nm	0.93 mW	3.7 mW
M490F4	Blue	490 nm	0.9 mW	2.8 mW

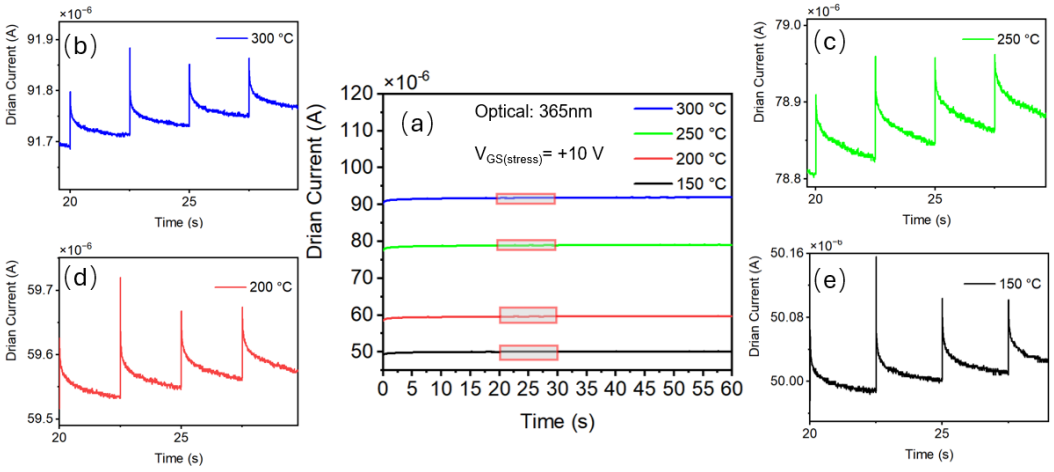


FIGURE 7.3: Bias step analysis and drain current response of ZnO TFTs under 365 nm light with $V_{GS(stress)} = +10$ V. (a) General drain current evolution of devices deposited at various temperatures (150-300 $°C$). Panels (b-e) indicate the magnified current spikes of each device temperature in transient. All devices show periodic current pulses caused by carrier trapping and de-trapping caused by steps in the stress bias, and the steady-state level of current density grows as the deposition temperature rises. The current magnitude emphasise that photo-assisted defect activation is temperature sensitive during optical bias stress.

7.4 Result & Analysis

7.4.1 Baseline Electrical Performance (Dark I-V)

The linear-scale transfer curves (Figure 7.4) show that the on-state drain current becomes strongly suppressed after 3600 s of bias stress, with the effect being stronger under positive bias stress (PBS) than negative bias stress (NBS). A moderate decrease is observed at 150 $°C$, which indicates some passivation of traps by hydrogen incorporated in the low-temperature Al_2O_3 films Nam et al. (2016). PBS shows the largest suppression at 200 $°C$, which correlates with the maximum mobility degradation ($\Delta\mu_{FE}$ = -3.1 $cm^2/(Vs)$), whereas NBS only attains a smaller degradation. As deposition temperature further increases to 250 and 300 $°C$, PBS-induced suppression is minimally weaker, whereas NBS-induced suppression is more pronounced, indicating an augmenting role of interfacial states.

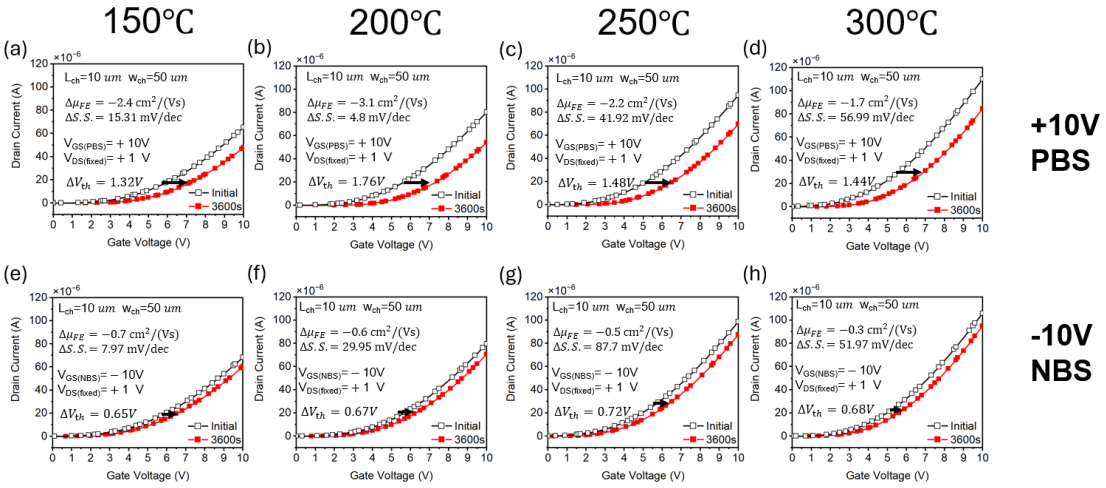


FIGURE 7.4: Linear-scale transfer characteristics of the same devices ($I_D - V_G$) under PBS and NBS. Post-stress suppression of the on-state current is greatly reduced, especially with PBS, where field-effect mobility decreases to as low as -3.1 $cm^2/(Vs)$ at 200 $°C$. Conversely, NBS causes a less extreme reduction ($\sim$ -0.7 $cm^2/(Vs)$), which is in line with its smaller $\Delta\mu FE$.

The logarithmic plots (Figure 7.5) give more information about the shift in threshold voltage and subthreshold slope (SS) degradation. With PBS, the transfer curves shift systematically as positive gate bias is increased with forward shifting (ΔV_{th}) in the range of 1.3-1.8 V. The highest ΔV_{th} is at 200 $°C$ (1.76 V) indicating that electron trapping in oxide-related defects is most effective at this intermediate deposition

temperature where hydrogen passivation is incomplete and oxygen-vacancy-related states are active Weber et al. (2011). Increasing temperature, the ΔV_{th} values fall a little and the SS degradation is significantly more pronounced, which implies that the trap-assisted tunneling and carrier scattering mechanisms are dominant in the films deposited at 250-300 $°C$. NBS, in contrast, causes smaller negative shifts ($\Delta V_{th} \approx$ 0.65-0.72 V), which are virtually temperature-independent but lead to large broadening of the subthreshold region at high deposition temperatures. The degradation of the SS is greatest at 250 $°C$ (+87.7 mV/dec), and is large at 300 $°C$ (+52.0 mV/dec), suggesting an enhanced density and charging activity of defect states in the ZnO/Al_2O_3 interfacial region, including (i) true interface states (D_{it}) located at or very near the ZnO surface/chemical interface (e.g., under-coordinated bonds and ZnO-related defect states), and (ii) near-interfacial oxide "border traps" within the first few nanometres of Al_2O_3 that can exchange charge with the channel via field-assisted tunnelling Bandopadhyay and Mitra (2015); Cabral et al. (2020). These observations are supported by the extracted parameter changes summarised in Table 7.2. PBS causes steadily greater ΔV_{th} ($\sim$ 1.5 V) and more severe mobility degradation than NBS, both at 200 $°C$. Maximum ΔV_{th} and maximum $\Delta \mu_{FE}$ at this temperature signify that the bulk Al_2O_3 charge trapping is most efficient in PBS. Conversely, NBS records nearly the same ΔV_{th} ($\sim$ 0.7 V) at all temperatures indicating that the negative stress instability is not restricted by bulk charge capture but by the generation of interface states. Here, the term "interface states" refers to electrically active states energetically coupled to the ZnO channel at the ZnO/Al_2O_3 boundary, whereas "border traps" denote oxide traps physically located inside Al_2O_3 near the interface. A fact that reinforces this is that the maximum ΔSS is observed at 250 $°C$, indicating that the interfacial defects dominate and that at 300 $°C$ ΔSS is still high in both PBS (+56.9 mV/dec) and NBS (+52.0 mV/dec), showing that films formed at high temperature have a higher concentration of the deep-level traps and un-passivated sites of defects Han et al. (2024); Vidya et al. (2011).

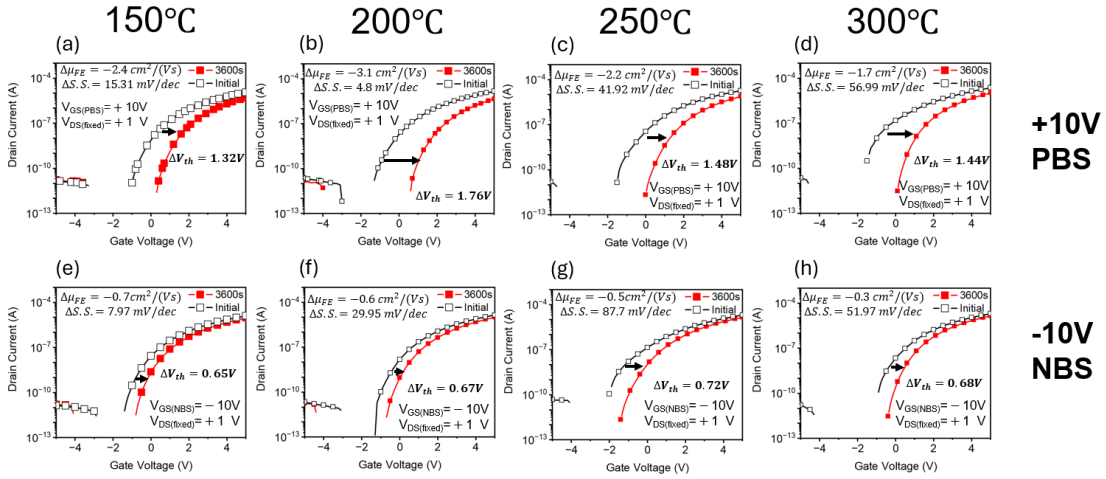


FIGURE 7.5: Transfer characteristics TFTs made of ZnO and Al_2O_3 gate dielectrics deposited at various temperatures (150-300 $°C$) in the dark (V_{DS}=1 V). The positive bias stress (PBS, +10 V) and the negative bias stress (NBS, -10 V) are related to panels (a-d) and (e-h), respectively.

In addition to the threshold voltage shift, a pronounced reduction in the OFF state current is observed after −10 V negative bias stress, with the drain current decreasing by approximately one order of magnitude across all Al_2O_3 deposition temperatures. This behaviour suggests that negative gate bias does not introduce additional leakage pathways in the ZnO channel. Instead, it suppresses residual conduction in the OFF state. Such suppression can be attributed to enhanced carrier depletion near the ZnO/Al_2O_3 interface and the possible deactivation or neutralization of donor like defect states under negative bias conditions. Unlike positive bias stress, which is typically associated with electron trapping and increased leakage, the observed OFF current reduction under NBS indicates a stabilizing effect on the channel electrostatics. This result highlights the asymmetric response of ZnO TFTs to positive and negative gate bias stress and suggests that negative bias operation may be beneficial for reducing standby leakage in low power applications.

TABLE 7.2: *Extracted changes in the parameters of ZnO TFTs (parameter changes: Δ V_{th}, Δμ_{FE}, and Δ$S.S.$) under PBS (+10 V) and NBS (-10 V) at various deposition temperatures (dark conditions V_{DS}1 V). PBS yields higher threshold voltage shift and mobility loss, and NBS results in worse SS degradation at higher deposition temperatures, especially at 250 °C.*

Temperature [$°C$]	ΔV_{th} **(V)**	$\Delta\mu_{FE}$ $(cm^2/(Vs))$	$\Delta S.S.$ (mV/dec)
PBS $(+10V)$ **@ Dark,** V_{DS} **=1 V**			
150	1.32	−2.4	+15.31
200	1.76	−3.1	+4.8
250	1.48	−2.2	+41.92
300	1.44	−1.7	+56.99
NBS $(-10V)$ **@ Dark,** V_{DS} **=1 V**			
150	0.65	−0.7	+7.97
200	0.67	−0.6	+29.95
250	0.72	−0.5	+87.7
300	0.68	−0.3	+51.97

Altogether, the joint study of the linear-scale suppression, log-scale shifts, and tabulated changes in parameters proves the fact that the PBS instability is majorly controlled by the electron trapping in the Al_2O_3-related defects, most intense at 200 $°C$, and the NBS instability by the generation of the interface states, which is most intense at 250-300 $°C$. This PBS-NBS asymmetry also demonstrates that there are varied microscopic sources of positive and negative bias instability and that a strong correlation exists between deposition temperature, defect chemistry, and electrical reliability.

Since the baseline instability condition under dark bias stress has already been established in which PBS is controlled by electron trapping in bulk Al_2O_3 and NBS by interface-state generation, it is necessary to further investigate the effects of external optical excitation on these processes. As photons with 365 nm energies are near the ZnO bandgap, direct light excitation can directly excite sub-gap defect levels and enhance carrier injection into the dielectric or interface traps Bandopadhyay and Mitra (2015); Han et al. (2024). Thus, optical bias stress response under 365 nm light is

examined in the next part to understand the interaction between photoexcitation and charge trapping caused by bias.

7.4.2 Optical Bias Stress Under 365 nm Illumination

Drawing on the dark stress measurements, in which PBS was observed to cause large positive threshold voltage shifts and mobility degradation and NBS primarily worsened the subthreshold swing at elevated deposition temperatures, it is worth studying how further photoexcitation affects such instability mechanisms. Excitation at 365 nm has photon energies similar to the ZnO bandgap, allowing the direct creation of electron-hole pairs and sub-gap activation. This does not only enhance the charge trapping in the Al_2O_3 dielectric and at the ZnO/Al_2O_3 interface but can also alter the occupancy of oxygen-related surface/near-surface defect states, which affects the surface electrostatics under illumination. Figures 7.6 and 7.7 show the linear- and logarithmic-scale transfer properties of PBS and NBS at 365 nm illumination, showing the interactive effect of electrical and optical stress on shifting threshold voltage, mobility degradation, and subthreshold response. The linear- and logarithmic-scale transfer properties of PBS (+10 V) and NBS (-10 V) of ZnO TFTs under 365 nm illumination following 3600 s of stress at various deposition temperatures are presented in Figures 7.6 and 7.7. The above-bandgap photons significantly increase charge trapping and defect activation in comparison with the dark case, resulting in larger shifts in the threshold voltages and stronger device-parameter degradation.
At 150 $°C$, PBS also causes a positive shift of ΔV_{th} = +1.18 V with mobility decreasing ($\Delta\mu_{FE}$ = -2.08 $cm^2/(Vs)$). On-state current in the linear plot is significantly suppressed, yet SS does not change much (almost +8.3 mV/dec). With NBS the negative shift is more pronounced (ΔV_{th} = -2.48 V), and the mobility is increased ($\Delta\mu_{FE}$ = +2.37) and the SS is somewhat improved (-9.99 mV/dec). This unexpected behaviour shows that at low deposition temperature, in excess of hydrogen and shallow defect states permit photoexcited carriers to fill traps, which partially cancels interface scattering Nam et al. (2016). PBS at 200 $°C$ yields a small positive shift (ΔV_{th} = +1.19 V) with degraded mobility (-2.5 $cm^2/(Vs)$) and SS marginally better (-13.4 mV/dec). Conversely, NBS has triggered a greater negative change (ΔV_{th} = -3.09 V), and better mobility (+2.99 $cm^2/(Vs)$) but also a considerable SS degradation (+732 mV/dec).

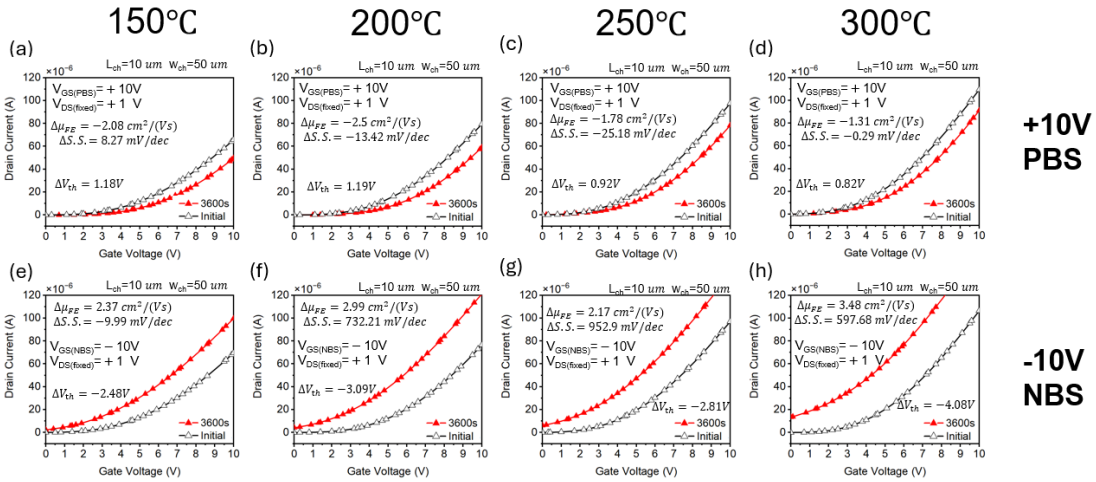


FIGURE 7.6: Linear-scale transfer characteristics of ZnO TFTs with Al_2O_3 gate dielectric deposited at various temperatures (150-300 $°C$) under a pre-test dark condition (V_{DS}=1 V) before and after 3600 s of bias stress (PBS, +10 V) and (e-h) after 3600 s of bias stress (NBS, -10 V).

It means that photoexcitation has a powerful effect on the negative bias instability at this intermediate deposition temperature when hydrogen passivation is weak and the oxygen-vacancy-related states are very active Bandopadhyay and Mitra (2015). At 250 $°C$, PBS exhibits a smaller positive shift (ΔV_{th} = +0.92 V) with a moderate loss of mobility (-1.78 $cm^2/(Vs)$) but significant SS increase (+25.2 mV/dec). Conversely, NBS causes a huge negative shift (ΔV_{th} = -2.81 V), an intermediate mobility increase (+2.17 $cm^2/(Vs)$), and a radical SS degradation (SS = +953 mV/dec). Here we evidently see that the instability under optical NBS stress is driven by interface traps, in agreement with the increased trap generation with higher deposition temperatures Cabral et al. (2020). PBS shows the smallest positive shift (ΔV_{th} = +0.82 V) at 300 $°C$ with slight loss of mobility (-1.31 $cm^2/(Vs)$) and almost constant SS (-0.3 mV/dec). Nevertheless, NBS generates the most significant negative shift (ΔV_{th} = -4.08 V), the greatest mobility increment (+3.48 $cm^2/(Vs)$), and the most significant SS degradation (+598 mV/dec). These findings show that deep oxygen-vacancy-related defects in Al_2O_3 and ZnO are highly activated by concomitant bias and illumination at high deposition temperature resulting in predominating negative stress instability Han et al. (2024); Vidya et al. (2011).The comparison based on deposition temperatures indicates that the instability mechanisms change in line with any interfacial chemistry derived by XPS and AFM. Hydrogen-containing Al_2O_3

at 150 °C offers good passivation Nam et al. (2016), and results in small values of the shift in V_{th} and slight SS variations at both PBS and NBS. The lowest hydrogen passivation and activated bulk oxide traps Nam et al. (2016); Bandopadhyay and Mitra (2015), at 200 °C, cause the most pronounced changes in the shifts in the V_{th} and the mobility under PBS whereas in NBS, the SS broadening is observed. High temperature (250 °C) oxygen-deficient bonding and surface roughness promote interfacial conditions Cabral et al. (2020), with NBS the most prevalent instability mechanism, particularly when the system is illuminated and SS degradation is disastrous at this temperature. Deep oxygen-vacancy-related defects are predominant at 300 °C Vidya et al. (2011); Han et al. (2024), leading to significantly increased SS at PBS and the greatest negative shifts of -V_{th} at NBS. These findings indicate that bias stress instability is highly temperature sensitive with a transition to hydrogen-limiting at low temperature, bulk-trap-controlling degradation at intermediate temperature, and finally interface- and oxygen-vacancy-driven degradation at high temperature.

Although the foregoing sections have determined the temperature-dependent instability mechanisms at dark and illuminated stress conditions at a constant gate bias of ± 10 V, the threshold voltage shift also varies with the magnitude of the applied stress. In order to further explain the dependence on bias, the next section compares the development of ΔV_{th} in the presence of stresses ± 10 V versus ± 5 V with PBS and NBS. This analysis highlights whether lowering the gate bias can effectively mitigate charge trapping and interface state activation across different deposition temperatures. In addition to the extracted shifts in ΔV_{th}, $\Delta \mu_{\mathrm{FE}}$ and ΔSS, the transfer characteristics under *dark* NBS show an apparent ∼one-order increase in the off-state current for the higher deposition temperatures (in our dataset, typically $\geq 200\,^{\circ}\mathrm{C}$), while such off-current boosting is not evident at 150 °C. This indicates that the off-current change under negative bias is not universal, but becomes prominent when the negative-stress condition induces pronounced *subthreshold broadening* and/or additional leakage contributions.

The elevated I_{OFF} is consistent with degraded electrostatic gate control associated with an enhanced effective trap response near the ZnO/Al_2O_3 interface (including interface and near-interface/border states), which can increase SS and broaden the subthreshold region. As a result, at a *fixed* negative gate voltage used to define the off-state (e.g., $V_{\mathrm{G}} = -10$ to -5 V), I_{D} decreases by fewer decades than in the initial state, leading to a visibly higher I_{OFF} on the log-scale transfer plot. In addition,

trap-assisted leakage in weak inversion may further contribute to an elevated current "tail" in the negative-V_G regime, amplifying the apparent off-current increase.

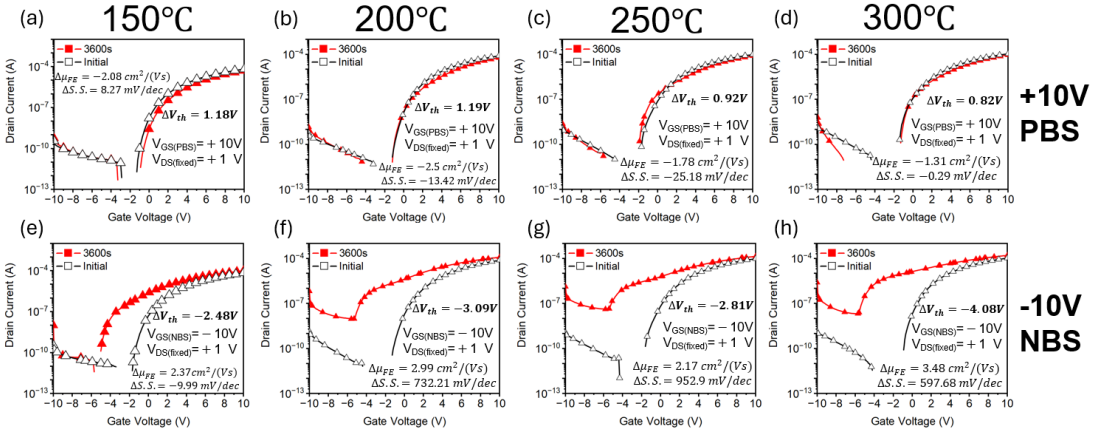


FIGURE 7.7: Transfer characteristics of the same devices in the same PBS and NBS conditions on a logarithmic scale (I_D–V_G). The log-scale plots contribute to illuminating the subthreshold area, in which the SS degradation is the most visible. PBS is characterised by systematic positive changes with moderate changes in SS whereas NBS, particularly at 250-300 $°C$, leads to extreme subthreshold broadening and off-state current boosting.

The lack of a pronounced I_{OFF} boost at 150 °C agrees with the comparatively small change in ΔSS under dark NBS, suggesting that subthreshold broadening and leakage enhancement are limited in this case. By contrast, at higher deposition temperatures the larger ΔSS implies a stronger involvement of deep-level and/or un-passivated near-interface defects under negative bias, which correlates with a marked loss of gate controllability and an increased I_{OFF}.

7.4.3 Comparison of Stress Voltage ($\pm 10V$ Vs. $\pm 5V$)

As it was previously presented, the extent of bias stress instability is highly sensitive to the deposition temperature and to the stress polarity. It is also required to consider the degradation process with regard to the magnitude of the applied gate bias. Figures 7.8 (a-d) represent the ΔV_{th} change with the influence of ±10 V and ±5 V stress, and under dark conditions. Figures 7.8 (e-h) represent the results of ΔV_{th} under the influence of 365 nm light. It is possible to explain the effects of stress amplitude on electron trapping and interface state activation by comparing the shifts in the threshold voltage at ±10 V and ±5 V over the four deposition temperatures, with and without

PBS/NBS. There is also a practical view of this analysis concerning whether the stress bias reduction can be effective in reducing the instability of ZnO/Al_2O_3 TFTs.
Figure 7.8 contrasts the development of ΔV_{th} at ±10 V and ±5 V bias stress at 150-300 °C, dark and 365 nm illuminated conditions, in devices deposited at 150-300 °C. Only under dark stress can we observe small ΔV_{th} at 150 °C, which is consistent with the stabilizing effect of hydrogen-related passivation observed by XPS Nam et al. (2016). With illumination, though, the difference between ±10 V and ±5 V is clear: PBS at +10 V causes stronger positive shifts, and NBS at -10 V causes a significantly larger negative shift than at -5 V, indicating photo-assisted activation of the shallow traps Scolfaro et al. (2018). The dependence on the bias is stronger at 200 °C. In dark PBS, ΔV_{th} in response to +10 V stress is larger than that to +5 V, but NBS is essentially bias-independent. NBS at -10 V shows rapid and substantial negative shifts under illumination, whereas -5 V shows less, suggesting that photoexcitation activates reduced hydrogen passivation and oxygen-vacancy-related states at this intermediate temperature Nam et al. (2016); Bandopadhyay and Mitra (2015). The difference between ±10 V and ±5 V is dramatic at 250 °C, especially in the presence of illuminated NBS, where ΔV_{th} at -10 V is much larger than that at -5 V. This is in line with the XPS evidence of increased oxygen-deficient bonding Bandopadhyay and Mitra (2015) and AFM findings of heightened surface roughness, which facilitates interface-state formation under negative bias Cabral et al. (2020). At 300 °C, again a bias dependence is observed: PBS exhibits moderate scaling of ΔV_{th} with stress voltage whereas NBS operated under illumination is catastrophically unstable, with ΔV_{th} approaching -4 V at -10 V stress. This is associated with the existence of rich deep oxygen-vacancy-related defects in high-temperature Al_2O_3 Vidya et al. (2011); Han et al. (2024) . In general, the reduction of ΔV_{th} shifts in the ±10 V to ±5 V gate stress is effective at all temperatures, though it becomes especially important in illuminated NBS where interface states and deep defect activation are predominant.
Even at pm10 V stress at 150 °C, the ΔV_{th} is small, since hydrogen-rich Al_2O_3 saturates many interfacial traps. PBS PBS Under PBS, electrons at the ZnO/Al_2O_3 interface are captured with a weak force, and under NBS, the depletion region grows and the majority of the interface states remain inactive Nam et al. (2016). PBS instability prevails at temperatures above 200 °C: the positive bias across the ZnO channel causes a large influx of electrons into the gate dielectric, where they become trapped at unpassivated oxygen sites, resulting in a high positive ΔV_{th} and loss of

mobility Nam et al. (2016); Scolfaro et al. (2018). In NBS the negative bias drains the electrons out of the interface, exposing unpassivated states but with a moderate effect. The instability mechanism changes at 250 $°C$. PBS continues to inject electrons into bulk traps, but with NBS the negative bias shifts the ZnO bands upwards, causing the holes generated by photoexcitation to concentrate at the interface at the expense of electrons. This increases interface state charging and charging of oxygen-related border traps, resulting in catastrophic SS broadening Scolfaro et al. (2018); Castillo-Saenz et al. (2022b). At 300 $°C$, both PBS and NBS are harsh: in PBS, the strong accumulation forces the electrons deep into oxygen-vacancy-related traps in Al_2O_3, whereas in NBS, deep interfacial defects are excited and recapture/release carriers repeatedly. This gives the highest ΔV_{th} ($\sim$ -4 V) and shows that deep oxygen-vacancy-related defects Vidya et al. (2011); Han et al. (2024) dominate high-temperature films.

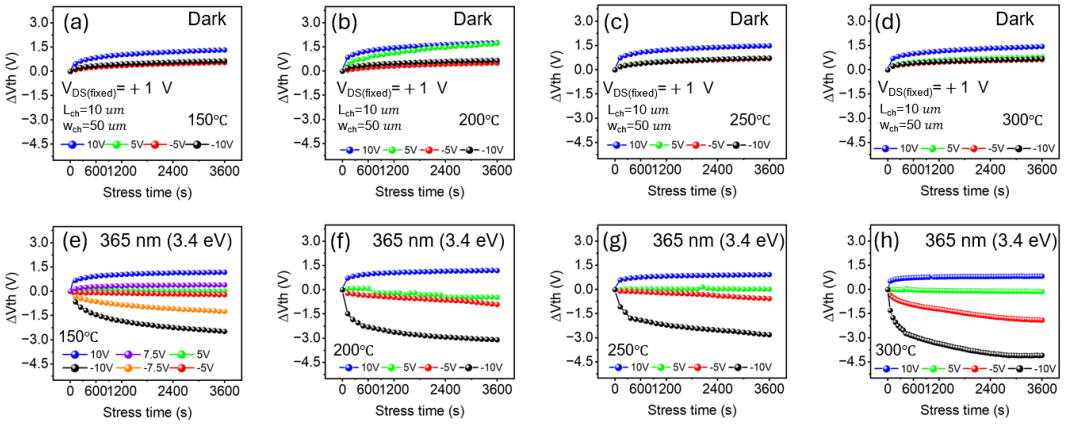


FIGURE 7.8: Variation in threshold voltage shift (ΔV_{th}) with stress time at various stress voltages ($\pm$10 V vs $\pm$5 V) of ZnO TFTs with Al_2O_3 deposited at 150-300 $°C$. Panels (a-d) indicate dark conditions and (e-h) depict 365 nm illumination. Larger positive ΔV_{th} can be observed appears at +10 V than at +5 V, especially at 200 $°C$. In NBS (-V_{GS}) the disparity between -10 V and -5 V is most notable under illumination at 250-300 $°C$, with negative ΔV_{th} shifts being worse at -10 V.

PBS injects ZnO moderately into the Al_2O_3 dielectric in the dark state, and NBS injects primarily channel charge without strongly activating interface traps. Photoexcited pairs of electrons and holes improve injection and interface charging under 365 nm light, however. Photoexcited electrons can now be trapped by shallow defects previously hydrogen-passivated at temperatures as high as 150 $°C$ Nam et al.

(2016). At 200 °C, PBS causes these other carriers to be injected into bulk Al_2O_3 traps, enhancing ΔV_{th}. With a temperature of 250 °C and the light of NBS, holes are formed at the interface and the photoexcited electrons are eliminated on the channel, significantly increasing the occupation of the interface traps and causing catastrophic SS broadening. Deep oxygen-vacancy-related states at the dielectric and interface are the efficient recombination and trapping sites at 300 °C, and illumination promotes the charging of these states, resulting in the largest negative ΔV_{th} ($\sim$ -4 V) under NBS. Combined, the dark and light bias stress result comparisons are direct electrical proof that supports the defect evolution observed by XPS and AFM. XPS at 150 °C exhibited high hydroxyl and hydrogen content and AFM verified the smoothest surface ($R_q < 1$ nm), which indicates effective passivation of interface states. In this regard, electrical measurements indicated the smallest changes in V_{th} and almost constant SS and μ_{FE}, which is consistent with the literature that hydrogen incorporation inhibits trap activity in ALD Al_2O_3 Nam et al. (2016). At 200 °C, XPS showed a decrease in hydrogen-related bonds and AFM showed an abrupt rise in surface roughness, both indicating the formation of unpassivated bulk oxide traps. Regularly, PBS generated the most beneficial V_{th} shifts and the strongest mobility loss, and this demonstrates that electron trapping in Al_2O_3 was the dominant process as already linked with oxygen-vacancy-related states Weber et al. (2011) . At 250 °C, XPS revealed oxygen-deficient bonding and AFM revealed local protrusions, indicating an increase in interfacial disorder. At the same time, NBS at dark and optical stress induced catastrophic SS broadening, confirming that interface-state charging predominated the instability, which is consistent with the optical activation of ZnO sub-gap and interface defect states Scolfaro et al. (2018); Castillo-Saenz et al. (2022b). The XPS evidenced strong oxygen vacancy features at 300 °C and the surfaces appeared rough and textured via AFM, suggesting the presence of deep defect states. This was consistent with the electrical measurements, in which PBS resulted in catastrophic SS degradation and NBS giving the largest negative V_{th} shifts, as DFT and irradiation experiments have found deep-level oxygen vacancies to be the primary centres of instability Vidya et al. (2011); Han et al. (2024).

In this way, the spectroscopic and morphological data are directly confirmed by the electrical bias stress response over 150-300 °C: low temperature hydrogen passivation inhibits instabilities, whereas high temperature reduced hydrogen, enhanced roughness,

and oxygen-vacancy-related defects promote charge trapping and interface-state processes, culminating in larger SS, worse mobility, and more exalted V_{th} shifts.

7.4.4 Wavelength Dependence (150 $^{\circ}C$ devices)

Since the temperature-dependent instability mechanisms have been established under dark and 365 nm illumination, it is also of interest to examine the influence of photon energy by changing the illumination wavelength. Because photon absorption is a direct measure of how many electron-hole pairs can be generated and the activation of sub-gap states in ZnO and Al_2O_3, measurements of bias stress at various excitation wavelengths can give further information on how optical energy can be used to control the dynamics of charge trapping and interface-state processes. In this part, we concentrate on devices deposited at 150 $^{\circ}C$, where the baseline instabilities were least, so that the wavelength-dependent contributions to ΔV_{th} under PBS and NBS can be clearly resolved.

It is necessary to add that the drive current regulated the LED excitation intensity. Early experiments on 6 mA and 10 mA drive current showed that the larger drive current causes more significant changes in the transfer characteristics following stress and this result validates the instability being sensitive to illumination intensity. As shown in figure 7.9, by comparing the transfer properties of ZnO TFTs,that have 150 $^{\circ}C$ deposited Al_2O_3, prior to and following 3600 s of optical bias stress during 365 nm illumination with two LED drive currents. An evident positive shift in the threshold voltage is seen following stress and the amplitude of the shift improves with the increase of drive current from 6 mA to 10 mA. This effect means that enhanced optical excitation produces an increasing photo-carrier concentration that gets sequestered in interface or dielectric defect locations, increasing the bias stress instability.

Remarkably, the linear-scale inset validates that current in the on-state does not decrease significantly meaning that the primary degradation process is the shift in threshold voltage but not the decrease of channel current.

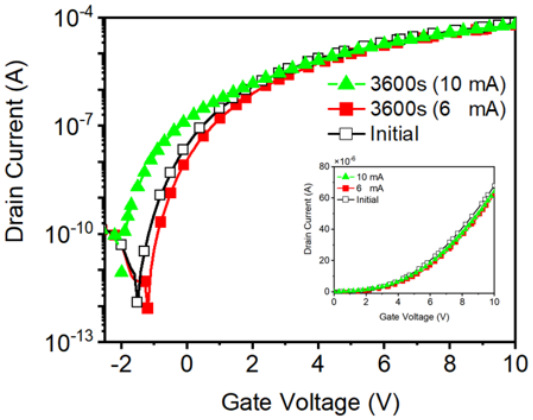


FIGURE 7.9: Transfer properties of a ZnO TFT with Al_2O_3 gate dielectric deposited at 150 $°C$, as measured prior to stress (black squares) and following 3600 s optical bias stress at various LED drive currents (6 mA, red squares; 10 mA, green triangles). The positive change of the threshold voltage shift, herein denoted as (ΔV_{th}), increases as the drive current increases, implying that greater optical excitation produces more carriers that are trapped at the interface or dielectric defect locations. The inset demonstrates the curves of the linear-scale ID-VG, which proves that the on-current does not change significantly, whereas the primary degradation takes place in the threshold region.

To achieve consistency, all measurements in this study involving wavelength-dependent measurements were thus performed at a constant drive current of 10 mA. This value was selected as a trade-off: it is high enough to provide stable excitation of all LEDs and to clearly measure processes related to defects, but not so high that it would cause excessive carrier densities and thus abnormal heating or irreversible device breakdown. The experimental setup could not allow direct calibration of the optical power of each LED. The relative photon-energy effects are thus seen as the main basis of comparison of the various wavelengths, as opposed to absolute optical intensity. The method enables us to decouple the wavelength effect on the charge trapping and interface-state dynamics and the results are also reliable and not due to over-stress.

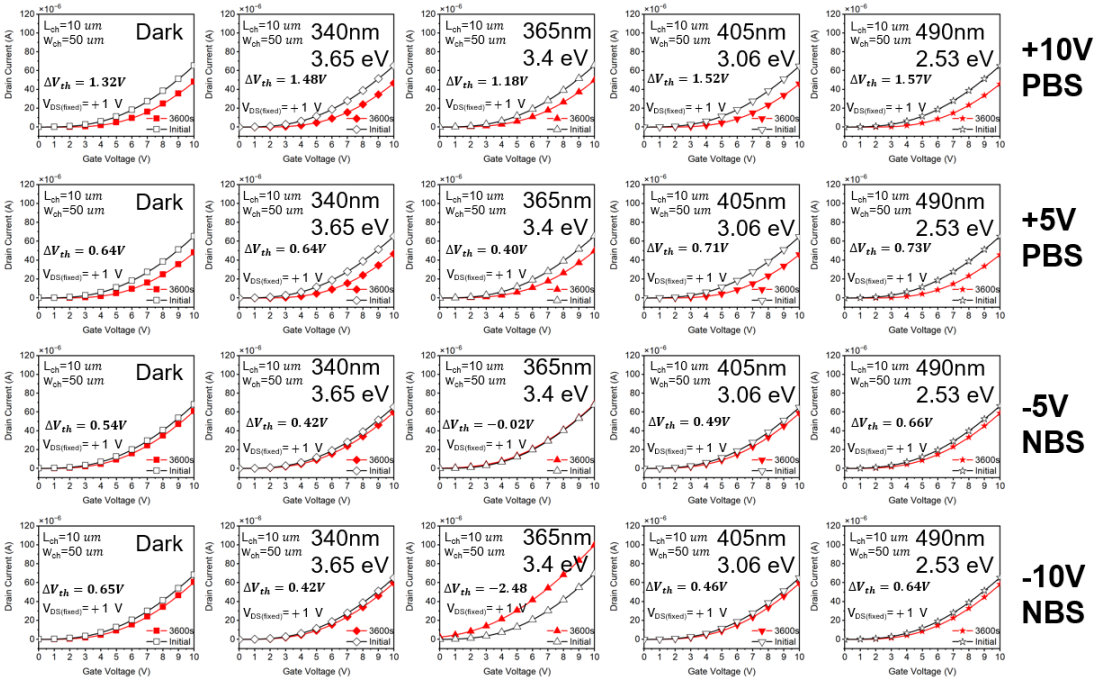


FIGURE 7.10: Linear-scale transfer characteristics ($I_D - V_G$) of 150 °C ZnO TFTs at the start of 3600 s bias stress under dark and optical illumination of varying wavelengths (340, 365, 405, 490 nm, constant LED drive current of 10 mA). Stresses of positive-bias (PBS, + 5 V and +10 V) and negative-bias (NBS, - 5 V and -10 V) are compared. Illumination causes further shifts of thresholds in comparison to dark - PBS has positive values of the photo-assisted electron trapping as expected, NBS has negative values of photo-assisted electron trapping, and subthreshold broadening as evidence of interface/border-trap charging.

Figures 7.10 and 7.11 provide the optical bias stress dependence on wavelength of ZnO TFTs produced with Al_2O_3 gate dielectrics deposited at various temperatures. In PBS, it is observed that devices have an apparent positive shift of V_{th}, and the magnitude of the change in V_{th}, or delta V_{th}, reduces with increasing excitation wavelength (between 340 nm and 490 nm). A comparable but reversed effect is seen under NBS, where negative gate bias and shorter-wavelength illumination lead to more dramatic shifts in V_{th}. These results are in agreement with the photoexcitation of defect states in ZnO and at the ZnO/Al_2O_3 interface: lower wavelengths, nearer or energetically higher to the ZnO band edge (3.3 eV), create more electron-hole pairs, contributing to carrier trapping of dielectric-related and interface-related defect states Scolfaro et al. (2018); Castillo-Saenz et al. (2022b).

It is necessary to note that all the sources of LEDs were operated at the same nominal current (10 mA). Although this guarantees the same operating conditions in the stress experiments, the actual incident optical power was not calibrated, which entails an

inherent uncertainty in the cross-wavelength comparison. Accordingly, the horizontal comparison of the various wavelengths mainly offers qualitative information between different Al_2O_3 deposition temperatures. However, the monotonic decrease in observed threshold voltage shift (the delta V_{th}) with wavelength is a strong indication that sub-gap states and near-band-edge transitions are critical in bias stress instability during optical excitation.

In general, the findings point to the fact that UV light increases instabilities caused by bias-stress by trapping carriers on oxygen vacancies, zinc interstitials, and Al_2O_3-related defects. The interdependence between deposition temperature and photoactive defect density, already indicated by XPS and AFM analyses, is once again supported in this work: lower-temperature films (150-200 $°C$) with increased hydroxyl-related surface disorder have stronger responses to the presence of oxygen vacancies in the form of traps, whereas higher-temperature films (250-300 $°C$) have lesser but still significant responses.

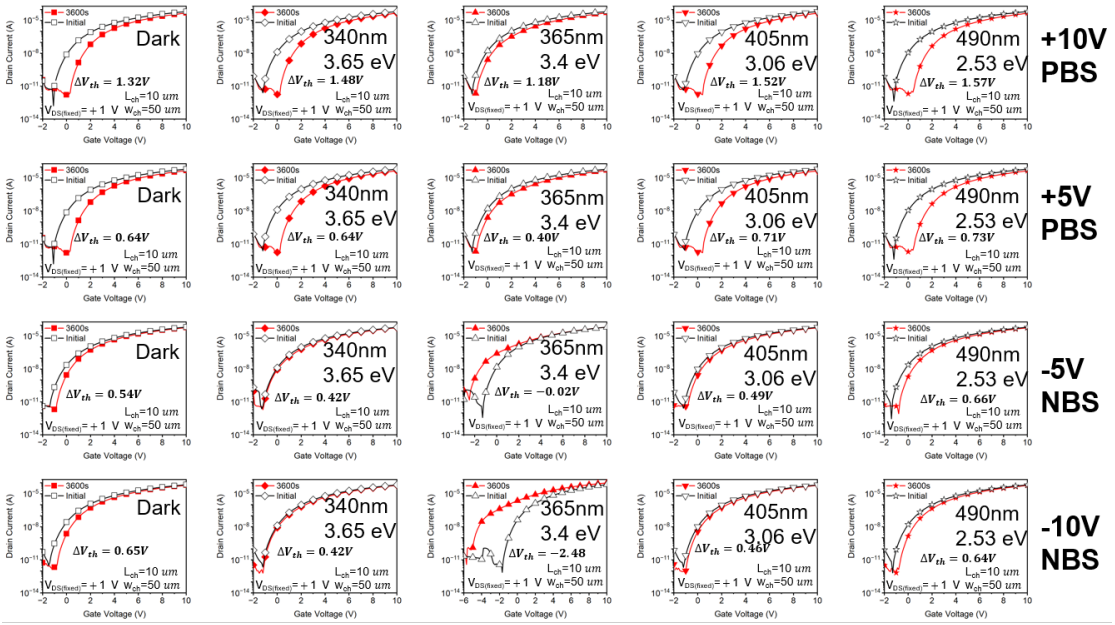


FIGURE 7.11: Transfer characteristics on a log scale of the same devices and conditions as Figure 7.10. The logarithmic perspective emphasises that the illumination increases the subthreshold region, particularly under NBS, which agrees with the activation of interface and sub-gap defect states. The shorter wavelengths around the bandgap (340/365 nm) and below the bandgap wavelengths (405/490 nm) are both sources of instability (band-to-band generation vs. defect-state absorption).

7.4.5 Mechanism Discussion

The joint electrical and material description of last chapter and this chapter enables the development of a detailed trap dynamics model of Al_2O_3/ZnO TFTs under the stress of bias. The charge-trapping processes in dark and illuminated conditions of PBS/NBS are schematically outlined in figures 7.12,7.13,7.14 and are further correlated with temperature-dependent defect chemistry indicated by XPS, AFM, and C-V studies. The combined method allows detection of the sources of defects at various deposition temperatures and the influence on threshold voltage stability, subthreshold swing (SS), and carrier mobility.

7.4.5.1 Dark Bias Stress Dynamics

Figure 7.12 (a) shows that in PBS the downward bending of the ZnO conduction band pushes the electrons towards the Al_2O_3/ZnO interface. Oxide receives these electrons and the interfacial traps (Q_{ot}, $Q_{ZnO,t}$) and an overall negative charge is accumulated in the dielectric. This effect minimizes the effective gate bias, resulting in a positive ΔV_{th}. This behaviour is confirmed by the I-V data in which ΔV_{th} is steadily on the rise with stress time in the case of dark conditions of PBS with moderate loss in mobility and SS. The steepness of the shift is saturated at 200 $^{\circ}C$ deposition, in line with the XPS evidence of slower hydrogen passivation and the appearance of bulk oxygen-vacancy traps.

Conversely, figure 7.12 (b) shows that NBS causes the bending of the bands upward, and in theory this band should induce electron detrapping. But in our devices with p-type Si gates, the majority carriers are holes, not the electrons, which accumulate at the interface between the gate and oxide, and make the electrostatic compensation restricted. As a result, the detrapping out of deep traps is inhibited very strongly and ΔV_{th} does not change by much under dark NBS. This point is consistent with the fact that there is no strong SS variation in dark NBS, where deep traps should be thermally or optimally optically activated in order to be effectively trapped.

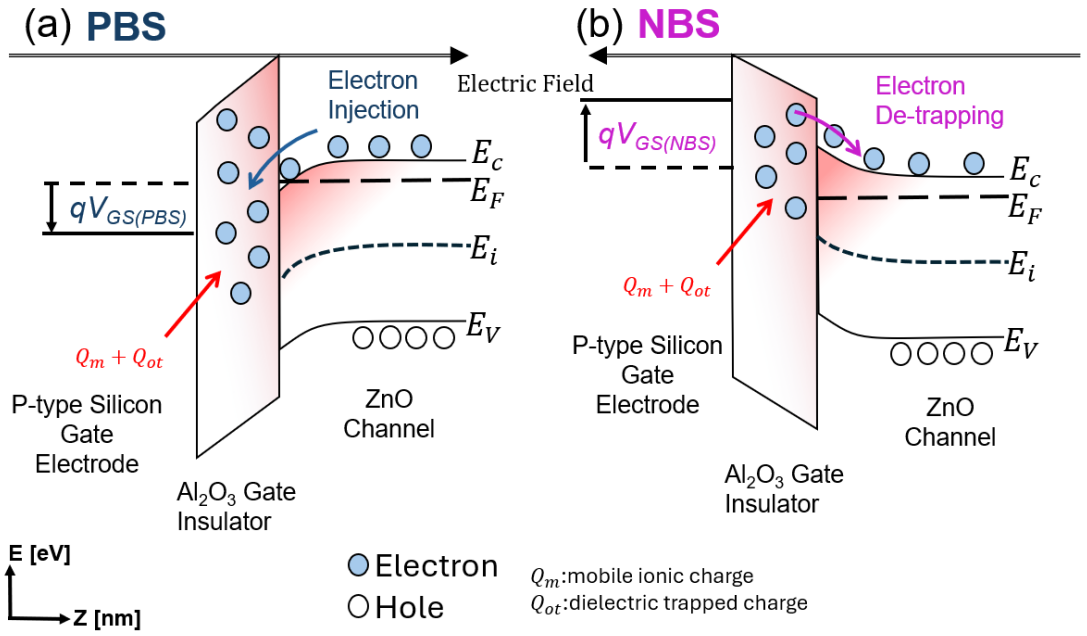


FIGURE 7.12: Band diagram illustration of the dynamics of bias stress during the dark environment. With positive bias stress (PBS), the ZnO conduction band folds downwards, causing the electrons to move towards the Al_2O_3/ZnO interface and a trapping of the electrons in the oxide or interfacial states (Q_{ot}, $Q_{ZnO,t}$, resulting in a positive change in threshold voltage ($\Delta V_{th} > 0$). Conversely, with negative bias stress (NBS) the band bends upwards. Nevertheless, the supply of holes out of the p-type Si gate is limited, and the oxide traps are deep, hence, detrapping is highly suppressed and causes ΔV_{th} to be negligible.

7.4.5.2 Light-Assisted Dynamics of Stress on Bias

Figure 7.13 (a) shows the dynamics in 365 nm illumination. Photon absorption is both a ZnO bandgap electron-hole pair exciter and a sub-gap oxygen vacancies (V_O), zinc interstitials (Zn_i), and oxygen interstitials (O_i) exciter Scolfaro et al. (2018); Vidya et al. (2011). The electrons generated by the photo generation are concentrated quickly in the interface, which increases the trapping at first and leads to a rapid positive ΔV_{th}. Continuous illumination is also capable of promoting the process of photo-assisted detrapping of oxide traps, making the injection process balanced. As the figure 7.14 (a-d) shows, device B is measured under the PBS stress for 3600s. Due to the light excited detrapping process, the final threshold voltage is shifted to negative due to more electrons being excited into the conduction band. Consequently, the experimental ΔV_{th} under light PBS (figure 7.14 (e-f)) reaches a lower level of maximum ΔV_{th} shift than under dark PBS, which means the trap-detrapping equilibrium is

established. The effect on SS is small, implying that the main effect of photo-excited carriers is to cycle between shallow and mid-gap traps without causing a deep interface disorder to develop.

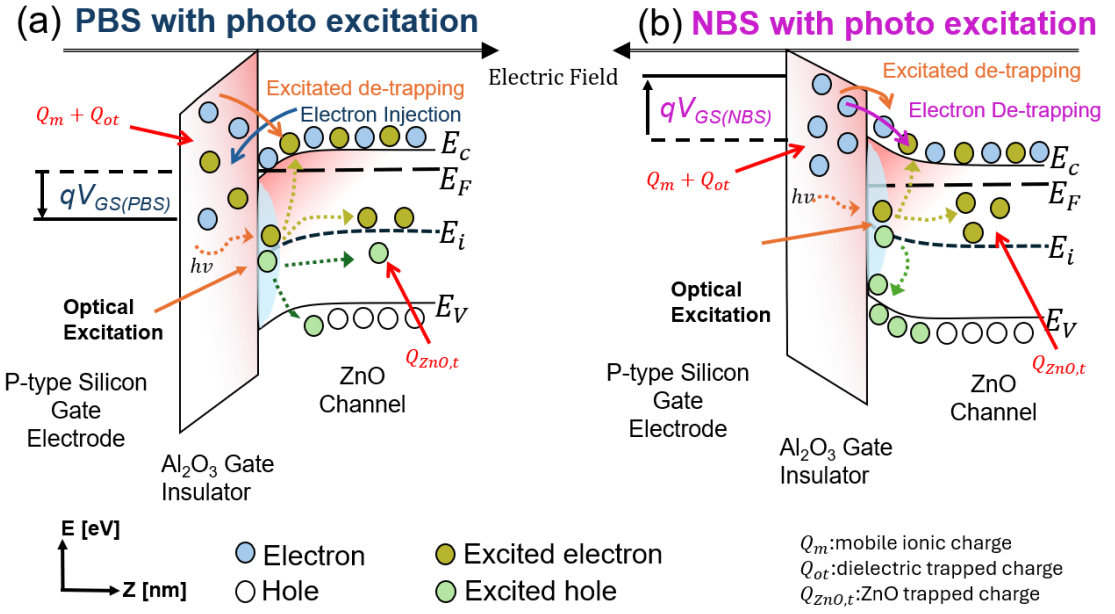


FIGURE 7.13: Band diagram illustration of light-assisted bias stress dynamics. Light of 365 nm photons is used to excite electron-hole pairs in ZnO, where electrons are excited to the conduction band out of the valence band. (a) For PBS, although a portion of the electrons are injected into oxide traps, others stay free in the channel. At the same time, light can also induce sub-gap defects where in the ZnO (oxygen vacancies, Zn interstitials), which increases trapping and detrapping dynamics. Consequently, photo-assisted PBS exhibits a positive ΔV_{th}, which levels off at the start of the electron injection process, after which the trap-detrapping processes stabilise at a dynamic equilibrium. (b) For NBS, the holes created by the photo-generated holes are concentrated at the interface of the Al_2O_3/ZnO, and the holes enable the electron detrapping of the oxide traps, and a strong negative ΔV_{th} shift is observed.

In illumination with negative bias (figure 7.13 (b)) photo-generated holes move towards the Al_2O_3/ZnO metal-oxygen interfaces, and electrons fill the conduction band. This twofold action facilitates electron detrapping of oxide traps and recombination routes. The overall effect is the strong negative ΔV_{th} shift, experimentally realized. At the same time, the growth in the number of holes in interfacial defects causes serious SS broadening, which is in line with the existence of oxygen-vacancy-associated deep states that have the capability to trap holes Castillo-Saenz et al. (2022b). The increase in the negative ΔV_{th} with time during the whole stress time of 3600 s is evidence that light provides carriers to maintain the detrapping such that equilibrium is not established.

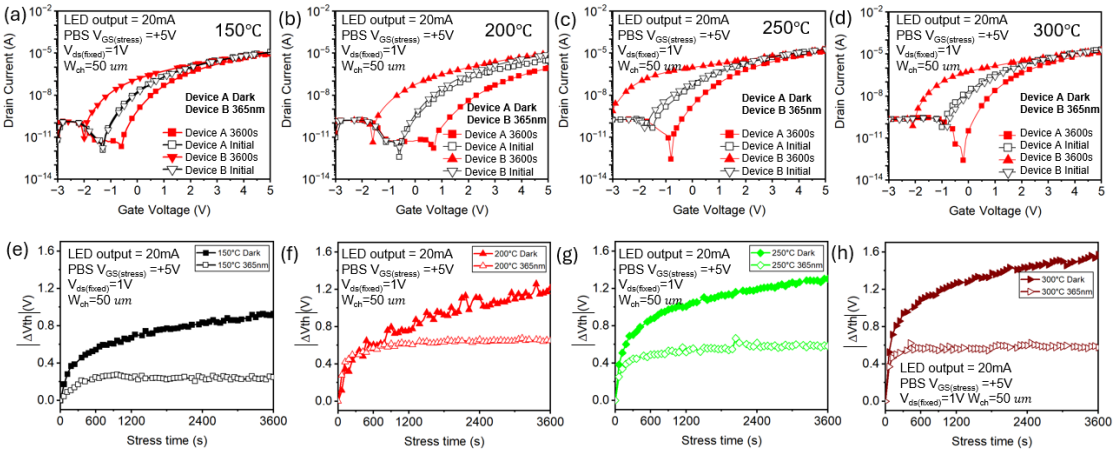


FIGURE 7.14: Bias stress dynamics in ZnO-TFTs are experimentally verified with Al_2O_3 as gate dielectrics. Exploratory results of threshold voltage shift (ΔV_{th}) under conditions of positive bias stress (PBS, V_{GS}= +5 V, 3600 s) in the context of ZnO-TFTs and Al_2O_3 gate dielectrics. ΔV_{th} exhibits a gradual positive drift in the dark where the electrons are injected into the oxide and interface traps, and the shift is nearly saturated with the trap states filled and additional injection prevented by field screening. ΔV_{th} 365 nm positive shift in the first stage of accelerated electron generation and injection but rapidly levels off due to photo-assisted trapping/de-trapping dynamics and equilibrium, which results in a smaller ΔV_{th} shift than in the dark after 3600s stress bias.

7.4.5.3 Temperature Dependent Defect Origins

Comparing the devices that are produced under different temperatures of Al_2O_3 deposition, it is possible to isolate the dominant defect mechanisms. 150 $°C$ (Hydroxyl-rich regime): XPS indicated a large amount of surface hydroxyl and AFM presented smooth morphology. These properties add to efficient hydrogen passivation of ZnO interface states. As a result, devices undergo little ΔV_{th} drift within PBS/NBS and are more mobile with slim SS. Nevertheless, even very shallow traps can be optically triggered under illumination, and cause moderate instability. 200 $°C$ (Bulk-trap regime): Hydrogen-related defects are to a large extent eliminated at this temperature and the onset of oxygen deficiency is to be observed. O/Al ratio becomes lower, and the roughness of AFM becomes more prominent. The worst PBS-induced ΔV_{th} and mobility degradation is observed in the electrical response, which demonstrates that bulk oxide traps tend to dominate the instability. 250-300 $°C$ (Oxygen-vacancy/Interface-trap regime): Films become denser and Al-rich, with XPS showing stronger low-binding-energy $O1s$ components attributed to oxygen deficiency.

AFM reveals roughened surfaces with protrusions, consistent with enhanced interface disorder. These conditions favour interface trap formation, which strongly impacts NBS (ΔV_{th} negative shifts and SS broadening). Under illumination, Negative Bias Illumination Stress (NBIS) effects are particularly pronounced, as oxygen vacancies act as hole-trapping centres that destabilize the subthreshold region.

7.4.5.4 Unified Mechanism

The combined picture is that PBS instability is dominated by electron injection into bulk oxide traps, while NBS instability is governed by interfacial oxygen-related traps and light-assisted detrapping processes. The relative severity of each instability depends on the deposition temperature of Al_2O_3, which determines the balance between hydrogen passivation, oxygen vacancy density, and interface disorder. Mobility degradation is most closely tied to bulk trap-assisted scattering (200 $°C$), while SS broadening reflects interface trap activation (250-300 $°C$). These findings are consistent with prior literature on oxide semiconductor TFT instabilities, including reports of NBIS in IGZO TFTs Nomura et al. (2004); Scolfaro et al. (2018); Castillo-Saenz et al. (2022a). Importantly, they demonstrate that careful control of deposition temperature can suppress instability mechanisms, and our results show 150 $°C$ offering optimal hydrogen passivation and 250-300 $°C$ prone to oxygen-vacancy-dominated degradation.

7.4.6 Summary

A detailed mechanism explanation was developed in this chapter to justify the bias stress instabilities of ZnO TFTs when PEALD Al_2O_3 dielectrics were deposited at different temperatures (150-300 $°C$). Through integrated I-V transfer, PBS/NBS stress measurements at dark and illuminated, and material characterizations were undertaken in *Chapter 6* (XPS, AFM, C-V), a global tapestry of trap-dynamics has been built. Electron injection into Al_2O_3 bulk and interfacial traps (Q_{to}, $Q_{ZnO,t}$) is the most significant during dark PBS, with a positive ΔV_{th}. The transition point is the clearest in the devices produced at 200 $°C$, with both XPS and AFM showing reduced hydrogen passivation and increased surface roughness, respectively, that are favorable to better electron entrapment. In comparison, dark NBS exhibited very little ΔV_{th}, due to no electron compensation at the p-Si gate and limited thermal activation of

deep traps, indicating a strong suppression of detrapping kinetics in the absence of external excitation.

As there was light (365 nm) the dynamics of bias stress significantly changed. In illuminated PBS, electron-hole pairs that were generated by photo-generation enhanced the constant rate of injection, which created a rapid change in ΔV_{th}. None-the-less, constant photon absorption also triggered trap-detrapping mechanisms, and an equilibrium was reached with ΔV_{th} being saturated at a lower value than in the dark case. Under light-assisted NBS (NBIS), on the other hand, the photo-generated holes were concentrated at the interface between the Al_2O_3/ZnO, which facilitated the detrapping of electrons trapped at oxide traps and generated a strong negative ΔV_{th} shift. This was coupled with an expansion of the subthreshold swing (SS), which is the activation of oxygen-vacancy-related states and an increase in interface disorder. The continuous negative shift with no saturation indicates the contribution of photo-excited carriers to constant detrapping, which is common with NBIS instabilities reported extensively in IGZO and ZnO TFTs.

These effects are further dependent on temperature, which explains the origins of the dominant defects:

- 150 $°C$ (hydroxyl-rich films): extensive -OH and hydrogen species give good passivation to interface states, leading to the most stable bias stress response and relatively high mobility with steep SS.
- 200 $°C$ (bulk-trap regime): hydrogen passivation removal and the build-up of oxygen deficiencies result in active oxide bulk traps, which introduce the largest ΔV_{th} shifts under PBS and can be observed to cause mobility degradation.
- 250-300 $°C$ (oxygen-vacancy/interfaces-trap regime): densification and Al-rich stoichiometry stabilise oxygen-vacancy-related states, and AFM verified the existence of the increased surface roughness. These defects prevail in NBS and NBIS responses, resulting in the extreme negative ΔV_{th} shifts and the extreme SS broadening.

In sum, the instability processes could be concisely outlined as follows:
PBS-dominated by electron injection into oxide traps, NBS/NBIS-dominated by electron detrappings and interfacial state activations, which are highly promoted by

illumination. The complementary evidence provided by XPS, AFM, C-V hysteresis and I-V stress measurements indicates that the balance between injection and detrapping depends on dielectric defect chemistry and morphology. These observations not only give mechanistic understanding of the trap physics of low-temperature Al_2O_3/ZnO TFTs but also give clear advice on optimal deposition temperatures: low temperatures ($<150\ ^\circ C$) are necessary to delineate the trap physics of hydrogen passivated interfaces. High temperatures ($>250\ ^\circ C$) exacerbate interface-driven instabilities by forming oxygen vacancies.

Chapter 8

Future Work and Conclusion

8.1 Future Work

The choice of the Al_2O_3/ZnO stack used in this work was due to the ability to be fabricated at temperatures below 400 $°C$, thus appealing to 3D heterogeneous integration (BEOL compatibility), flexible electronics, and metal-oxide circuits. The identical temperature limit also excludes standard anneals at high temperatures commonly practised to passivate traps because of the low process temperature. This leads to the necessity of front-end process optimization (patterning, deposition chemistry, and interface engineering). On the basis of the mechanisms introduced in **Chapters 6-7**, three definite directions are suggested.

8.1.1 Gate Patterning Reliability

The present wet-etched gate presents undercut, which locally increases the electric field at the dielectric edge and increases the likelihood of weak points and trap activation during PBS/NBS. This forms an added pressure on dielectric quality.
A dry etched AZO bottom gate can be used to (i) control sidewall angle, (ii) prevent undercut, and (iii) reduce field crowding at gate corners. Just prior to ALD of Al_2O_3, place an in-situ mild plasma clean or introduce an ultrathin nucleation/smoothing layer (typically ∼0.5–2 nm) prior to the main Al_2O_3 ALD, for example a short ALD Al_2O_3 seed layer (5–20 cycles) to promote conformal nucleation across gate steps and corners; alternatively, an ultrathin SiO_2 (or AlO_x) interlayer can be evaluated as a

smoothing layer to improve step coverage and suppress edge-related weak points. Simultaneously, testing a global AZO bottom gate flow (see Table **??** in appendix) to eliminate undercut at all at the gate edges is another method that is worth trying. By considering those works, we expect fewer edge-initiated defects and leakage paths. Benchmark by corner/edge leakage statistics and improved SS stability at high fields.

8.1.2 Low-temperature Dielectric/interface engineering for trap suppression

Electron injection into the oxide and interfacial traps dominates Dark PBS. NBIS / NBS also shows the sensitivity to interfacial states. Since high-T anneals are limited by requiring high temperature ($> 400\ ^{\circ}C$), the deposition pathway itself will be required to suppress traps.
Compare thermal-ALD, PEALD (O_3) Al_2O_3 in the 100–300 $^{\circ}C$ window, tuning precursor/oxidant pulse and purge times to control hydrogen incorporation (beneficial passivation at low T) versus oxygen-vacancy formation. Explore bilayer dielectrics and remote O_2/Ar plasma soft treatments to reduce interface states density without exceeding BEOL budgets is also a proposed work.

8.1.3 ZnO Channel engineering through PEALD plasma-chemistry regulation

In **chapter 7**, ZnO intrinsic defects (V_O, Zn_i, O_i) and sub-gap states were demonstrated to strongly mediate trap-detrapping kinetics and persistent photoconductivity (PPC), thus regulating PBS/NBS and optical stress results. The defects are very sensitive to PEALD O_2-plasma. We have designed a process to evaluate the effect of O_2 flow time to devices, as shown in Table A.3).
According to the initial measurement results which are shown in figure 8.1 and 8.2. Dark PBS (+5 V, 3600 s): transfer curves drift right and extracted $\Delta V_{TH} \sim +2.55$ V, which is consistent with the electron injection/trapping in oxide/near-interface traps. Light-assisted PBS (365 nm, +5 V, 3600 s): curves shift to the left with a strong current lift up and $\Delta V_{TH} \sim 5.11$ V, which shows photo-assisted detrapping and PPC (release of trapped electrons into the channel and reduced re-capture). Dark multi-bias ($\pm 5/\pm 10$ V): $+V_G$ results in a monotonic positive drift to a shallow plateau, and - V_G

shows no significant change as is expected of hole-suppressed detrapping, as shown in figure 8.2. These opposite tendencies reveal the tunability and the need for plasma-chemistry control: by changing the O_2-plasma exposure/flow time, we can both minimize the dark $+\Delta V_{TH}$ and the illuminated negative shift and PPC under UV.

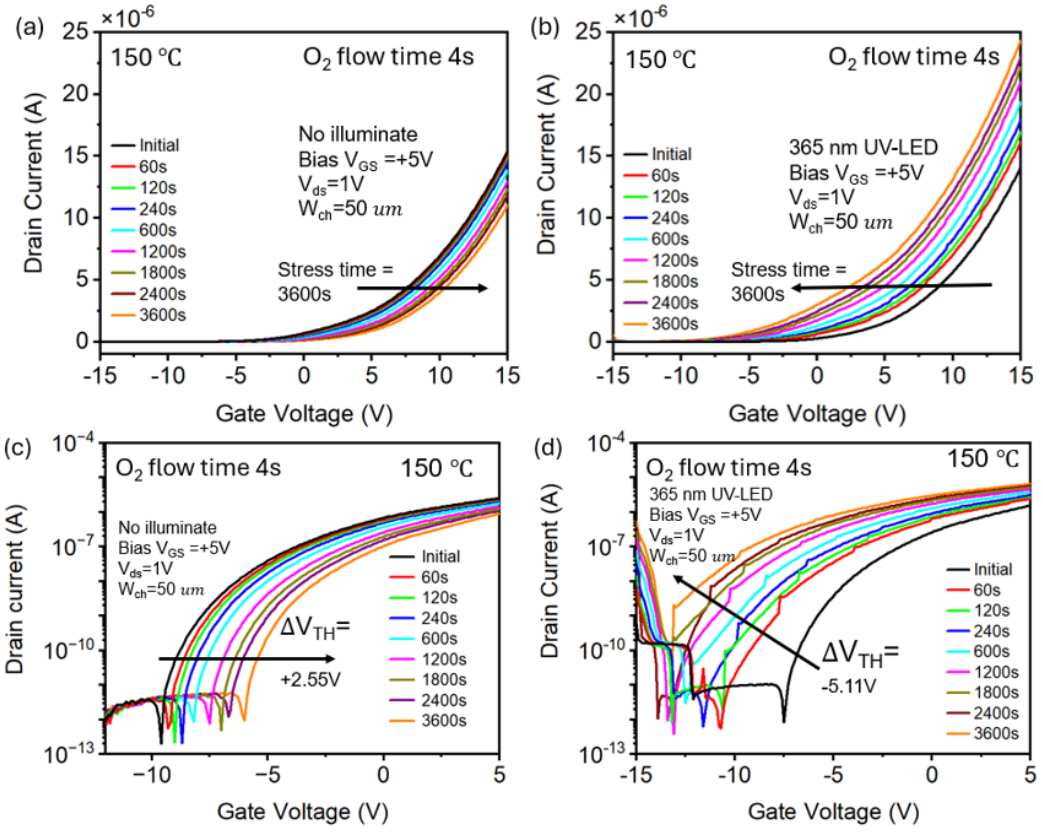


FIGURE 8.1: I-V transfer characteristics of the fabricated ZnO thin film transistor. The device uses Ti/Al bilayer (5 nm/150 nm) as source/drain contacts and Al_2O_3 dielectric on the gate deposited through plasma-enhanced atomic layer deposition (PEALD). To examine how thermal conditions affect the dielectric quality, surface morphology, and interface properties and allow a systematic study of their effects on device performance and reliability, the Al_2O_3 films were deposited at various deposition temperatures (150 $^\circ C$, 200 $^\circ C$, 250 $^\circ C$, and 300 $^\circ C$).

A proposed work can be planned, which records a design of experiments with O_2-flow time = 2, 3, 4, 5, 6 s. Then extract μ_{FE}, SS, D_{it} and ΔV_{TH}(t) under dark PBS/NBS and NBIS. Measure recovery (light-off and temperature-dependent) to measure PPC time constants as well as detrapping barriers. Measure correlated electrical trends and surface quality measurement (XPS, AFM) to map the effect of O_2-plasma timing on the defect spectrum.

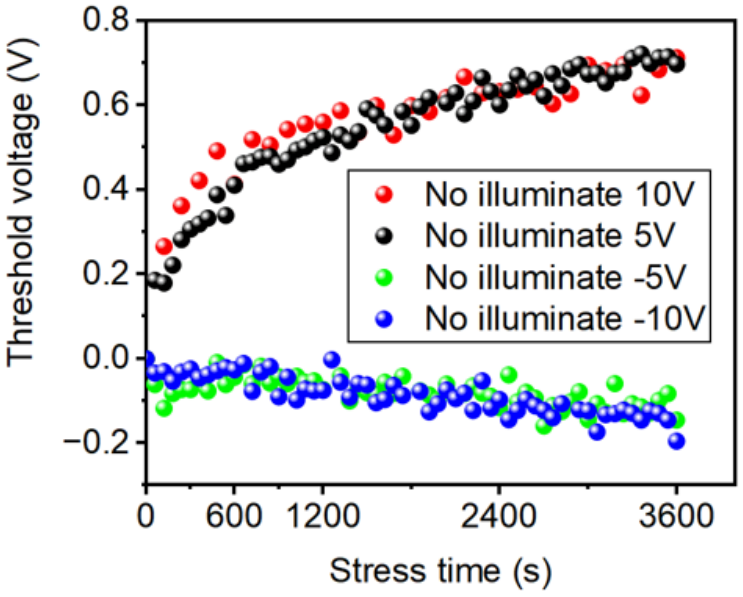


FIGURE 8.2: Threshold voltage evolution as a function of stress time under dark positive and negative bias stress (±5 V and ±10 V). Positive bias stress induces a pronounced positive shift in threshold voltage, whereas negative bias stress results in a comparatively minor negative shift, indicating an asymmetric bias stress response.

The above three proposed works (gate patterning, low-temperature dielectric/interface engineering, and ZnO plasma-chemistry control) would focus directly on the processes observed in this thesis (structure defect, electron injection into oxide traps under PBS, suppressed dark detrapping under NBS, and light-assisted detrapping/PPC). They are also explicitly consistent with the $< 400\ ^{\circ}C$ BEOL limit of the targeted applications. Introduced together, they must provide Al_2O_3/ZnO TFTs with significantly enhanced bias-stress stability in 3D integration, flexible substrates and oxide-logic circuits.

8.2 Conclusion

Overall, this thesis has logically addressed the gap in knowledge regarding the well-known basis of the known knowledge concerning the thin-film-based transistor (TFTs) devices and the little known concerning the impacts of low-temperature deposited high-k dielectric (particularly Al_2O_3) on the device reliability and interface quality of the ZnO-based channels. Although the defect physics of ZnO has been understood before, including the intrinsic defects of ZnO Zhang et al. (2001); Bandopadhyay and Mitra (2015); Cabral et al. (2020); Vidya et al. (2011) and the

influence of oxygen vacancies and zinc interstitials in determining its constant n-type conductivity, and the overall physics of the bias-stress instability in metal oxide TFTs Daus et al. (2025); Zhang et al. (2025), there has been no dedicated study on the direct relationship between the deposition temperature of Al_2O_3, the density of interface defects, and the stability of the electrical characteristics. In addition, PE-ALD grown dielectrics have been reported to potentially permit defect passivation by hydrogen Nam et al. (2016), but there was inadequate investigation into the interaction between bias stress (PBS/NBS) and electrical/optical excitation.

To fill this gap, we constructed an experimental programme plan that was systematic, comprising structural, chemical, and electrical characterizations. Structurally, TEM ((measured by Dr Ben Rowlinson)) was used to measure the morphology of the gate edge, AFM (measured by Mr. Bohao Ding) was used to measure the roughness and morphology of the oxide, and XPS (measured by Mr. Bohao Ding, plotted by Dr Ben Rowlinson) was used to give quantitative results on O/Al ratios and chemical bonding configurations of Al_2O_3 films deposited at varying temperatures. These were complemented with I-V and C-V measurements, in which threshold voltage (V_{th}), subthreshold slope (SS), mobility, and interface trap density (D_it) were obtained. Bias stress tests, indicating work under dark and optical conditions, allowed us to uncouple trapping and detrapping processes, as well as to determine how interface and bulk defects contribute to device instability.

The findings boil down to a number of important results. To begin with, Al_2O_3 deposition temperature is a critical factor that determines film density and hydroxyl incorporation, thus regulating interface trap density and hysteresis. Hydrogen content is maintained at higher levels in low temperature Al_2O_3 ($<200\ ^\circ C$) and effectively passivates defects, but increases long-lived traps, whereas a stress-induced drift in V_{th} is increased by depositing at higher temperature ($>250\ ^\circ C$) and eliminating any hydroxyl concentration, and rougher interfaces and increased fixed charge are obtained. Second, electrical measurements have revealed that charge injection into dielectric/interface traps dominates the instability of PBS, and that NBS instability is severely constrained by the p-Si gate and only becomes significant under optical excitation, where optical-generated carriers catalyse detrapping. Third, optical bias stress at 365 nm exhibited a dynamical balance between fast trapping and photo-assisted detrapping that stabilises ΔV_{TH} at long stress durations. Such observations are in agreement with theoretical descriptions of ZnO defect states Zhang et al. (2001); Bandopadhyay and

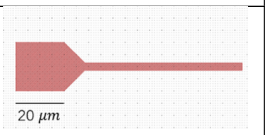
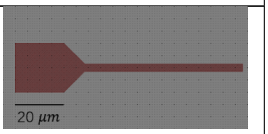
Mitra (2015); Vidya et al. (2011) and recent reports of low-temperature ALD dielectrics Castillo-Saenz et al. (2022a); Zhang et al. (2011); Weber et al. (2011). In general, our results represent a consistent physical image of the connexion between the conditions of Al_2O_3 deposition, defect chemistry, and ZnO TFT reliability. This work will not only provide a solution to one of the perennial dilemmas in oxide electronics, with respect to elucidating the defect-mediated processes that underlie PBS/NBS in dark and luminous conditions, but also provide useful suggestions on optimizing dielectric processing windows in low-temperature, flexible, and transparent electronics.

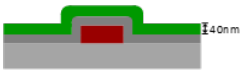
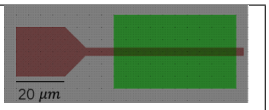
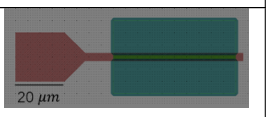
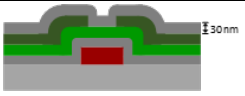
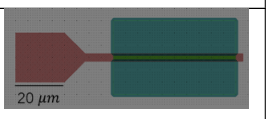
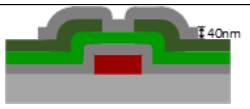
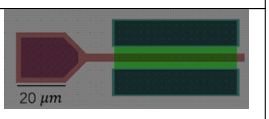
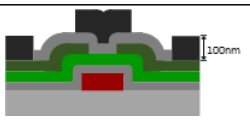
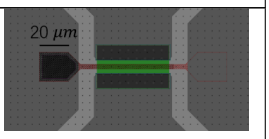
Appendix A

Fabrication process

A.1 Dual-gate fabrication

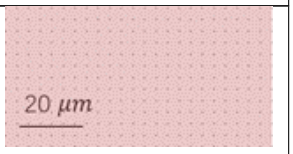
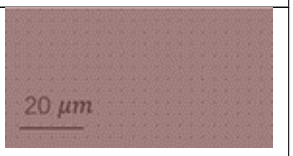
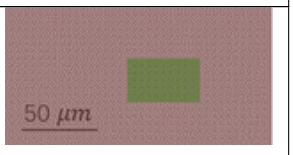
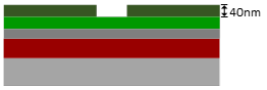
TABLE A.1: *Step-by-step description of the fabrication process for the Dual gate ZnO TFTs, top-view and cross-sections of the design is included*

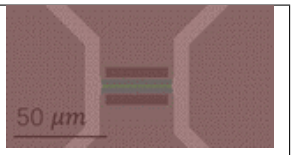
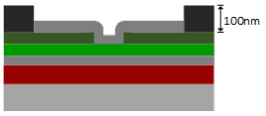
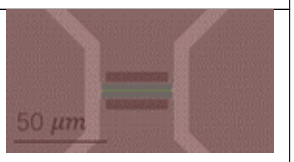
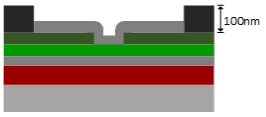
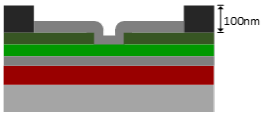
Fabrication Steps (Dual Gate Devices)			
Step	Description	Cross-Section View(not to scale)	Top-View (to scale)
1	45 nm 5% AZO Bottom-Gate deposited by PEALD at 175 $°C$, patterned by Photolithograph using S1813 positive resist and wet etched in HCL (HCL: DI water - 1:1000)		
2	30 nm Al_2O_3 Bottom Dielectric layer deposition by PEALD at 150$°C$		

3	40 nm ZnO Channel deposited by PEALD at 190°C, patterned by Photolithograph using S1813 positive photoresist, and wet etched in HCL (HCL: DI water - 1:1000)		
4	40 nm 2% AZO Source and Drain contacts deposited by PEALD at 175°C, patterned by Photolithograph using AZ2020 negative resist and Lifted-off in NMP		
5	30 nm Al_2O_3 Top-dielectric layer deposition by PEALD at 150°C		
6	Vias opened by wet etching using TMAH (25% TMAH: DI water - 80: 8000), patterned by Photolithograph using S1813 positive photoresist, the source drain layer (2% AZO) as an etch stop layer		
7	100 nm Al metal contact pads deposited by Evaporation, patterned by Photoresist AZ2020 negative resist and lifted off in NMP		
End of Fabrication Steps			

A.2 AZO Global bottom gate

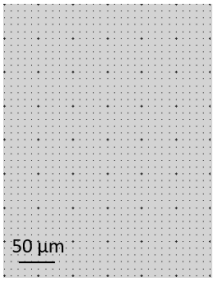
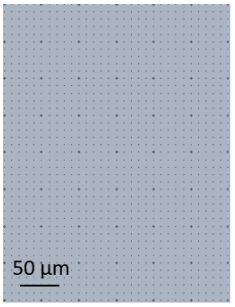
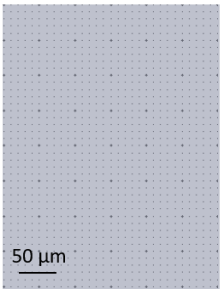
TABLE A.2: *Step-by-step description of the fabrication process for the Global bottom gate ZnO TFTs, top-view and cross-sections of the design is included*

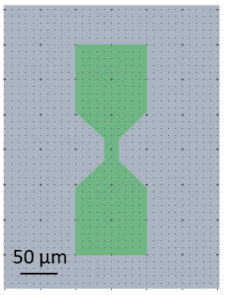
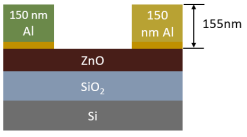
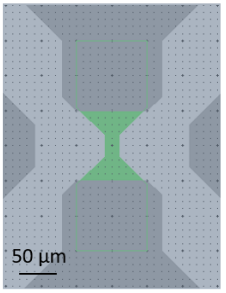
Fabrication Steps (AZO Global Bottom Gate Devices)			
Step	Description	Cross-Section (not to scale)	Top-View (to scale)
1	45 nm 5% AZO Bottom-Gate deposited by PEALD at 175°C		
2	30 nm Al_2O_3 Bottom Dielectric layer deposition by PEALD at 150°C		
3	40 nm ZnO Channel deposited by PEALD at 190°C, patterned by photolithography using S1813 positive photoresist, and wet etched in HCL (HCL:DI water = 1:1000)		
4	40 nm 2% AZO Source and Drain contacts deposited by PEALD at 175°C, patterned by photolithography using AZ2020 negative resist and lifted off in NMP		

5	30 nm Al_2O_3 passivation layer deposition by PEALD at 150°C, with vias opened by wet etching using TMAH		
6	100 nm Al source and drain metal contact pads deposited by evaporation, patterned by AZ2020 negative resist and lifted off in NMP		
7	Vias opened by wet etching using TMAH, patterned by S1813 positive photoresist, with the bottom gate layer (5% AZO) as an etch stop layer		
8	100 nm Al global bottom metal contact pads deposited by evaporation, patterned by AZ2020 negative resist and lifted off in NMP		
End of Fabrication Steps			

A.3 Si Global bottom gate

TABLE A.3: *Step-by-step description of the fabrication process for the Si Global bottom gate TFTs, top-view and cross-sections of the design is included*

Fabrication Steps (Si Global bottom Gate Devices)			
Step	Description	Cross-Section (not to scale)	Top-View (to scale)
1	150nm dummy silicon wafer prepare		
2	100 nm SiO_2 Bottom Dielectric layer grown through thermal oxidation		
2	30 nm Al_2O_3 Bottom Dielectric layer deposited by PEALD at $150°C/200°C/250°C/300°C$		

3	40 nm ZnO Channel deposited by PEALD at 190°C, patterned by Photolithograph using S1813 positive photoresist, then wet etched in HCL (HCL:DI water - 1:1000)		
4	5 nm Titanium and 150 nm Al deposited continuously by sputtering, patterned by photolithograph using AZ2020 negative photoresist, then lift off in NMP (80°C, 3 hours)		
End of Fabrication Steps			

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