UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING AND APPLIED SCIENCES
DEPARTMENT OF ELECTRONICS AND COMPUTER SCIENCE

Towards an Integrated Atom Chip

By

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ABSTRACT

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The field of atom chips is a relatively new area of research which is rapidly becoming of great interest to the scientific community. It started out as a small branch of cold atom physics which has quickly grown into a multidisciplinary subject. It now encompasses topics from fundamental atomic and quantum theory, optics and laser science, to the engineering of ultra sensitive sensors.

In this thesis the first steps are taken towards a truly integrated atom chip device for real world applications. Multiple devices are presented that allow the trapping, cooling, manipulation and counting of atoms. Each device presents a new component required for the integration and miniaturisation of atom chips into a single device, capable of being used as a sensor.

Initially, a wire trap was created capable of trapping and splitting a cloud of Bose Einstein condensate (BEC) for use in atom interferometry. Using this chip a BEC has been successfully created, trapped and coherent splitting of this cloud has been achieved.

Subsequently, the integration and simplification of the initial trapping process was approached. In all the experiments to date, atoms are initially collected from a warm vapour by a magneto-optical trap (MOT). This thesis presents a new approach in which microscopic pyramidal MOTs' are integrated into the chip itself. This greatly reduces the number of optical components and helps to simplify the process significantly.

Also presented is a method for creating a planar-concave micro-cavity capable of single atom detection. One such cavity consists of a concave mirror fabricated in silicon and the planar tip of an optical fibre. The performance of the resonators is highly dependent on the surface roughness and shape profile of the concave mirrors therefore a detailed study into the fabrication technique and its effects on these parameters was undertaken. Using such cavities single atom detection has been shown to be possible. These cavities have also been successfully integrated into an atom wire guide.

Finally a co-sputtered amorphous silicon/titanium (a-Si/Ti) nanocomposite material was created and studied for its use as a novel structural material. This material is potentially suitable for integrated circuitry (IC)/Micro-electro-mechanical-systems (MEMS) integration. The material's electrical and structural properties were investigated and initial results suggest that a-Si/Ti has the potential to be a compelling structural material for future IC/MEMS integration.

To build all of these devices, a full range of standard microfabrication techniques was necessary as well as some non standard processes that required considerable process development such as the electrochemical deposition.

This thesis presents a tool box of fabrication techniques for creating various components capable of different tasks that can be integrated into a single device. Each component has been successfully demonstrated in laboratory conditions. This represents a significant step toward a real world atom chip device.

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DECLARATION OF AUTHORSHIP

I, Gareth Neil Lewis declare that the thesis entitled 'Towards an Integrated Atom Chip'

and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published as:

Resistivity percolation of co-sputtered amorphous Si/Ti films, Materials Letters, Volume 63, Issue 2, 31 January 2009, Pages 215-217

Fabrication of Magneto-Optical Atom Traps on a Chip, Journal of Microelectromechanical Systems, Accepted for publication

Signed: ……..

Date:……

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Chapter 1

Introduction

Since the Nobel Prize winning work of Cohen-Tannoudji, Chu and Phillips for laser cooling and trapping of atoms in 1997 [1] and Ketterle, Cornell and Wieman for Bose-Einstein condensation (BEC) in dilute alkali gases in 2001 [2], there has been a huge increase in the field of cold and ultra cold atom physics. Using ultra cold atoms it is possible to study the quantum wave like nature of matter in a manner not previously possible which, in turn, is opening up the field of atom optics and quantum information processing. These original traps were created using only optical elements but since then new faster methods for producing BEC's have been created involving micro machined microchips [3].

Micro-Electro-Mechanical Systems (MEMS) is the manufacturing of micro machined sensors and actuators on a substrate to create new integrated devices. Using tools and methods developed for the integrated circuit industry, microelectronic fabrication techniques are combined with micromachining processes to realise a complete system on a single microchip. MEMS processing is therefore ideally suited for use in the production of micro machined chips for trapping ultra cold atoms often termed 'atom chips'. Atom chips combine cold atom physics with MEMS microfabrication techniques to create electric, magnetic and optical fields to trap and manipulate cold atom clouds [4-6] and to form BECs [7-9].

Over the last two decades the field of atom chips has advanced rapidly. Initial experiments involving the trapping of ultra cold atoms soon led to the production of a BEC on such microchips. These experiments continued to advance from simple traps and guides [10, 11] to conveyor belts [12] that allow the BEC to be moved non destructively along the surface of the chip.

Looking further into the future even more elaborate designs have been envisioned like atom-optical systems for use in applications including atomic clocks [13], atom

interferometry [14], gyroscopes [15] and quantum information processing [16]. For the realisation of such devices optical integration will be required and so this is of great interest to the field.

1.1. Motivation and approach

Electronics has benefited massively from the miniaturisation and integration of components allowing the control and manipulation of the electron. Many of the advances in science and technology would have been impossible without this technology. The electron was first discovered in 1898 by Thomson and since then our ability to control and manipulate this particle has enabled the creation of much of the technologies we now take for granted. With inventions such as the p-n junction, the transistor and integrated circuits, modern electronics has exploded. Using these devices it became possible to manipulate electrons in a manner never before possible.

A similar story is true of the photon. The idea of a photon was first broached by Planck in 1901, whose work on blackbody radiation led to the hypothesis that the energy of any system that absorbs or emits electromagnetic radiation is an integer of an energy quantum. It was not however, until the invention of the laser in 1960 that the field of research really took off. This was followed by the development of the optical fibre in the 1970s and the fibre amplifier which allowed the photon to be transmitted with precision over large distances. These inventions were the basis of the telecommunications revolution at the end of the 20^{th} century.

Atom chips bring the promise of being able to control and manipulate atoms in a similar manner to which we now control electrons and photons in electronics and optoelectronics. To achieve this high precision control over atoms is required. This would enable controlled quantum manipulation and entanglement. This is possible using miniature current carrying wires to create electric and magnetic potentials. Integration with optical elements will allow the creation, manipulation and measurement of the atoms. With such devices a miniature quantum laboratory would be possible allowing fundamental research into quantum behaviour, low dimensional

physics, entanglement and coupling experiments to mention but a few. Successful implementation of these chips could then lead to widespread applications from highly sensitive sensors to quantum information storage and processing.

A major achievement of this field would be to create ultra sensitive portable sensors for real world applications. However, to achieve this much work is needed. Currently an atom chip experiment requires a laboratory full of equipment and auxiliary systems. Tables full of optical components; multiple lasers, mirrors, lenses, wave plates, beam splitters etc,. vacuum pumps and a chamber capable of ultra high vacuum; banks of electronics from power supplies, amplifiers and oscilloscopes to computers required for recording and analysis the results are all required For a complete list and explanation of a typical setup see reference [17].

1.2. Aims of this thesis

In this thesis the aim is to both create devices for trapping and manipulating atoms and also to try to simplify some of these auxiliary systems required for trapping and detection. This is achieved by designing and fabricating novel atom chips by integrating electronic, magnetic and optical elements on a single device that can be used to trap and manipulate ultra cold atoms and Bose Einstein condensates. It aims to create a 'tool box' of techniques and components that will be a step towards the ultimate aim of creating a single integrated portable sensor for real world applications.

1.3. Summary of the main achievements

During this research a number of original contributions to science were achieved.
These are outlined briefly below:

An atom chip consisting of gold microwires for the controlled, coherent manipulation and splitting of a Bose-Einstein condensate was designed and fabricated. This involves the creation of microwires capable of withstanding high current densities

with highly smooth surfaces to prevent disturbance of the resultant magnetic potentials used to trap the condensate.

Another device created was an atom chip integrating optical elements. A system for creating microscopic magneto optical traps (MOT's) integrated into an atom chip was designed and fabricated. This can be used to collect small atom clouds that are automatically well positioned with respect to the traps on the chip. To realise this optical trapping it was discovered that the cavities must be patterned, a method was therefore implemented for deep cavity patterning. This device integrates both an on-chip optical trapping method with gold microwires allowing the manipulation of the atom clouds once created.

A method was developed for fabricating high finesse optical cavities which can be easily integrated into existing atom chips. An in depth study into how to optimise these cavities has been undertaken. The cavities were then integrated into an atom chip. This was combined with an optical fibre to produce a laser cavity capable of, on-chip, single atom detection.

Finally, a study into a novel MEMS material suitable for the integration of MEMS structures with integrated circuits (ICs) was performed. In this study the effect of using titanium as the co-sputtered metal along with amorphous silicon was investigated, aiming to create a new MEMS structural material with a compatible temperature budget while retaining MEMS functionality such as the ability to deposit and process it using standard methods.

1.4. Thesis structure

Chapter 2 presents the basic science behind the trapping of atoms and creation of Bose-Einstein condensates for use in atom chips. It also presents a literature review of the current fabrication techniques being used to create atom chips. This chapter includes an overview of the techniques used by other groups as well as the specialist methods used to produce the various devices fabricated in this thesis.

Chapter 3 describes the design, fabrication and testing of an atom guide and interferometer. The atom chip has four Z-shaped wires and two end-wires. The geometry of the Z wires is designed to create an Ioffe-Pritchard magnetic trap. The multiple parallel wires allow a single trapping potential to be split into two or more traps forming an analogue of an optical beam splitter.

Chapter 4 describes the design, fabrication and testing of an integrated array of micro magneto optical traps integrated into an atom chip. Each of these MOTs automatically provides all the required light beams from a single circularly polarised input beam by reflecting the light in a concave square pyramid of mirrors. This greatly reduces both the number of expensive optical components needed to prepare the light beams and the amount of laser power required.

Chapter 5 describes the design, fabrication and testing of hemispherical micro cavities and their integration into atom chips. These cavities are designed to have a very small mode volume and a high finesse while allowing atoms direct access to the high intensity part of the field to enable single atom detection.

Chapter 6 describes the design, fabrication and testing of a novel composite MEMS material consisting of co-sputtered silicon and titanium. The material is designed to have a tuneable conductivity while still being compatible with the low thermal budgets of complimentary metal oxide semiconductor (CMOS) wafers.

Finally chapter 7 states the conclusions of this work and the overall achievements. It also sets out a plan for further work arising from this thesis.

Chapter 2

Literature Review

The atom chip project is a multi disciplinary area of research. This chapter gives an overview of the development and current literature on atom chips. This is followed by a review of some of the auxiliary components required to make trapping atoms using atom chips possible.

2.1. Interferometry

Interferometry covers a large area from optics to matter waves. Generally speaking an interferometer can be described as a device that utilises the superposition of waves and produces measurable interference patterns. This is achieved by splitting an incoming beam into two components which then follow different paths through space. Each path may encounter a slightly different environment causing a phase shift. When the beams are then recombined an interference pattern will be created and this can be measured. In atom interferometry a beam of atoms is used instead of a beam of light. The beam is split into two paths and then later recombined and the interference fringes are observed in a similar manner to laser interferometry. A simple schematic of this idea is shown in Figure 1.

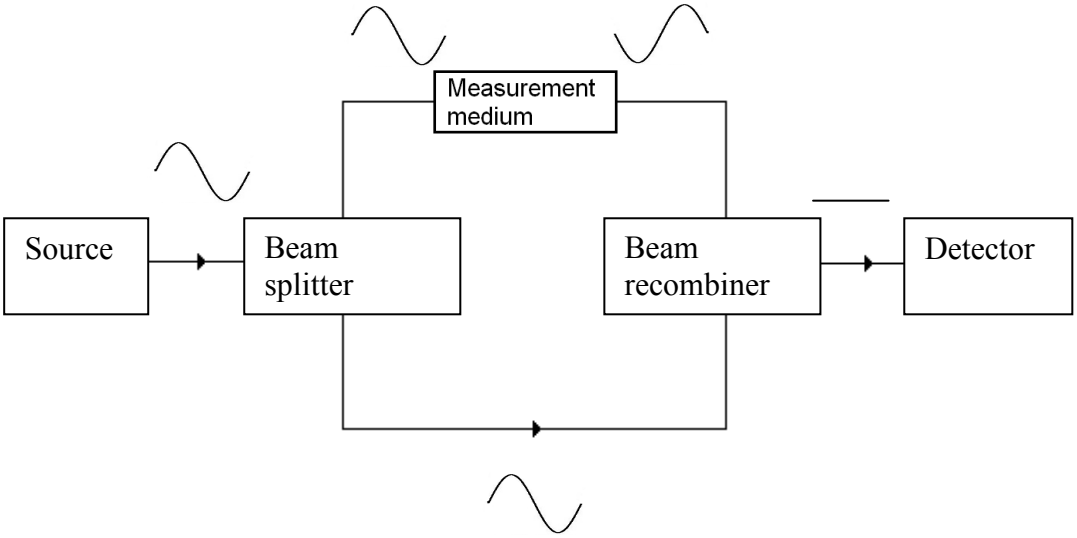

Figure 1: A generic interferometer. A single phase source is used as an input. This beam is then split and one path experiences a different condition such as going through a medium and the phase is changed. Both beams are then recombined and interference occurs which is measured by the detector.

In order to perform interferometry a coherent source of atoms is desirable. One source of highly coherent atoms would be from a Bose-Einstein condensate. Bose-Einstein condensation was first predicted in 1924 by the work of both Albert Einstein and Satyendra Bose [18]. It was however not until 1995 that the first BEC was observed. It was created by Cornell, Wieman, and their co-workers at JILA [19] for which they later received the 2001 Nobel Prize for physics.

A Bose-Einstein condensate is a phase of matter formed when bosons are cooled to temperatures very near absolute zero. At high temperatures an atom can be described by a solid sphere that obeys the laws of classical mechanics as shown in Figure 2a. At extremely low temperatures, or small volumes, this model begins to fail and quantum mechanics starts to play a more important role. When this occurs the atom is more accurately described as a wave packet spread over a region of space. As the temperature decreases this wave packet expands, as shown in Figure 2b, until eventually merging with those of other atoms, Figure 2c. At this point if the atoms are bosons they will form a state called a Bose-Einstein condensate. This is the point when all the atoms fall into their lowest quantum state. The wave packets of the individual atoms merge into a single macroscopic packet making single atoms indistinguishable as shown in Figure 2d.

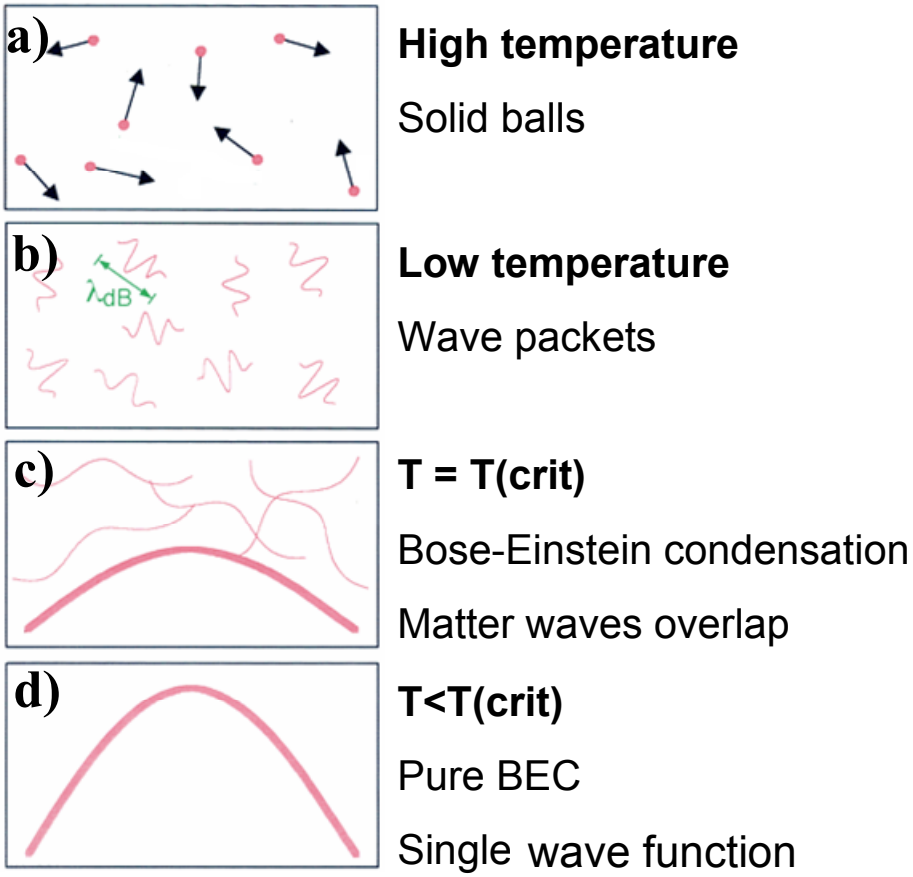

Figure 2: Image showing the formation of a Bose-Einstein condensation as atoms undergo increasingly low temperatures (Taken from ref [20]).

2.1.1. Atom interferometry and gyroscopes

Interferometry has many applications in the modern world. It can be used in sensors for many applications from gyroscopes for navigation to scientific sensors for use in fields as varied as oil exploration to searching for gravitational waves. To create a gyroscope, instead of sending the beams over two different paths in space, the beams are made to propagate in opposite directions around a common path. If the interferometer is then rotated one path will shorten and the other lengthened by a factor related to the speed of the rotation. This will create a phase shift in the beams and therefore an interference pattern. This effect is called the Sagnac effect and was first demonstrated for atoms in 1991 by J. Helmcke et al. [21]. Atomic interferometers are also sensitive to accelerations. This sensitivity has been used to develop high precision measurements of the local acceleration due to gravity and its gradient [22].

Atom interferometers have one main advantage over the typical laser interferometer. Atoms interact with a wider range of phenomena and with a greater sensitivity. This can be well demonstrated using the Sagnac effect. If the interferometer is rotated the phase shift (φ) between the two beams is given by

$$\varphi = \frac{4\Omega A\pi}{\lambda v} \tag{1}$$

Where Ω is the rotation frequency, A is the area enclosed by the beams, v is the velocity of the atom or particle and λ is the wavelength [23]. The wavelength is dependant on the beam type.

For a photon

$$\lambda = \frac{c2\pi}{\omega} \tag{2}$$

For atoms

$$\lambda = \frac{h}{mv} \tag{3}$$

where c is the speed of light, ω is the angular frequency, h is Planck's constant and m is the mass. Using this it is possible to approximate the difference in sensitivity for the two systems.

$$\frac{\varphi_{atom}}{\varphi_{Light}} = \frac{mc^2}{\hbar\omega} \approx 1x10^{10} \tag{4}$$

where

$$\hbar = h/2\pi. \tag{5}$$

This shows that an atom beam can give significant improvements over a conventional laser beam system. Further improvements can be made by using a Bose-Einstein condensate. In a thermal beam the atoms move at very high speeds. This makes them difficult to manipulate. This high speed also makes it difficult to produce a

significant beam deflection which in turn makes the area enclosed by the beams smaller. This will lead to a decreased sensitivity due to a reduced phase shift. The coherence length is also orders of magnitude better in a Bose-Einstein condensate. A comprehensive review of atom optics and interferometry can be found in ref [24].

2.2. Atom chips

This section gives an overview of the development and current literature on atom chips. It does not aim to be an exhaustive review of every single chip made but shows the progression of the field to its current state. Particular attention is paid to the fabrication processes and their suitability for integration into a practical working device.

2.2.1. History of atom guides

Many techniques have been used to trap and manipulate atoms and atomic beams. In recent years these have evolved into 'atom chips'. It was in 2000 when Folman et al. first coined the term atom chip, referring to chips created using microfabrication techniques that can be used to trap and manipulate ultra cold neutral atoms [25]. However, the field of atomic trapping has been around well before this terminology was created.

Atom chips are devices designed to integrate atom optics, control of magnetic and electric fields, and MEMS into single chips which will enable the trapping, manipulation, detection and measurement of atoms and their properties. Many different designs of atom chips have been fabricated each using a wide range of techniques. In the following chapter these chips and the fabrication techniques used to create them are discussed.

One of the first attempts at deflecting atoms was performed in 1921 by Stern and Gerlach [26]. This work involved deflecting atomic beams with magnetic fields. For the following years most work in manipulation of neutral atoms revolved around

small angle deflections of neutral atom beams using magnetostatic fields. The invention of laser cooling allowed a much greater control in the trapping and manipulation of atoms [27]. Using this technique, clouds of ultra cold atoms could be created which essentially have zero kinetic energy. These clouds can then be manipulated using relatively small potentials.

The first 3D trap for neutral atoms was created by Migdall et al. in 1985 [28]. They used two coaxial coils of radius 2.7 cm to carry the current. The current in the coils was setup in opposite directions creating a zero field in the centre. The presence of a zero field however presents a problem of spin flip loss from the trap. A solution to this is to create an Ioffe-Pritchard trap [29] that does not contain a zero field point. This was done by adding four current carrying wires running through and parallel to the two coils. However these still involved relatively large coils of wires.

Work then began on manipulating these cold atoms using microstuctured magnetic surfaces instead of laser potentials. In 1995 the first example of atomic retroreflection from a surface with microscopic magnetic structure was presented by Hinds et al. [30]. This involved releasing rubidium atoms from a MOT and allowing them to fall by gravity onto a strip of magnetic audio tape that had a sinusoidal magnetisation signal recorded onto it. The result was the atoms 'bounced' off the tape and could then be recaptured in the MOT. This technique was further improved by using different magnetic media, first a floppy disk [31] and then videotape [32]. The use of magnetic storage media made it possible to easily create strong interaction potentials over a short range. This method is clearly not compatible with most other fabrication techniques and is therefore not easily integrated into more complex devices.

The use of magnetic materials advanced from using recording media to structured films of magnetic materials such as TbGdFeCo [33] FePt [34] and $(BiYTmGd)_3(FeGa)_5O_{12}$ [35]. Devices made of such materials have a few advantages over current carrying wires. These films do not suffer from electrical-power dissipation issues. They do not suffer from magnetic field fluctuations and noise produced from temporal and spatial fluctuations in the current used in wires. These films do however, suffer from an inability to switch and modulate the field in a manner easily obtained using current carrying wires. They are also often difficult to

fabricate and can be incompatible with many common MEMS techniques. For this reason no work has been done using such films in this thesis.

At the same time in work presented by J. Weinstein et al. [36] designs for planar microscopic traps were given. This work discussed the advantages of using microstructures to create extremely high field gradients. It also showed that microwires could be easily fabricated using standard microfabrication techniques, which were ideal for atom trapping.

This was then fabricated in 1998 by Drndic et al. [37] as shown in Figure 3. The device was fabricated on sapphire and the gold wires electroplated into a lithographically patterned mould. Current carrying wires have several critical advantages over permanent magnets. The magnetic field can easily be varied or switched by varying the current in the wire and they are more suited to current microfabrication techniques.

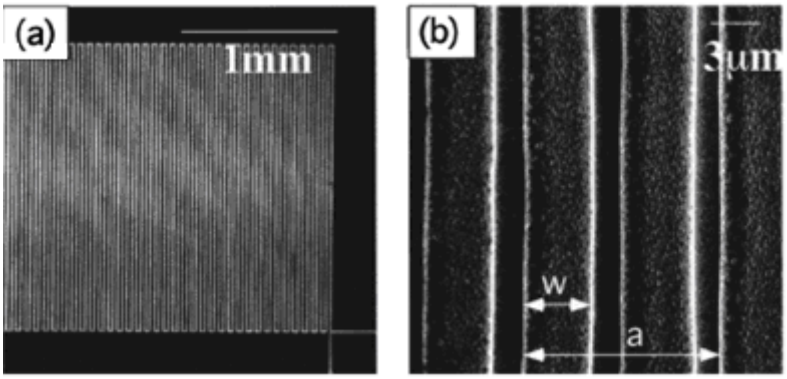

Figure 3: SEM images of micro-electromagnets with geometries suggested in [36] created by Drndic et al. [37]. This was the first 'atom chip' to use microwires for trapping atoms. a) shows the microwires while b) shows a close up of these wires.

The field then began to expand rapidly with many groups starting to create atom chips using microfabricated wires. For example, Hannaford's group in Melbourne [38] created their microwires on a silicon wafer. This was coated in a thin nickel adhesion layer and followed by a gold seed layer. They spun and then developed a photoresist onto the gold. This acted as a mould for the electroplated wires to be grown in. The photoresist was then removed and the seed layer etched away using a wet etch. It has since been discovered that such wires are highly unsuitable for creating smooth trapping potentials. The wet etch of the seed layer will also etch the wires

themselves. This has the effect of creating a highly rough, jagged wire edge [39], which in turn creates rough trapping potentials. However, their fabrication method uses standard MEMS technology and cleanroom compatible materials making it ideal for integration and fabrication into more complex devices. Microchip materials also generally have low outgassing rates making them suitable for ultra high vacuums required in these experiments.

Having shown the ability to deflect clouds of atoms the next step was to be able to transport and guide the atoms. As light can be carried down optical fibres so the ability to control the path of atoms in a similar fashion was desirable as this is a requirement for the realisation of more complex devices. Such a device was suggested by Hinds [5] involving four parallel current carrying wires, equally spaced, carrying +I and –I currents alternately. In this work the current required to trap rubidium atoms at 10 μK in a guide of radius R = 1 mm is calculated to be 1.1 kA. However, it was also found that the required current scales as R^2 so using a wire of R=10 μm the current drops to 110 mA. It was shown that with cooling to 100 K a wire of cross section 1 μm by 3 μm could carry 1.8 A ($6x10^{11}$ Am^{-2}) [37]. This showed another advantage of making the trapping wires on a micron scale.

In 1998 Fortagh et al. [40] produced the first miniaturized waveguide for atoms using a single current carrying wire and the addition of a uniform perpendicular magnetic field. To do this they used a 45 μm thick copper wire capable of carrying 3 A. This method has two major drawbacks. Firstly, the wire was free standing and not created on any substrate. Although simple to produce it could not be used for creating complex shapes and therefore trapping potentials. This method also requires an external magnetic field. Again this is not ideal for the creation of a self contained device.

In October 1999 Reichel et al. [3] published the results of trapping cold atoms using wires microfabricated onto a sapphire substrate. This was the first time neutral cold atoms had been trapped by microfabricated wires. With the move to the creation of wires on solid substrates came new problems. Loading the trap is problematic due to the microtraps' small volume and the proximity of the atoms to the substrate. To load the chip the atoms must first be trapped and cooled using a MOT. The placing of a

large substrate into the chamber will block the laser beams and make trapping by an ordinary MOT impossible.

One solution is to turn the substrate itself into a mirror and initially trap and cool the atoms using a mirror MOT system which is further described in detail in section 2.3. An example of such a chip is shown in Figure 4. The surface of the whole chip has been turned into a mirror by applying a gold layer. Such a method does impose constraints. The area surrounding the wires must be an optically reflective smooth surface. It also must have a surface area in the order of 5 cm^2 to accommodate the laser trapping beams [41]. To avoid the problems associated with keeping a large area of gold smooth and undamaged while creating structures around it, some groups have taken a different approach.

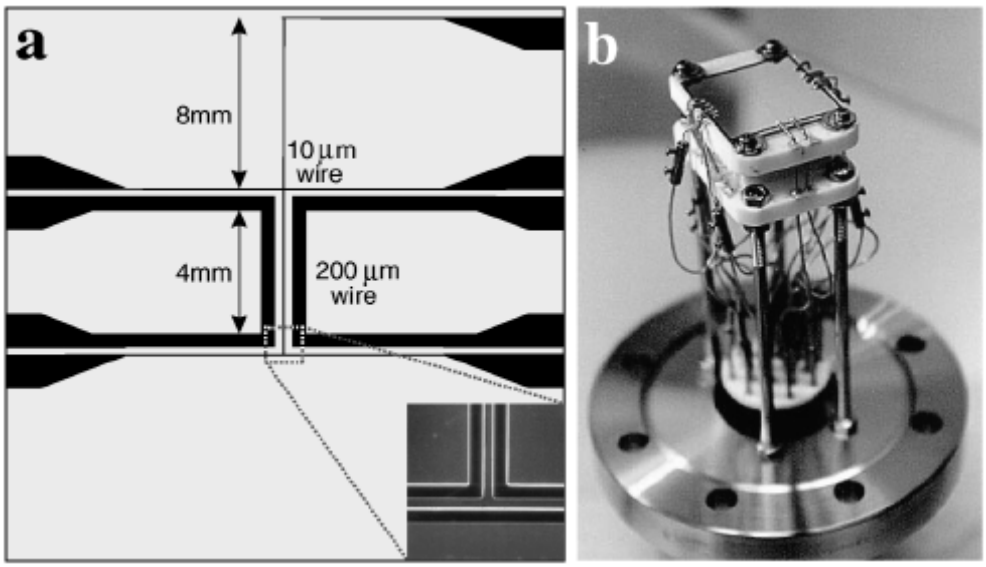

Figure 4: A schematic and photograph of the atom chip created by Folman et al. [25]. The wide wires are 200 mm wide while the thin wires are 10 mm wide. The inset shows an electron microscope image of the surface and its 10 µm wide etchings defining the wires. Part b shows the mounted chip before it is introduced into the vacuum chamber.

In work by Esteve et al. [42] the wires were first created by taking a silicon substrate with an insulating layer of silicon oxide. This was covered in an evaporated layer of titanium and gold. This layer is patterned and wet etched. A photoresist mould is then created and the wires electroplated into this to a thickness of 4.5 µm. The mirror surface is then created over the top of the wires. This is done by covering the substrate in a planarising dielectric layer of a Benzocyclobutene based polymer

(BCB). On top of this a 200 nm layer of gold is evaporated. This has the advantage that the gold mirror layer is applied last so avoiding any damage during the processing.

Another group used a similar technique whereby the gold wires are fabricated onto an aluminium nitride substrate using standard lithographic processes. Meanwhile on another substrate a 250 nm layer of silver is sputtered. The wires are then covered in epoxy glue and 25 μm gold wires are placed at the edge of the chip to act as spacers. The substrates are then sandwiched together and left until the glue has cured. The silver substrate is then lifted off leaving a silver mirror over the top of the current carrying wires isolated by the epoxy glue layer [43].

A detailed fabrication method for creating atom chip wires was given by Koukharenko et al. [44]. In this paper two methods were described. One method used sputtering and wet etching, the other technique used electroplating into a photoresist mould. In both cases silicon wafers were used as the substrate. The results showed the top surface roughness of the sputtered wire to be much rougher than the electroplated wires. The sputtered wire also had grain sizes approximately ten times larger than the electroplated wires. While the side walls were not studied in this work, further work in section 3 of this thesis showed the side walls of the sputtered/wet etched wires were considerably rougher than the relatively smooth side walls produced from electroplating into a photoresist mould. In this paper wires were also created by growing a thick evaporated gold film 5 μm thick and then ion beam milling the wire patterns into the wires. This method has the draw back of over etching into the substrate due to the non uniformity of the etching over the whole wafer. This means that in some places the wafer must be over etched to ensure other areas are etched sufficiently. This could cause problems if structures are required under the wires.

A very simple device was created by Vale et al. [45] using simple micro cutting techniques with no photolithography. A 125 μm thick silver foil was glued onto a ceramic substrate of macor. The foil was then polished in several steps to achieve an optically reflective surface. The wire pattern was then cut into the foil using a computer controlled milling machine. The cut trenches were then filled with epoxy

glue and the surface repolished. This method is much cheaper than using the more complex MEMS processing for single device manufacturing however it is not suitable for batch processing and it can only be used to create features on a scale >100 μm.

With many groups now successfully creating and trapping cold atoms and BECs using atoms chips new ideas for more complex devices began to be created. Continuing with the goal of manipulating atoms, to the same level possible with photons, experiments began on beam splitters and working towards an interferometer [46, 47].

The ability to split beams of atoms had been done previously and even used in interferometry [48, 49], however these devices only worked on beams of atoms moving through free space. Using atom chips to guide atoms close to a surface greater control is possible and this led to the first beam splitter being demonstrated in 2000 by Cassettari et al. [50]. Figure 5 shows the results of their experiments where cold lithium atoms were guided and split by an angle of 15 degrees. By varying the current in each arm the splitting fraction can be continuously changed. In the image a 50:50 split is shown. However the splitting was not achieved using a coherent matter source which is required for interferometry. Towards this aim a BEC would be a suitable source of coherent matter.

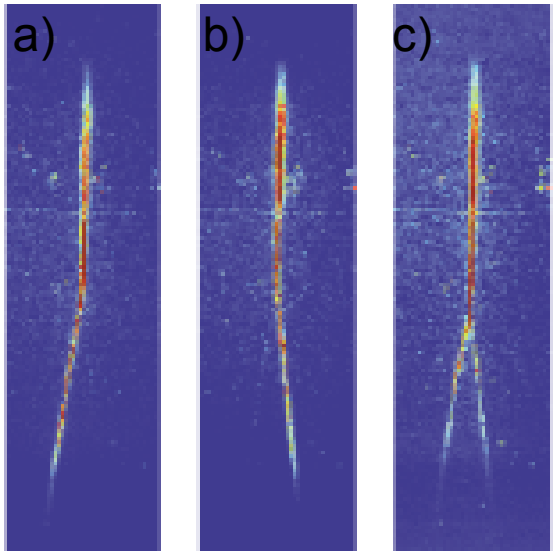

Figure 5: Demonstration of a beam splitter on a chip. The image shows fluorescence images of guided atoms. a) Showing current driven through the left side and therefore guiding the atoms to the left, b) showing current driven through the right side and therefore guiding the atoms to the right and c) current split equally to both paths therefore splitting the cloud (Taken from ref [50]).

In 2004 Wang et al. created the first atom Michelson interferometer on a chip [14]. This device uses lithographically patterned wires and a pair of large prism shaped mirrors. The mirrors used are glued onto the substrate as shown in Figure 6. While this chip allowed the first on chip observation of atom interference its structure is not well suited for further integration. The prisms provide a simple method of introducing a laser beam into the system parallel to the chip surface. However this type of structure could be fabricated using MEMS techniques on a silicon wafer and the laser light applied via a fibre optic to allow further reduction of the cumbersome prisms. This is also a fixed structure which prevents any tuning of the system.

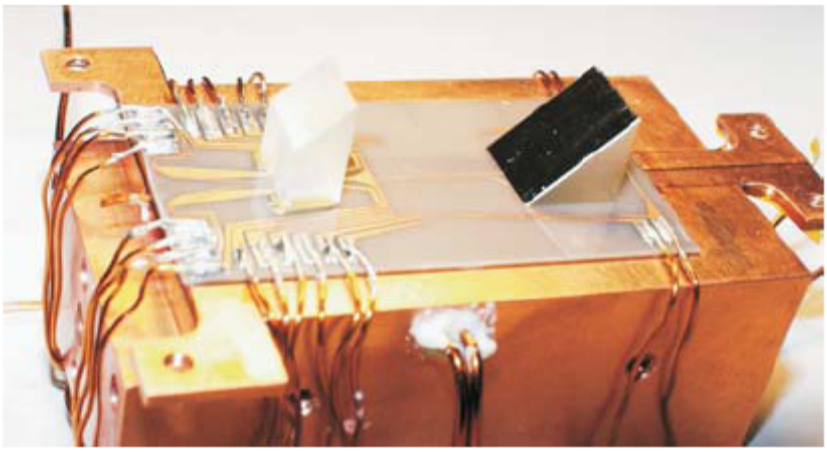

Figure 6: Photograph of the atom interferometer glued onto a copper holder. The chip is 5 x 2 cm (Taken from ref [14]).

This chip is a good example of the advantages that could be gained by the integration of optical elements into atom chips. Optical elements are important throughout the atom chip, from the initial trapping phase using MOTs to the detection of the atoms in the traps. For the creation of portable devices optical integration is therefore very important.

Another good example of what is possible when MEMS techniques are used to miniaturise and integrate multiple components is a microfabricated atom clock created by Knappe et al. in 2004 [51]. The device is shown in Figure 7, it measures 4.2 mm tall with a square cross sectional area measuring 1.5 mm in length. This single device incorporates a laser, vapour cell, micro optics package for collimating and polarising

the light and a photodiode. This device is 100 times smaller, by volume, than previous state of the art devices.

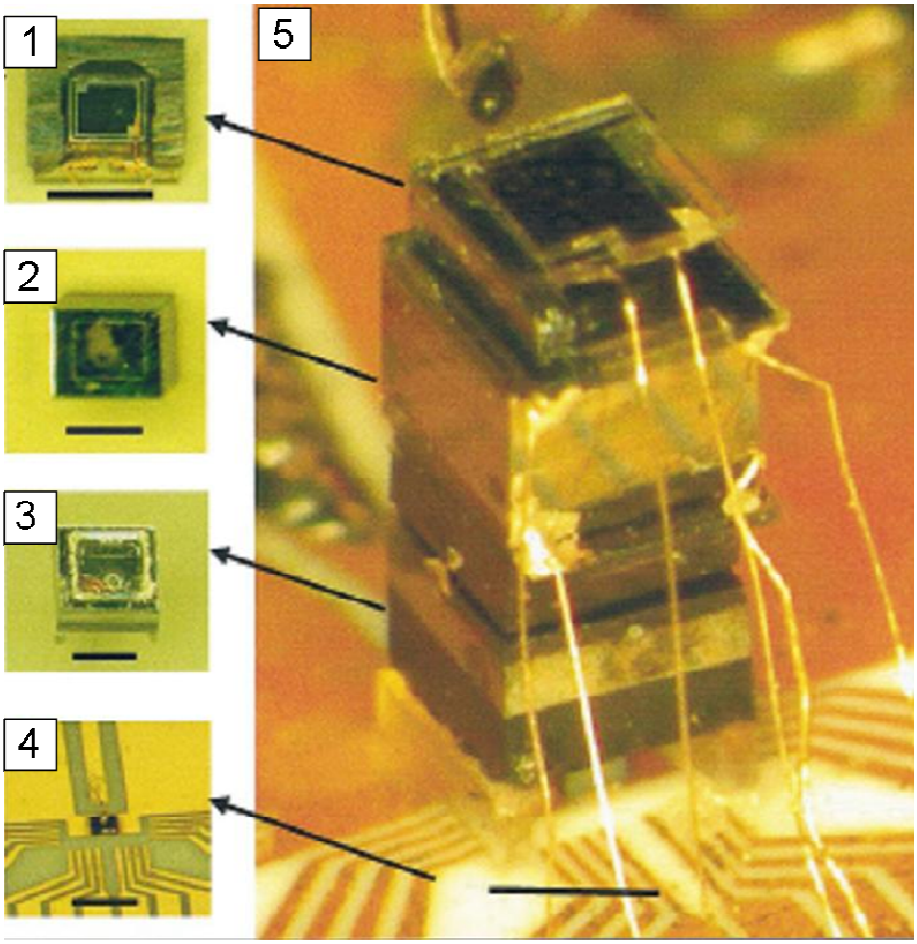

Figure 7: 'The microfabricated atomic clock physics package. Photographs: (1) photodiode assembly, (2) cell assembly, (3) optics assembly, (4) laser assembly, and (5) the full atomic clock physics package realized as a microchip. The black line in the photographs indicate 1 mm. (Adapted from ref[51]).

The complete package consists of four individual devices each with its own complex fabrication process. Each of the sub devices are then assembled together to form the finished single device. A detailed description of each fabrication process can be found in reference [52]. At the bottom is the laser assembly consisting of a vertical cavity surface emitting laser (VCSEL). This is a semiconductor laser diode where the emission is perpendicular to the top surface. Next is the optics sub assembly. This consists primarily of a spacer, filters and lens system. The main function is to attenuate the power, collimate the beam and set the correct polarisation. On top of this is the atom vapour cell. This is a cell created by etching silicon and bonding a layer of glass on both sides to create an enclosed cavity to confine the atoms. Finally

a photo diode detector is placed on the top to complete the integrated device. While this device is a big achievement in physics it is still not compatible for mass production devices. Currently each device is hand assembled one by one from the constituent sub devices. This is both time consuming and expensive and leads to a large inconsistency in the performance from device to device. In order to solve this problem the group are now working on creating the whole device in wafers that could then be bonded into a single large stack making it possible to produce 3000 clocks at a time on a 4 inch wafer.

2.2.1.1. Superconducting atom chips

Another interesting branch of atom guides is the use of superconducting materials. In 2006 one group successfully trapped rubidium atoms using a niobium superconducting atom chip [53] and this was followed by trapping a BEC in 2008 [54]. Another group used wires created by molecular-beam epitaxy-grown MgB_2 to create their superconducting chip [55]. Superconducting atom guides have a number of advantages over normal current carrying wires. They can create much more stable traps. Due to their zero resistance they produce no thermally driven noise and more stable current flows. This leads to trap lifetimes of 1000s of seconds being theorised [56]. Superconducting material are however expensive and difficult to fabricate. They also require high levels of cooling to enter the superconducting state. Both these factors make them less suitable for atom chip devices.

2.3. Optical elements on atom chips

Optical elements are fundamental to the functionality of all atom chips. The first step towards a working atom chip is capturing and trapping the atoms. This is done using an MOT. The use of MOTs and laser trapping is a field in its own right and so only a very brief outline of the workings of a MOT is presented here for the casual reader; for a more detail explanation, see reference [57].

An MOT uses a combination of both magnetic fields and laser beams to create the trap. The atoms are cooled by an exchange of momentum between the laser photons. The actual trap is created by using a detuned laser which is then split into three pairs of orthogonal, counter propagating beams, see Figure 8. This configuration allows atoms travelling in any direction away from the MOT centre to be slowed. This however only acts to reduce the atoms velocity and is not a position dependent force. An inhomogeneous magnetic field with zero field at the centre creates the position dependence needed to trap the atoms in one place.

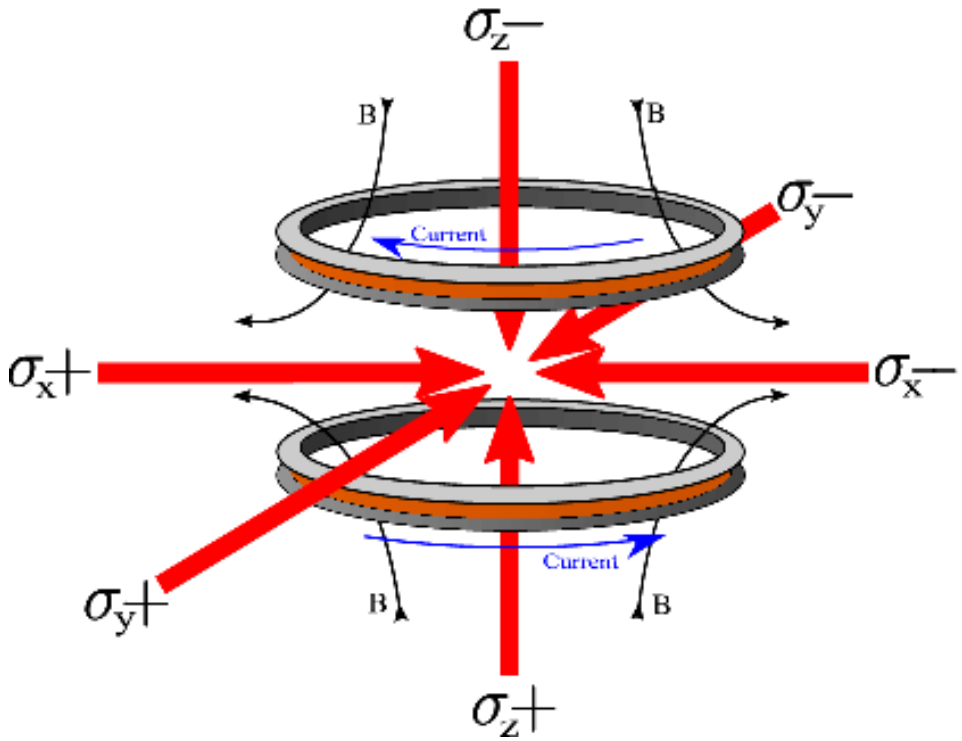

Figure 8: Configuration of the laser beams in a standard MOT. Six incoming beams create the optical component while the magnetic field is produced using two counter current propagating coils of wire (Taken from ref [58]).

A mirror MOT works on the same principles as a MOT but instead of six beams only four are used, see Figure 9. Two counter propagating beams shine along one axis as before but only two other beams are required. These beams are shone onto a mirrored surface and the reflections create the final two beams.

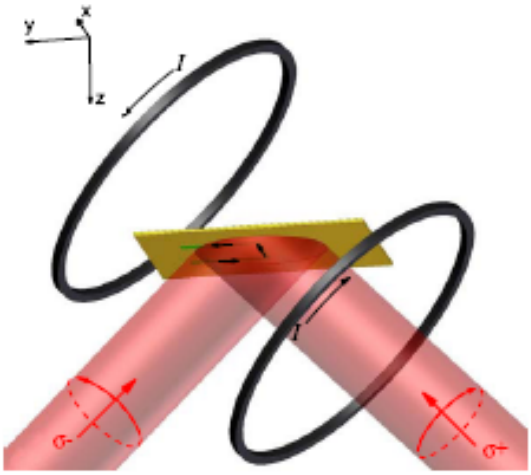

Figure 9: Schematic of a mirror MOT. The black rings represent large coils of current carrying wires while the yellow surface represents the reflective mirror used to create the mirror MOT. Two beams shown in the yz plane reflect on the chip surface while the other two beams (not pictured for clarity) propagate along the x axis parallel to the chip's surface (Taken from ref [59]).

A mirror MOT has several advantages over the traditional MOT especially for work with atom chips. The atom chip itself is not compatible with a standard MOT. The atom chip's substrate must not block the beam paths of the MOT and so has to be transparent. Also the loading of the atoms from the MOT onto the atom chip is difficult due to the small area of the micro trap. The solution to both these problems is to use a mirror MOT with the surface of the atom chip acting as the mirror. This allows the atoms to be cooled and trapped close to the surface of the chip making the transfer simpler.

Beyond the original move from using MOTs to mirror MOTs very little work has been done on improving the integration of this important step with atom chips. One group created a 'V' MOT using commercial polysilicon micromachining processing [60]. This consisted of two mirrors brought out of the plane of the wafer to form a V shape. Shining a laser onto this V shape produces four of the 6 required laser beams so reducing the MOT to a 3 beam system. It has however been shown previously that MOTs could be greatly simplified by using macro sized conical or square based pyramidal cavities [61]. In this work a novel yet simple MOT was presented that involved shining a single input beam into the cavity that automatically creates the 6 counter propagating beams required for trapping. This is a very promising technique that could easily be scaled down and integrated into a silicon wafer.

The other important requirement is detecting and manipulating the atoms. To be able to use single atoms as qubits for example individual atoms and their states must be readable. To select atoms with specific states either an optical field or state selective transforms of the trapping potential could be used [46]. Single atom detection is not new and has been achieved by many groups [62, 63]. These experiments used high finesse optical resonators made with extremely high quality concave mirrors but were performed on free atom clouds and are unsuitable for substrate based traps.

It is a relatively simple operation to allow photons to interact with large clouds of atoms however, to detect single atoms is a more complex task. A well focused light beam with the atoms present at the waist can detect as few as 10 atoms. In order to detect single atoms a more sensitive method is required. This is achieved using an optical cavity. This allows the photons to pass through the region containing an atom several times and therefore increases the interaction potential. In order to detect a single atom high finesse is not necessarily required as long as the beam waist is small. A high finesse is desirable for atom photon coupling which would allow two atoms to be entangled and therefore perform quantum logic operations [64].

One such cavity that could be used is a whispering gallery cavity. While such cavities have been shown to be capable of single atom detection [65], they are not highly suited to atom chips. In whispering galleries the light is trapped near the perimeter of a small sphere or disk allowing atoms to be coupled with the evanescent field that leaks out. While they have been shown to produce the highest Q factors measured in a resonator (>100 million) [66], they are closed resonators. This means the highest intensity part of the mode is inside the solid material of the cavity meaning atoms can only interact with the weaker evanescent field. This causes problems as atoms must be positioned accurately, very close to the surface.

Another type of cavity most commonly used is a Fabry-Perot (FP) cavity. The first instance of single atom detection on an atom chip was performed using this type of cavity in 2006 by Teper et al. [67]. To achieve this they used high reflectivity, low loss mirrors mounted on opposite sides of the chip to create a cavity. This work still makes use of macro scale components and therefore is not ideally suited for a microscopic device.

A simple method of creating a FP cavity is to bring two optical fibres together with dielectric mirrors on their ends. This was first suggested by Horak et al. in 2003 [68] and was first achieved on an atom chip by Quinto-Su et al. in 2004 [69]. They used two optical fibres chemically bonded onto the substrate. The method of alignment is not presented. In order to strengthen the coupling between the fibres a spherical lens is placed onto the input fibre as shown in Figure 10.

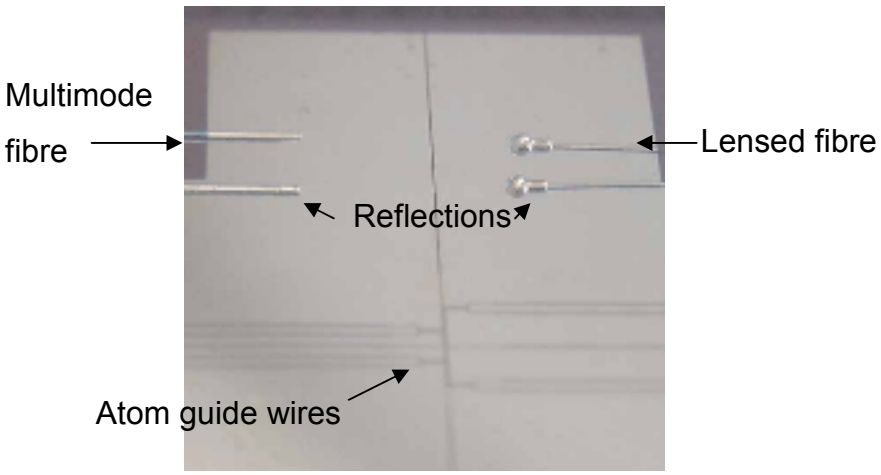

Figure 10: Configuration of the optical fibres. The lensed fibre is coupled to the laser and the multimode fibre takes the light into a photo-detector. The "fibres" on the bottom are reflections from the mirrored surface. The dark lines on the surface are the contours of etched wires. The separation between the fibers and the height are 4.5 mm and 0.6 mm respectively (Taken from ref[69]).

Liu et al. created a method for aligning two fibres accurately without etching into the substrate [70]. This can be advantageous in many situations where further processing becomes problematic on non planar surfaces or where aggressive silicon etches can damage pre fabricated structures. To achieve this, permanent SU8 structures were patterned using deep ultraviolet lithography to form a channel that could hold an optical fibre as shown in Figure 11. They claim an accuracy of 150 nm is achievable with this design though the only limit is the resolution of the photolithography. Further results shown in [71] demonstrated such a system could be used to detect single atoms.

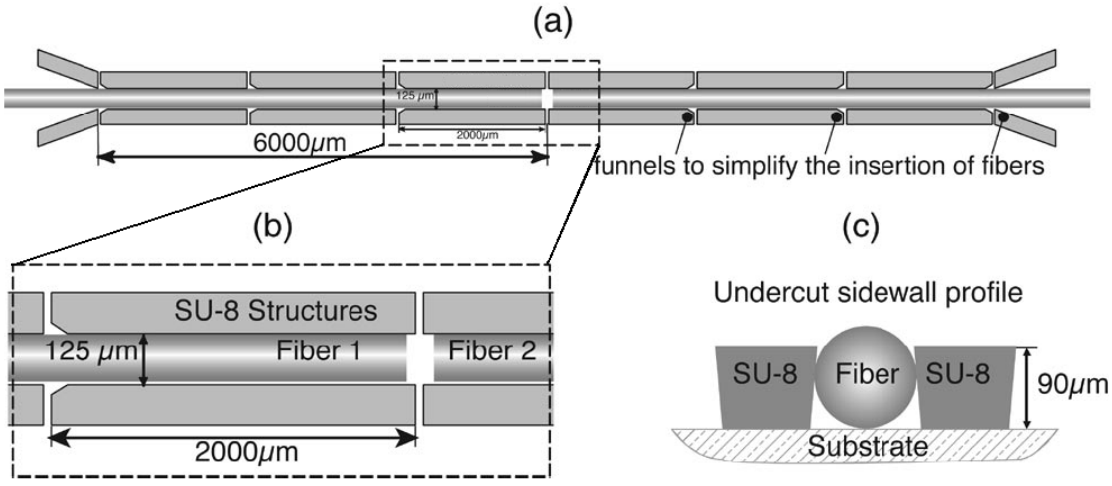

Figure 11: Diagram of the structure created in SU8 (a) shows the channel the fibre is placed into (b) showing the structure in more detail (c) showing the cross section view (Taken from ref [70]).

Another method currently being developed within our group at the University of Southampton is to microfabricate a single mirror into an atom chip substrate and use an optical fibre as the second mirror and input method [72]. The setup and cavity is shown in Figure 12.

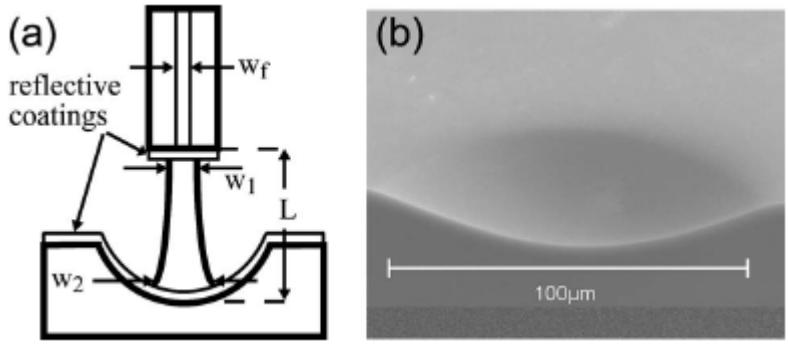

Figure 12: A Schematic diagram of the cavity where *L* is the cavity length and w_1 and w_2 represents the beam waist size. (b) Scanning electron microscope image of an uncoated mirror template cleaved almost across the diameter (Taken from ref [72]).

This method creates a microscopic cavity suitable for integration into atom chips as it uses standard microfabrication techniques. Using this technique, hemispheres of any size can be fabricated with surface roughness of 5 nm or less. The cavity is open allowing easy access to the cavity and is tuneable by the positioning of the input fibre. The positioning of the fibre and tuning is however difficult and requires external piezoelectric stage actuators. Other members of our research group have been

working on a solution to this by fabricating an electrostatic micro actuator for aligning and tuning optical cavities.

A 1D [73], 2D [74] and 3D [75] actuator has been designed and partially fabricated. The 1D actuator allows actuation within the plane of the substrate while the 3D actuator allows movement out of the plane. All the designs used electrostatic actuation for integration with atom chips. Results reported that the 1D actuator has 20 μm movement with a resolution of 2 nm being possible. For a full review of these actuators and their capabilities see the thesis of C. Gollasch [76].

2.4. Vacuum on chip

All atom chip experiments require high vacuum conditions. The initial MOT requires high rubidium vapour pressure approximately 10^{-8} torr to allow the capture of a large number of atoms. The evaporative cooling process needed to create a BEC requires an ultra high vacuum or $<10^{-11}$ torr. Creating such environments involves a lot of bulky complicated systems not suitable for a portable device.

These environments can be created using two methods. Firstly, using a double chamber system with both a vapour cell chamber and a science chamber [77]. This allows large numbers of atoms to be rapidly trapped; however, the equipment is large and complicated and therefore not suitable for portable devices for use in the real world. The second method is to control the pressure temporally [8]. This however does not decrease the size of the system as larger chambers are required serviced by equally large pumping systems.

One research group in the University of Colorado has put a lot of work into miniaturising the vacuum system to allow truly portable devices. The system they produced measures 30 x 30 x 15 cm and can maintain the ultra high vacuum required to produce a BEC as shown in Figure 13 [78]. Figure 13a shows the atom chip, chamber and vacuum pump system while b shows the chamber itself which contains both the atomchip and the atom dispenser. The atom chip itself forms one wall of the

chamber and with the use of through wafer interconnects removes the need for vacuum feed throughs for direct electrical connections. This represents a big step in miniaturisation and is a further step towards a portable device.

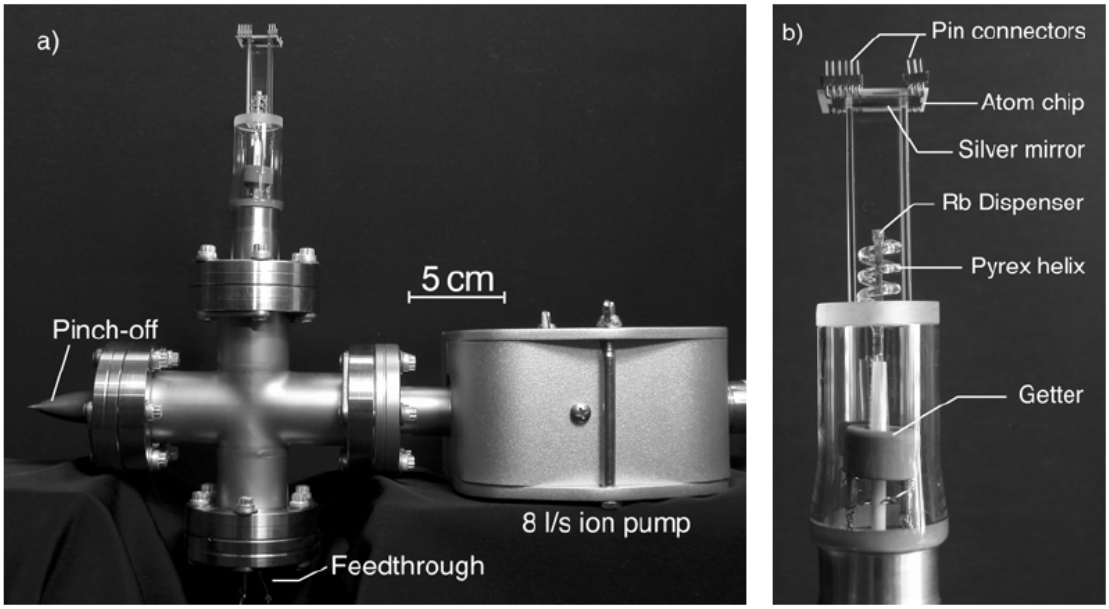

Figure 13: The first 'portable' vacuum cell for production of a BEC on an atom chip. a) shows the complete vacuum cell b) showing the cell itself in greater detail (Taken from ref [78]).

2.5. Overview of fabrication techniques for atom chips

Atom chips are manufactured using many techniques [37, 44, 79]. Many of these processes are standard MEMS techniques and so require no further explanation with reference to atom chips. In this chapter the various processes which are non-standard or require study and modification to be used in the fabrication of atom chips are described. An in depth look at electrochemical deposition and electrochemical deposition of photoresist is performed as these are two key processing steps in the chips that have been produced.

2.5.1. Resist coating

Lithography is a key part of all microfabrication processing; it is the method used to define regions and patterns on wafers where material needs to be selectively added or

removed. Lithography is mainly done using light sensitive photoresists which are usually deposited in liquid form using spin coating. However, photoresist can also be deposited by a wide variety of other methods. In liquid form it can be sprayed, dipped [80] or electrodeposited onto a wafer. It can also be deposited in dry form via lamination [81].

Creating 3D microstructures on silicon wafers with non planar surfaces often requires a uniform resist layer over varied topology. In such situations the traditional method of spin coating a resist often cannot be relied on to give this uniformity. Alternative methods such as spray coating and electro deposition of photoresists offer a solution.

2.5.2. Spin coating

Spin coating of resists is the standard and mature technique of resist coating a wafer. It uses commonly available equipment and resists. The wafer is held onto a spinner chuck by a vacuum and the wafer rotated. This rotation speed and time is dependent on the coating required but is typically at 2000-4000 rpm for around 30 seconds. This method relies on the centrifugal force created when the substrate is spun pushing the resist radially outwards. However, if the substrate is non planar due to an existing structure it can cause a physical obstruction to the radial flow resulting in poor, uneven coverage and often leads to striation. The extent of this effect depends on the size, shape and depths of the features.

Spin coating can be used on any substrate and the optimised process condition is generally well published and characterised. An example of a spin curve for determining resist thickness is shown in Figure 14. There are two main factors that define the spinning process, the viscosity of the resist and the thickness required. Manufactures often supply a spin curve for each resist giving the exact spin speed required for a desired thickness. The spinning itself often consists of a short slow speed spin to spread the resist over the wafer followed by the desired speed for a longer period to create a uniform film thickness.

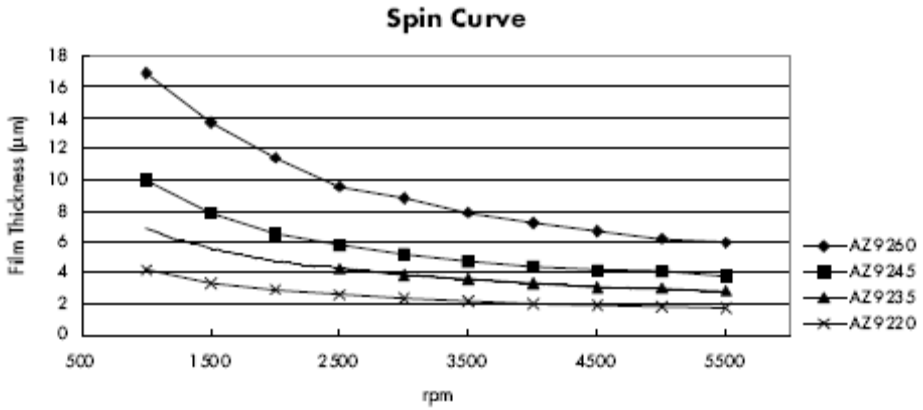

Figure 14: Graph showing the film thickness created using different spin speeds for the AZ9xxx series of resists (Taken from ref [82]).

2.5.3. Spray coating

Spray coating operates on a fundamentally different principle to spin coating. It works by spraying resist from an ultrasonic nozzle which creates micrometer size droplets. The droplets are propelled onto the wafer from the nozzle using clean dry air or nitrogen. During the coating process the wafer is rotated slowly (30-60 rpm) to produce minimal centrifugal force while allowing the spray head to evenly cover the whole wafer. To achieve a good droplet size distribution the resist must have a viscosity of less than $2x10^{-5}$ m^2s^{-1}. This can be achieved by diluting commercially available resists with solvents [83]. Spray coating can be performed on any substrate.

This method has several advantages over the traditional spinning method. It is economically more viable as it uses a lot less resist as no resist is spun off the wafer as with the conventional method. The resist thickness over the wafer is highly uniform and coverage of cavities does not suffer from the directional effect of spinning. While the coverage is better than when the resist is spun it is still not perfectly uniform. Figure 15 shows an example of spray coating resist onto non planar surfaces. At the bottom of cavities a small increase in thickness is often observed and a slight thinning at the top due to the effect of gravity on the resist. This effect can be amplified when cavities of different depths are present resulting in a thicker layer at the bottom of the smaller cavities.

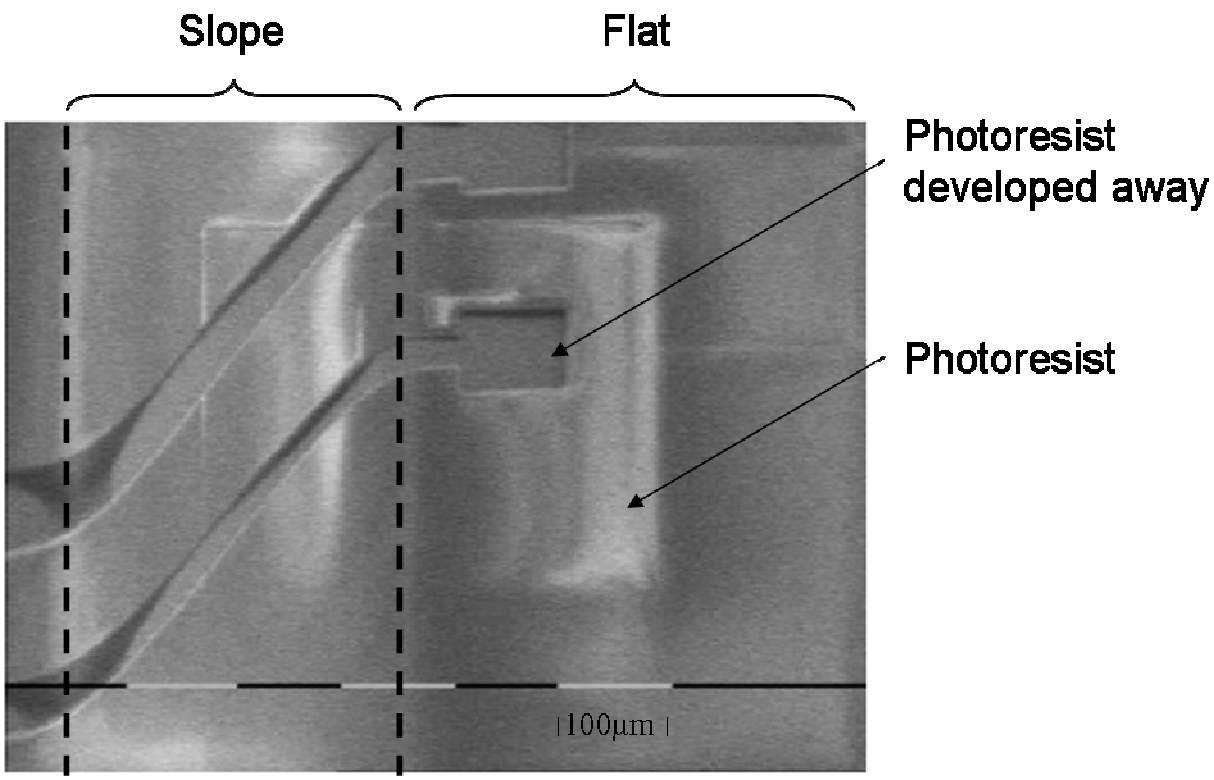

Figure 15: An SEM image of a cavity with spray coated resist covering the sidewalls showing resist thinning at the top and thickening at the bottom (Taken from ref [84]).

2.5.4. Electrochemical deposition of photoresist

Electrochemical deposition of photoresist was first developed for the printed circuit board industry [85] before being adopted for MEMS processing for creation of 3D microstructures. The method requires special plating equipment and solutions.

This technique produces highly uniform resist thickness over any geometry. Unlike spray coating, cavities can be coated with no variation between the top and bottom edges and no pooling effects are seen. Figure 16 shows an example of electrochemically deposited photoresist. It shows a much higher uniformity of thickness at the top and bottom of the slope compared to spray coating shown in Figure 15.

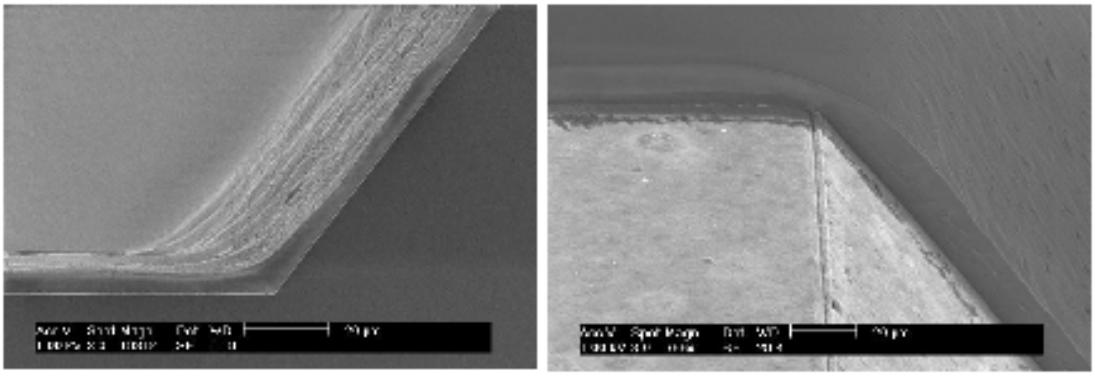

Figure 16: An SEM image showing electrodepostion of photoresist over a cavity wall. The image shows the bottom and top corner of the cavity respectively demonstrating little variation in thickness compared to other methods (Taken from ref [86]).

Using this method, complex patterns can be produced in and across cavities, opening up new possibilities for MEMS processing. Figure 17 shows an SEM image of the type of complex patterning that can be achieved inside a cavity with the help of electrochemical deposition of photoresist.

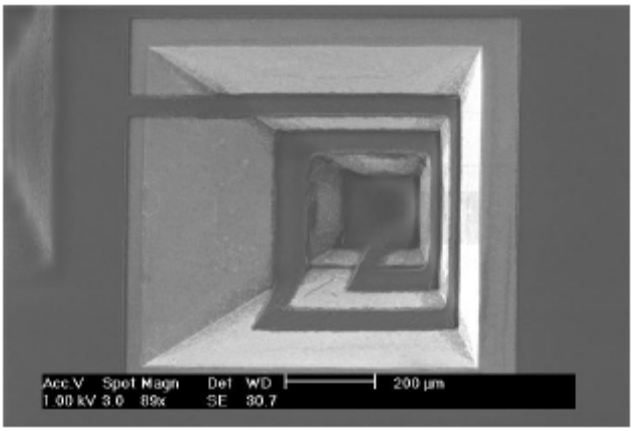

Figure 17: An SEM image of a pyramidal cavity with a patterned resist running along the angled side walls created using electrodeposition of photoresist (Taken from ref [86]).

The process works on the same principles as the electrochemical deposition of any metal with an anode and cathode required and a current applied to the system to initiate the reaction. The deposited film has a high resistivity and so as the film increases in thickness it hinders the current flow and therefore further deposition. Eventually, when the film reaches a set thickness the deposition will cease as no current can flow through the resist. This self limiting process creates highly uniform

layers even over complex topology. The maximum thickness is given by the voltage applied to the system.

The main drawback of this process is that it can only be used on conductive surfaces, such as metals, which can act as an electrode. It can not therefore be used on any devices where such a layer is not present or cannot be created.

Both positive and negative photoresists are available, such as the Eagle series from Shipley Limited [87]. The stability of the resist to future processing is dependent on the specific resist chosen. Generally negative resists are more stable to wet chemicals whereas positive resists are better in dry etch processes [88]. The negative resists are also generally tackier after deposition. This means they are not as suitable for contact lithography; however, topcoats have been developed to remove this effect.

The most important variables are the current/voltage applied and the temperature of the bath both effecting the thickness and quality of the layer deposited. Figure 18 shows how the deposited thickness is strongly dependent on the temperature of the bath for T<36 ^{o}C and to a lesser extent the voltage applied. Below 40 ^{o}C the thickness fluctuates significantly with small changes in temperature, therefore to obtain the best reproducibility of thickness a temperature of 35-45 ^{o}C should be used.

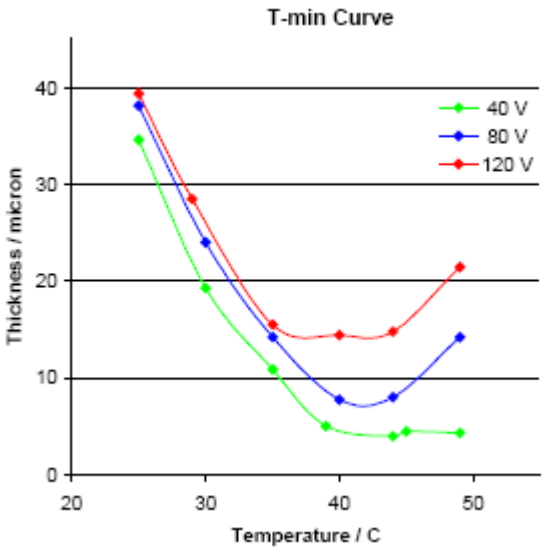

Figure 18: Graph showing the thickness of electrodeposited films at different temperatures and voltages (Taken from ref [89]).

The temperature also affects the adhesion; at low temperature the adhesion is weak (generally below 30 ^{o}C). Resist deposited below 35 ^{o}C also suffer from pinholes. This is due to hydrogen production during water hydrolysis; this then adheres to the wafer creating either a bubble or a pinhole. Figure 19 shows the relationship between voltage and thickness. The best overall linearity is in the range of 40-45 ^{o}C.

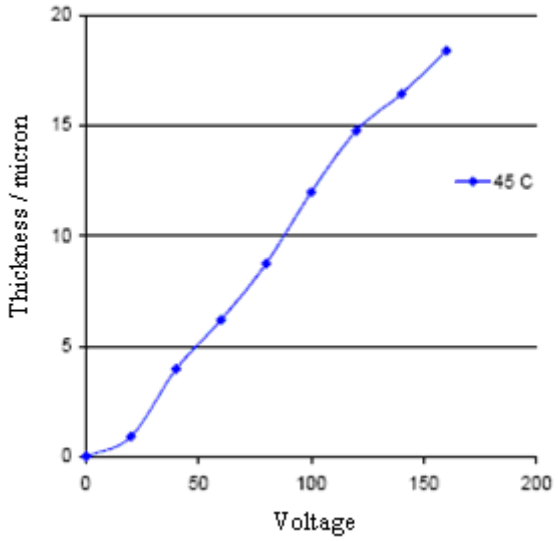

Figure 19: Graph showing the resist thickness as a function of applied voltage at 45^{o}C (Taken from ref [89]).

The bath requires constant monitoring and any acid produced by the ionisation process must be removed by ultra-filtration. This creates another constraint on the bath temperature. Above 40 ^{o}C the ultra filtration units used tend to deteriorate after prolonged use. With all these factors in mind, experiments performed in this thesis were run in a bath at 37 ^{o}C.

After deposition a prebake is required to remove the remaining water contained in the film. The prebake will tend to reflow the resist due a relatively low glass transition temperature [88]. This can help to remove any granules that have formed therefore smoothing out the surface and also close any pinholes and help the adhesion. However reflow can negate all the advantages of the process as resist flows to the bottom of trenches and away from sharp edges. Figure 20 shows an example of this reflow effect on the resist coating over corners and overhangs. It has also been shown that vacuum treatment has minimal effect on the reflowing of the resist and it is

independent of the vacuum pressure or time [88]. Care must be taken not to over dry the film by prolonged exposure (>1 hour) as this can cause the resist to become insoluble to the developer.

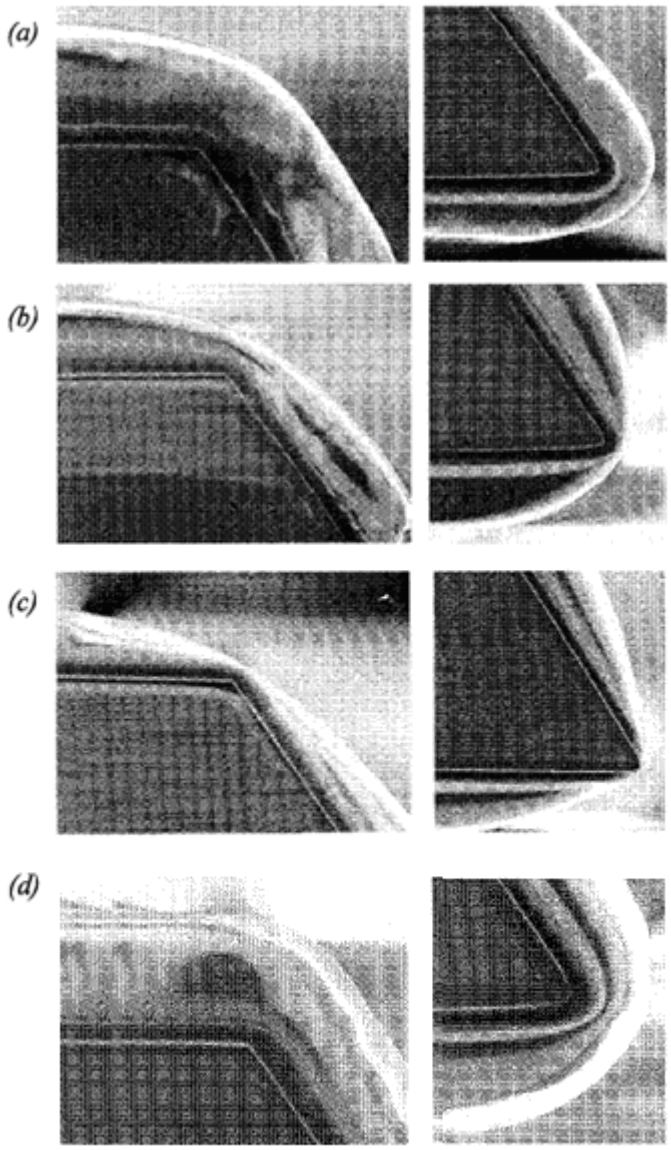

Figure 20: SEM image of an obtuse (left) and acute (right) corner covered in 12μm of electrodeposited photoresist, (a) before prebake (b) 25 minutes at 50°C prebake (c) 3 minutes at 80°C prebake (d) vacuum treated for 1 hour at 10^{-4} Pa (Taken from ref [90]).

Table 1 presents a summary for comparison of the three main methods for applying photoresist.

	SPIN COATING	SPRAY COATING	ED DEPOSITION
Process	Simple Difficult to automate process	Simple Possible for batch production	More complicated (equipment, solution) Batch production
Surface materials	Insulating or conductive	Insulating or conductive	Only on conductive layer Electrical connection to the wafer
Parameters	Viscosity Spin speed	Solid content of solution Resist dispensed volume Scanning speed Spray pressure	Voltage Temperature
Photoresist	Several commercially available types	Resist solution with viscosity <20cSt Use much less resist	Special ED resist Resist bath needs frequently refreshing
Resist uniformity	Difficult to control Poor reproducibility Dependent on position of cavities on the wafer	Controllable Reproducible Independent on position of the cavities	Reproducible and good uniformity (the best among three methods)
Suitable applications	Transfer patterns to the bottom of etched cavities. One level etched and large cavities are preferable	Transfer patterns to the bottom of etched cavities. Cavities with comparable size are preferable	Transfer patterns that run in and across cavities. Metal patterning are preferable

Table 1: A table summarising the three main methods used to apply photoresist

2.5.5. Electrochemical deposition of metals

Electrochemical deposition of metals is a very mature technology and in more recent years has changed from an art into a science. The invention of modern electrochemistry is widely attributed to the Italian chemist Luiigi V. Brugnatelli in 1805. Brugnatelli used a voltaic pile to facilitate the first electrodeposition. There is however speculation that artifacts found in Iraq dating to around 250 BC may have been the first examples of electroplating [91].

Electrochemical deposition has been widely used in the electronics industry for fabrication of printed circuit boards and is widely used in the CMOS industry particularly for interconnects. It can be used for both macro and micro structures and has become a common technique for MEMS fabrication [92].

Many metals can be deposited by electrochemical deposition and several elements can be co-deposited if one of the plateable elements is present. Recently alloys have also been deposited electrochemically and many are now commercially available. Figure 21 shows all the elements that can be deposited by this method.

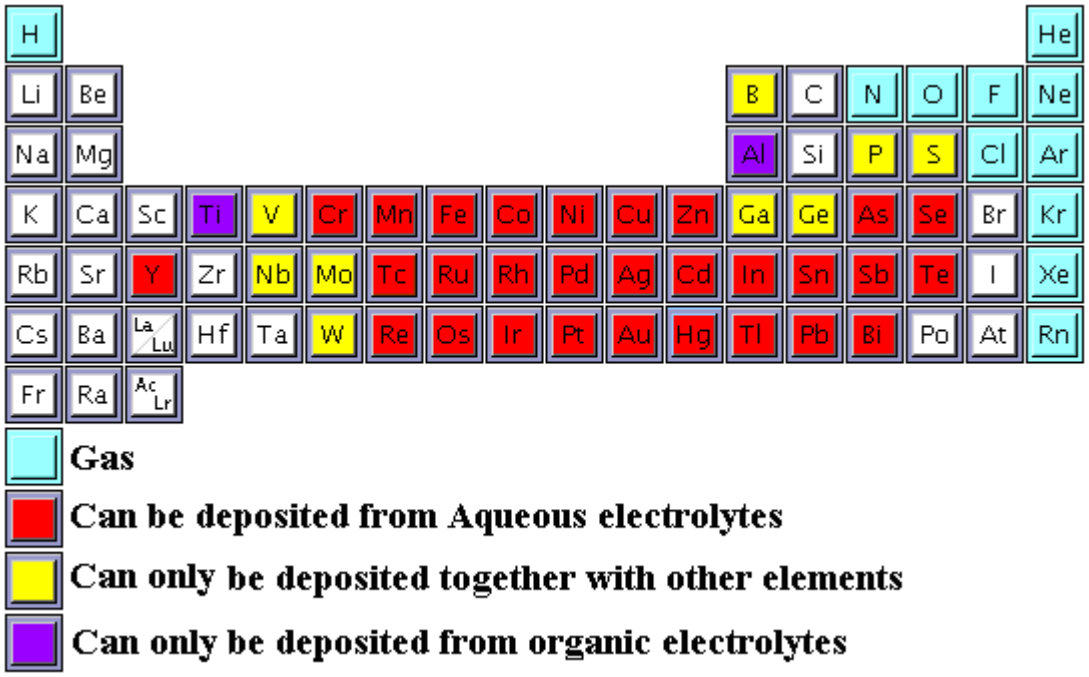

Figure 21: Periodic table showing the elements that can be electrochemically deposited, (Adapted from ref [88]).

Electrochemical deposition has several advantages over other methods of deposition. Electrochemical deposition is a relatively simple process. It does not require any high temperatures, pressures or radiation. It can be performed at room temperatures and at atmospheric pressure. This makes it both a cheap and safe process.

Electrochemical deposition produces high fidelity metal reproductions even with the use of high aspect ratio resist moulds and has a high deposition rate. It can also be used to produce a wide variety of properties such as composition, grain size and surface roughness. It is a reversible process for many metals with removal achieved by simply reversing the plating bias. It can also be used to create complex 3D topographies difficult and sometimes impossible by other methods.

Electrochemical deposition is performed, in its simplest form, by placing two electrodes connected to an external power supply into an electrolyte containing metal ions. It can therefore be performed in a beaker with standard laboratory equipment. The negative electrode is called the cathode and the positive electrode is called the anode. The deposition occurs at the cathode and is caused by the flow of positive ions in the electrolyte towards the cathode and the exchange of electrons at this interface.

Electroplating is characterised by a redox reaction, one element is reduced (gains electrons) while another is oxidised (loses electrons).

$$M^{z+} + ze^- \leftrightarrow M \tag{6}$$

The electrochemical deposition process always involves an electron donating reaction, left to right and an electron accepting reaction, right to left. However as free electrons cannot exist in the electrolyte a more accurate description is given by the half cell equation representing the reaction at each electrode, where M represents an element and z is the number of electrons (e^-) involved:

$$\begin{aligned} &\text{Left half cell:} \quad M_1 \leftrightarrow M_1^{z+} + ze^- \\ &\text{Right half cell:} \quad M_2^{z+} + ze^- \leftrightarrow M_2 \end{aligned} \tag{7}$$

The direction of this reaction can be calculated using the equilibrium potential E_{eq}. The equilibrium potential represents the potential at the electrode interface when no external power supply is connected and is described using the Nernst equation.

$$E_{eq} = E^o + \frac{RT}{zF} \bullet \ln \frac{[Ox]}{[\mathrm{Re}\, d]} \tag{8}$$

where E^o is the standard electrode potential, R is the gas constant, T is the temperature in Kelvin, F is the faraday constant and [] represents the concentration in moles per litre of the species. Table 2 shows a selection of standard electrode potentials.

Electrode-reaction	E^o (V)
$Na^+(aq) + e^- \rightarrow Na(s)$	−2.71
$Al^{3+}(aq) + 3e^- \rightarrow Al(s)$	−1.68
$Zn^{2+}(aq) + 2e^- \rightarrow Zn(s)$	−0.76
$Fe^{2+}(aq) + 2e^- \rightarrow Fe(s)$	−0.44
$Co^{2+}(aq) + 2e \rightarrow Co(s)$	−0.28
$Ni^{2+}(aq) + 2e^- \rightarrow Ni(s)$	−0.26
$Pb^{2+}(aq) + 2e^- \rightarrow Pb(s)$	−0.13
$Cu^{2+}(aq) + 2e^- \rightarrow Cu(s)$	+0.34
$Cu^+(aq) + e^- \rightarrow Cu(s)$	+0.52
$Ag^+(aq) + e^- \rightarrow Ag(s)$	+0.80
$Au^{3+}(aq) + 3e^- \rightarrow Au(s)$	+1.50
$Au^+(aq) + e^- \rightarrow Au(s)$	+1.69

Table 2: Standard electrode potentials E^o (Taken from ref [93]).

The potential of the whole cell is therefore given by:

$$E_{eq,cell} = E_{eq,right} - E_{eq,left} \quad (9)$$

Referring to equation 9, when $E_{eq,cell}$ is positive it means M_1 will be oxidised and M_2 reduced and when $E_{eq,cell}$ is negative the opposite is true. When an external power supply is connected the balance is shifted by creating an excess of electrons at the cathode and therefore creating a continual reduction of metal ions at the surface. This means current flows through the electrolyte. The bulk electrolyte will behave like a simple ohmic resistor creating a potential drop equal to $R \times I$ which is dependent on the electrolyte and electrode geometry, however at the electrode-electrolyte interface this no longer holds true. At this interface the situation becomes a lot more complex

as a diffusion layer and an electrochemical double layer, referred to as the Helmholtz double layer, are created.

The potential of the electrode is now given by:

$$E = E_{eq} + \eta \tag{10}$$

where η is the over voltage. The over voltage depends on many factors for example the current density, the amount of agitation, the reactions occurring at the electrode, the concentration and the temperature. The over voltage contributions can be divided into four parts each contributing a certain value; charge transfer η_{ct}, mass transport η_c, chemical reaction η_r and crystallisation η_{cr}.

The charge transfer is the rate at which electrons transfer from the metal to the ions at the electrode surface. This is determined by the electrode potential. The mass transport is the rate at which the ions can diffuse from the bulk solution to the interface. This depends on the concentration and agitation of the electrolyte. The chemical reaction rate is the rate at which the process itself can occur. If the chemical reaction is inhibited, such as if the ions are bound in complexes with water or other substances, this can hinder current flow. The crystallisation factor is the rate that the atoms can be incorporated into the crystal lattice. This depends on the concentration of absorbed atoms at the electrode surface and its morphology.

Depending on the situation one or more may contribute to the total over potential however generally the deposition rate is determined by the slowest contribution to the total reaction.

2.5.5.1. Throwing power

The throwing power is a measure of how uniformly the material deposits onto the substrate. In the ideal case the current distribution would only be a function of the local distance from the cathode to the anode. This model is very simplistic and only takes the electrode geometry into account. Such a model does not take into account

the effect of the over voltages and local fluctuation in the electric field. For example, the current density will be significantly higher at edges and protrusions than in recesses which will result in increased deposition thickness in these areas.

To counter act these effects so called current thieves can be used. These work by attracting part of the field away. They must be placed as close as possible to the area being plated, in this way the uniformity, consistency and quality of deposit will be very much improved [94]. Another method is to have a metal sheet with apertures in it which can be plated through. This must be connected along with the work piece and can help smooth the current density.

Alternatively the over voltages can be controlled to get the same effect. Electrolytes with a high concentration over voltage and high conductivity generally have a good macro scale distribution. This can be achieved by having either a low metal concentration together with low agitation (high diffusion over voltage) or a low temperature.

In contrast to get a good micro scale distribution a high metal concentration and a high level of agitation are required to ensure a good supply of ions into grooves and recesses. Therefore a balance must be found between the macro and micro distribution in order to electrochemically deposit on a wafer scale while still obtaining well defined microstructure features.

2.5.5.2. Stress

Electrochemically deposited gold films can be created with a wide range of stress values from compressive to tensile depending on the electroplating parameters. The stress for different types of baths also varies greatly [92]. As only non-cyanide sulphite baths are used in this thesis, only these shall be discussed here. The stress arises from a variety of sources including lattice defects and hydrogen inclusion in the deposited film [88]. The stress has been shown to be highly dependent on both the temperature and current density used [92].

2.5.5.3. Plating parameters

The electrochemical deposition process can be quantified using Faraday's laws of electrolysis [95]. Faraday's first law states:

"The amount of any substance deposited, evolved, or dissolved at an electrode is directly proportional to the amount of electrical charge passing through the circuit."

Faraday's second law states:

"The mass of different substances produced by the same quantity of electricity are directly proportional to the molar masses of the substances concerned and inversely proportional to the number of electrons in the relevant half-reaction."

Faraday's first law can therefore be written algebraically as follows:

$$w = ZQ \tag{11}$$

where w is the weight of a substance formed at an electrode, Q is the electric charge passed through the cell and Z is the constant of proportionality usually referred to as the electrochemical equivalent. The second law can be written as:

$$w_{eq} = \frac{A_{wt}}{n} \tag{12}$$

where w_{eq} is the equivalent weight, A_{wt} is the atomic weight and n is the number of electrons involved in the reaction. The electrochemical equivalent Z can be calculated using the Faraday constant F and the equivalent weight

$$Z = \frac{w_{eq}}{F} \tag{13}$$

Substituting equation 12 and 13 into equation 11 and rearranging gives

$$Q = \frac{wnF}{A_{wt}} \tag{14}$$

The weight of the deposit can be calculated using

$$w = \rho A h \tag{15}$$

where ρ is the density of the deposited material, A is the area deposited over and h is the height of the deposition. Substituting this into equation 14

$$Q = \frac{\rho A h n F}{A_{wt}} \tag{16}$$

As charge is simply a function of current (I) and time (t) as shown in equation 17, both of which can easily be measured during the experiment, the thickness of the deposition can be calculated at any specific time.

$$Q = It \tag{17}$$

The above equations assume that the only reaction occurring is the metal deposition at the cathode and therefore that all the electrons in the system are used in the process of metal deposition making the process 100% efficient. In reality other reactions occur such as the evolution of hydrogen at the cathode and oxygen at the anode. This results in a decrease in the efficiency of the process. This value can be calculated by comparing the actual amount of metal deposited M_a and the amount calculated theoretically from Faraday's laws M_t and is referred to as the cathode efficiency CE.

$$CE = 100 \times \frac{M_a}{M_t} \tag{18}$$

In reality this value can vary greatly and for example in nickel plating this value can often reach near 100% [96].

There are many factors that affect the properties of electrochemically deposited surfaces [96]. These include the current density, metal ion concentration, additives, current density, temperature, agitation, geometry and polarisation. Table 3 shows the effect each of these parameters has on the grain size of the deposition.

	Parameter	
	Low	High
Metal ion concentration	Smaller grains	Larger grains
Addition agents	Larger grains	Smaller grains
Current density	Larger grains	Smaller grains
Temperature	Smaller grains	Larger grains
Agitation	Smaller grains	Larger grains

Table 3: Effect of different parameters on the grain size in electrochemically deposited films (Taken from ref [96]).

2.6. Summary

As a result of the literature review, the pros and cons of different fabrication methods have been evaluated. In this research it was chosen to follow the approach of using methods suitable for batch processing, which are therefore suitable to producing manafacturable devices and not limited to laboratory or one off devices. Having reviewed the literature showing many different approaches towards creating atom chips our group has decided to concentrate on creating a new generation of chips that will be to combine multiple functionalities into a single chip. This integration will lead to the development of a multitude of devices from quantum computing to highly sensitive sensors, taking the atom chip from a laboratory experiment out into the real world.

Chapter 3

Atom Guides

In this chapter the first atom chip created in this work is presented. Atom chips are micro-fabricated devices which use electric, magnetic and/or optical fields to confine and manipulate cold atoms. An atom guide, the first step to creating an integrated atom chip, is presented. This is a form of atom chip capable of trapping and guiding cold atoms and is achieved using current carrying wires to create magnetic fields that can be manipulated to form various traps and guides. The flexible and accurate control of cold atoms that can be achieved with these devices makes them ideal for applications such as atom interferometry. First the design parameters and decisions are described. Then, three different methods used to fabricate a basic atom guide are discussed. Finally an atom guide capable of atom trapping is presented.

3.1. Design

3.1.1. Mirror magneto optical trap

As discussed in section 2.3, a mirror MOT is the most suitable method for creating the initial cloud of ultra cold atoms before they are placed into the atom guides. To enable the atom chip to act as a mirror MOT the surface of the atom chip must act as an optical mirror. This is achievable using an evaporated layer of gold. This layer however, must be as smooth as possible therefore limiting the processing that can be done to the areas requiring a mirror surface. Once the mirror has been created it must also be protected from any subsequent processing. A good mirror surface requires a high reflectivity value, preventing both absorption and unwanted scattering as both are detrimental to the atom trapping process.

3.1.2. Trapping atoms

Neutral atoms in a magnetic field feel a potential due their magnetic moment [11].

$$V_{Mag} = -\mu \bullet B \tag{19}$$

where V is the potential, μ is the magnetic moment of the atom and B is the magnetic field. If the atoms interact adiabatically with the magnetic field the potential V can be written as

$$V_{Mag} = \mu_B g_F m_F \mid B \mid \tag{20}$$

where μ_B is the Bohr magneton, g_F is the Lande g-factor and m_F is the magnetic quantum number.

It is this potential that is used to trap and manipulate the atoms close to the surface of the atom chip. The reaction of the atom to this field depends on its magnetic moment. If the atom has a positive magnetic moment it is repelled by a magnetic minimum; this is a strong field seeker. Conversely, if the magnetic moment is negative the atom will be attracted by a magnetic minimum; this is a weak field seeker.

Atom chips require the atoms to be trapped above the surface of the chip therefore the trapping potential must attract the atoms to a point away from the surfaces. To do this ^{87}Rb atoms are used in the weak field seeking state. Alkali atoms are usually used, as atom cooling techniques have mainly been perfected for these atoms. Rubidium in particular is used as it only requires moderate temperatures to obtain substantial vapour pressures and diode lasers that produce light at the required wavelength to interact with the element are quite inexpensive.

3.1.3. Trap configurations

There are two main trap types that could be used for confining neutral atoms, a quadrupole trap and an Ioffe trap [97]. The magnetic field profiles of both the quadrupole and Ioffe trap are shown in Figure 22a and b respectively. The quadrupole trap has strong confinement properties but contains a zero field point at its minimum. Atoms in such a trap remain confined as long as their magnetic moment can adiabatically follow the changing field direction and so stay in the trapped spin state. However at the zero field point atoms can undergo a non adiabatic spin flip, or Majorian transition, into an untrapped state and therefore become lost from the system [98]. The Ioffe trap however has a non zero confinement minimum therefore reducing any losses.

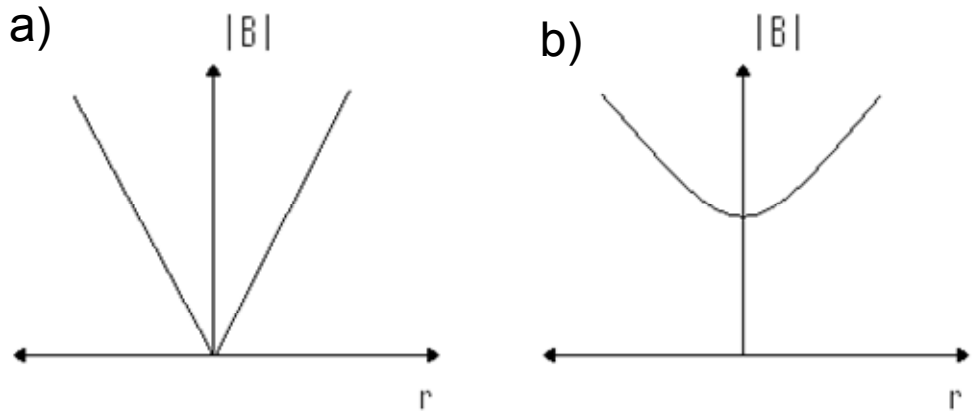

Figure 22: a) shows the spatial dependence of the magnetic field strength for a quadrupole trap and b) an Ioffe trap. The quadrupole trap has a zero minimum while the Ioffe trap has a non zero minimum.

3.1.4. Creating an atom guide

In order to trap these atoms a magnetic field minimum must be created. This is done using current carrying wires [15, 99, 100]. The magnetic field produced by a single current carrying wire is radial with the minimum situated at an infinite distance away from the wire (see Figure 23). All the following wire magnetic field figures are generated using Femlab and are for illustrative purposes only. A 2D wire was created and a current density J is set to be present inside the wire. The wire was set to have

the electrical resistivity of gold (2.4×10^{-8} Ωm). Gold is the material of choice in most atom chips because of its resistivity. The resistivity of the metal used has a great effect on the lifetime of the atoms trapped above its surface and gold produced one of the longest trap lifetimes[101]. It is also compatible with most MEM's processes. The magnetic field was then plotted with the colour showing the magnetic flux density.

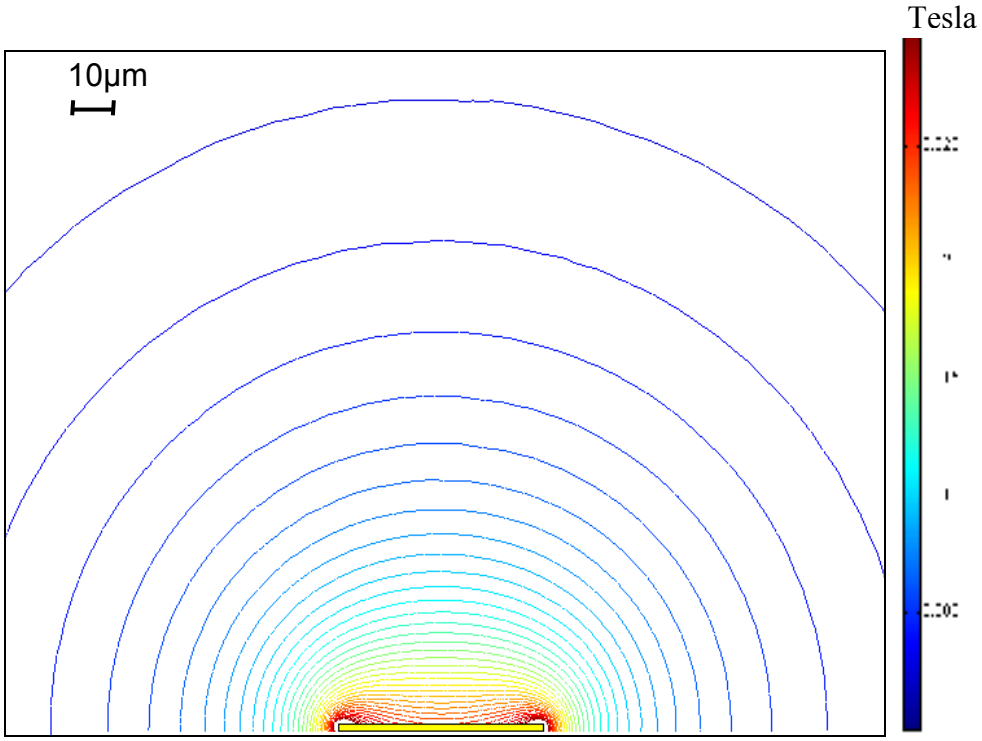

Figure 23: Magnetic field produced by a single current carrying wire. The wire has the same dimensions as the actual wires used on the atom chips produced in this thesis.

This arrangement would push the atoms radially away from the wire and so cannot be used as a trap. If an external field bias is then applied to the system a minimum can be created above the wire. Figure 24 shows the magnetic field due to a single wire and an external field applied perpendicular to the direction of the wire.

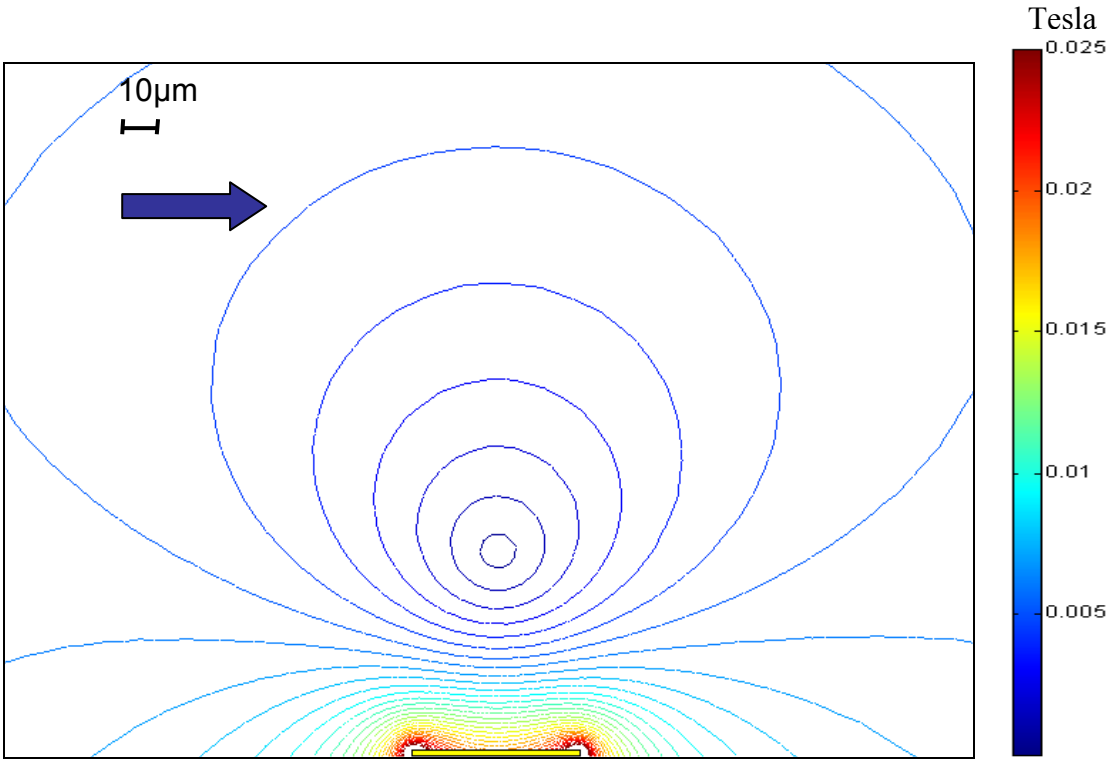

Figure 24: Magnetic field due to a current carrying wire with an applied external field bias (Blue arrow). The wire has the same dimensions as the actual wires used on the atom chips produced in this thesis.

Another set of designs use two wires. These wires can carry either co-propagating, or counter propagating current. Figure 25 shows the magnetic field when the wires are co-propagating. No external field is required as the minimum is created between the two wires. This design has the highest field gradient however it requires high relief wires which are harder to manufacture and are much harder to load with atoms.

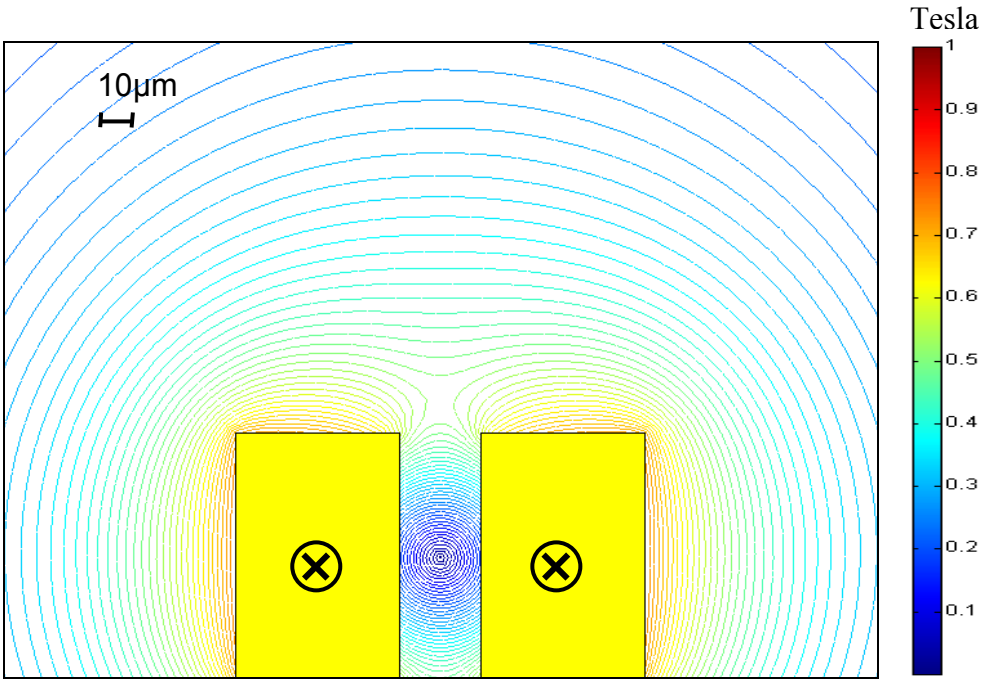

Figure 25: Magnetic field due to high relief current carrying wires.

Figure 26 shows two wires with counter propagating current. An external field bias is required to create a field minimum where atoms will collect but the minimum has a stronger trapping potential than a single wire.

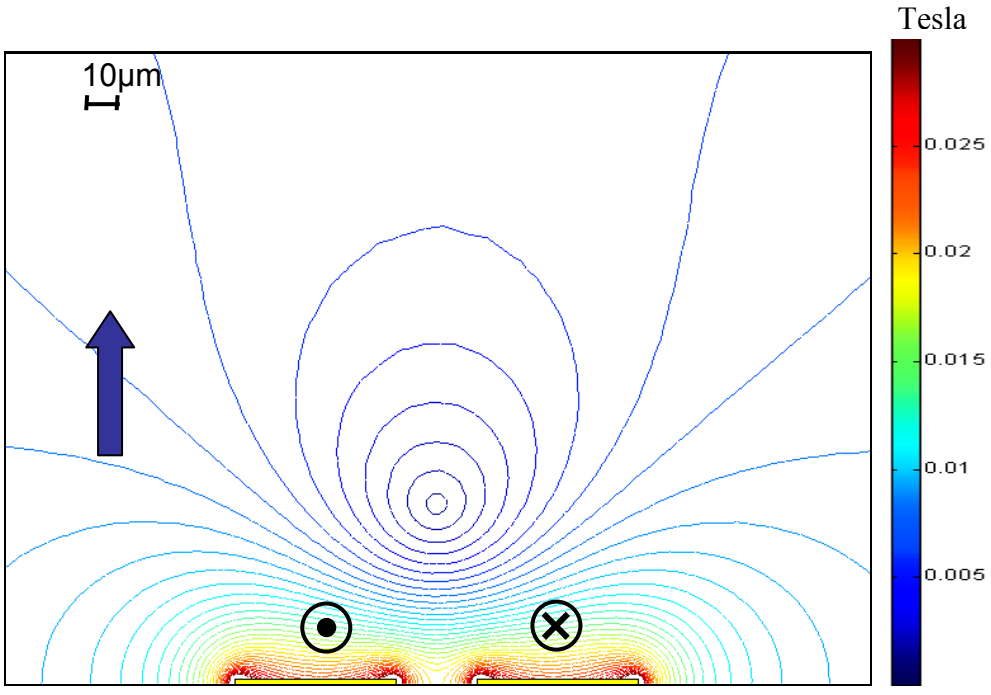

Figure 26: Magnetic field due to two current carrying wires with an applied external field bias (Blue arrow). The wire has the same dimensions as the actual wires used on the atom chips produced in this thesis.

Designs with a larger number of wires can create a minimum above the wire surface without the need for an external field bias. Figure 27 shows a design that uses three wires while Figure 28 shows a design that uses four wires.

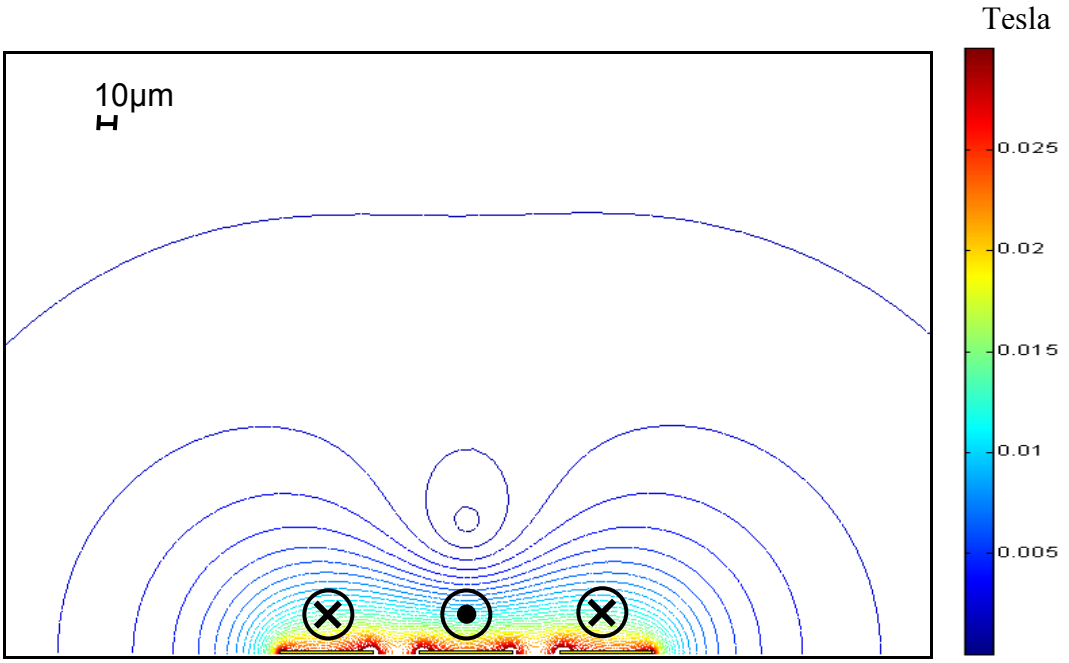

Figure 27: Magnetic field due to three current carrying wires. The wire has the same dimensions as the actual wires used on the atom chips produced in this thesis.

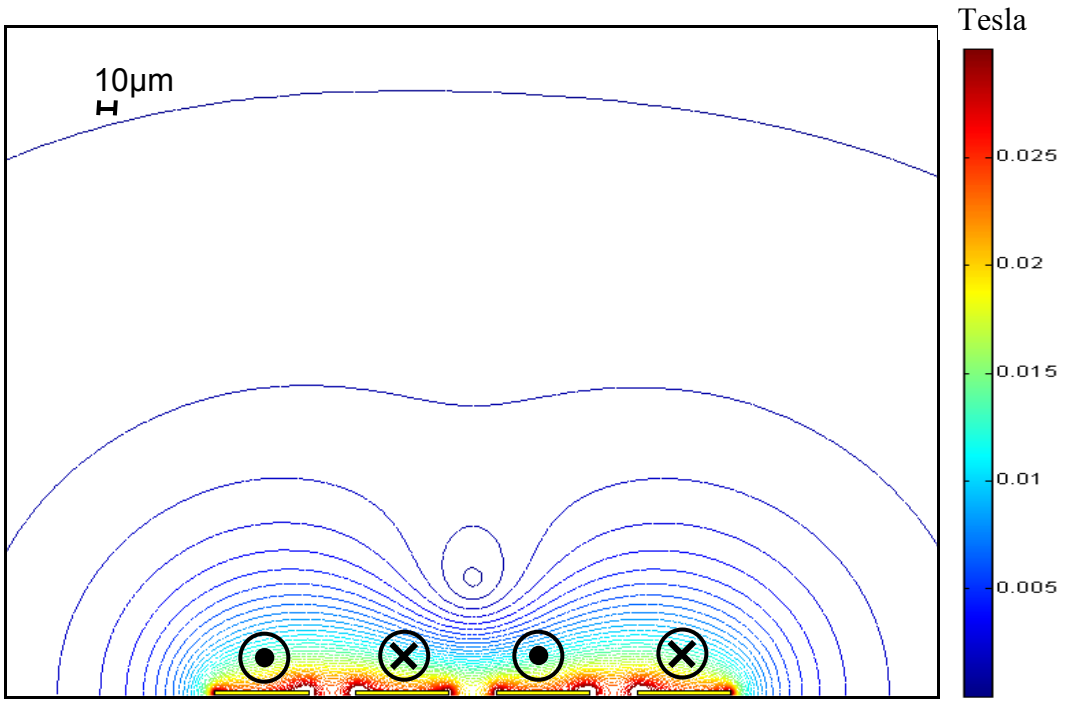

Figure 28: Magnetic field due to four current carrying wires. The wire has the same dimensions as the actual wires used on the atom chips produced in this thesis.

All the shown designs are suitable for creating atom chips. However the four wire guide is the most suitable for our applications. Four wire guides do not require an external field bias negating the need for bulky wire coils. Using four wires also allows for a finer control over the position of the guide by varying the current flowing in each wire.

3.1.5. Creating an atom trap

All these designs create a tube of minimum magnetic field and can therefore only act as an atom guide. Figure 29 shows how a single wire can be turned from a guide into a 3D trap. In order to function as an atom trap these ends must be blocked to prevent atoms escaping. This can be done by either bending the wire into a U or a Z shape.

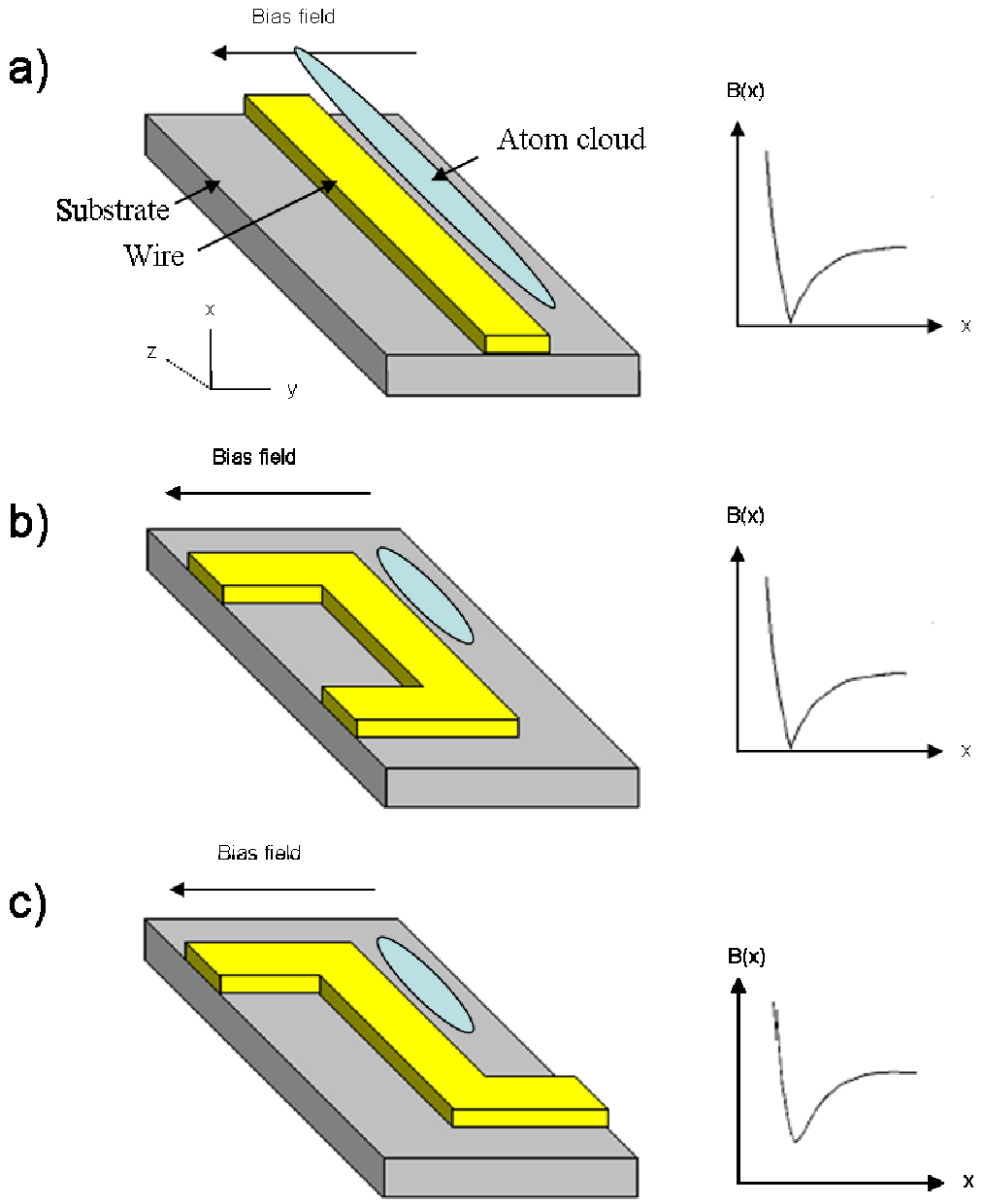

Figure 29: Figure showing the magnetic field created from a current carrying wire and an external field bias. The straight wire creates an infinite tube of minima (a). The U shaped wire creates a quadrupole trap with a stop on each end of the tube (b) and the Z shaped wire creates a Ioffe-Pritchard trap with the same stops (c) (Adapted from ref [15]).

Figure 29b shows a U shaped wire, the minimum is created to the right of the vertical wire. This bending of the wire causes the magnetic field to rotate by 180^{o} in each plane parallel to the plane of the U shape. This means if a homogeneous external field is applied there will always be a point where the fields cancel, creating a zero point. As previously stated this means a quadrupole trap is created which can cause atoms to escape.

Figure 29c shows a Z shaped trap. Here the magnetic field only rotates by 90 ^{o}. This allows an external field bias to be chosen that creates a potential with no zero points and is therefore an Ioffe-Prichard type trap [15]. This is the case when the external field is parallel to the plane of the substrate.

3.1.6. Trapping issues

The homogeneity and stability of trapped atom clouds have shown to decrease when brought close to the surface of the atom chip and the trapping wires. When loading the atom chip a fragmentation of the condensate is often observed [102-106]. This effect has been seen with chips produced by different fabrication processes such as; electrodeposition [104], machined foils [45] and permanent magnetic materials [107] and also with different materials such as copper [102], silver [45] magnetic video tape [107] and rare earth magnetic compounds [108]. The fragmentation increases as the condensate is lowered closer to the chip surface. It has also been shown that the cloud remains intact under optical confinement at the same height above the chip surface only fragmenting when magnetic trapping is used [104].

Three main phenomena have been identified as causing these instabilities; heating of the cloud [47], spin flip induction due to radio frequency noise [106] and corrugated trapping potentials due to non uniform current flow through the wires [109]. While the first two cause atoms to be lost from the trap it is the third one that creates the cloud fragmentation.

The heat generated by the wires comes from electrical resistance. The heat is mainly removed through conduction into the substrate as there will be negligible thermal radiation at the observed temperatures. This heating defines the maximum current that can be applied to lithographically fabricated wires and therefore the maximum trapping potential possible. In [79] it has been shown to be approximated by

$$I_{\max} = \sqrt{\kappa x y} \tag{21}$$

where x and y represent the height and width of the wire and κ is the thermal energy flow from the wire into the substrate.

Heating is also an obvious factor in the loss of particles from the trap. If the particles are heated to the point they have more energy than the trapping potential they will escape. One source of such heating is the compression of the atoms. The atoms are trapped above a room temperature atom chip giving off blackbody radiation. At large trapping heights the power produced at the resonant frequency of the atoms is low. When the trapping height is reduced to 10s of micrometres the atoms interact with the thermally fluctuating field produced near the surface which is usually at room temperature. This interaction can cause spin flips and therefore leads to loss of atoms [109].

Background collisions can also cause the loss of atoms. If atoms in the trap collide with background atoms the energy transferred can allow them to escape. This problem is reduced by placing the chip in increasingly strong vacuums.

Spin flips from low field seeking to high field seeking states can also cause the loss of atoms from the trap. Spin flips occur when the atoms experience a rapid change in the direction of the magnetic field. Their magnetic moment does not have time to respond and a previously weak field seeking state can be turned into a high field seeking state and therefore is lost from the trap.

Tunnelling can also cause atoms to escape from the trap. However, this effect can be easily reduced by increasing the distance over which the trapping magnetic field extends.

The fragmentation has been reported to be due to the local magnetic field inhomogeneity component parallel to the wire created by transverse components in the current density of the wire [102]. Theoretical work has been performed that attributes this to meandering in the current flow [109] and to the surface roughness in the wire edges [110]. The surface roughness of the side wall of the wires causes a non uniform current flow which, in turn, produced a longitudinal roughness in the magnetic field. It is this roughness in the potential that causes the atom cloud to

fragment. The amplitude of this potential roughening decreases with the height above the chip surface. The spectral density of this roughness shows decreasing bandwidth with increasing distance above the wires. This occurs as fluctuations of wavelengths smaller than the height above the wire at which the atoms are trapped average to zero [42]. It has also been shown that the potential roughness is mainly due to large wavelengths whose correlation length (ξ) is very large compared to the distance above the wire (d) [111]. It is therefore very important to minimise the side wall roughness in any fabrication process.

3.1.7. Practical limits

The wires fabricated for trapping atoms are typically rectangular in cross section with a greater width than height (aspect ratio less than one). The field of a long conductor such as these microwires can be approximated to be that of an infinitely long wire of zero height but non zero width w [100].

$$B(z) = \frac{\mu_o I}{w\pi} arc\cot\frac{2z}{w} = \frac{\mu_o I}{w\pi}\left(\frac{\pi}{2} - \arctan\frac{2z}{w}\right) \tag{22}$$

where z is the distance from the wire surface, I is the current and μ_o is the permeability of free space. For z«w the formula simplifies to:

$$B(z) \approx \frac{\mu_o I}{w\pi}\left(\frac{\pi}{2} - \frac{2z}{w}\right) \tag{23}$$

Meaning the surface field is:

$$B_s = \frac{\mu_o I}{2w} \tag{24}$$

This is therefore the maximum trap depth possible using a broad wire. Using equation 7 the gradient of the field is given by:

$$\frac{dB}{dz} = -\frac{\mu_o}{2\pi}\frac{I}{z^2 + (w/2)^2} \tag{25}$$

The gradient at the surface therefore gives the maximum field steepness achievable and is as follows:

$$B'_s = -\frac{2\mu_o I}{w^2 \pi} \tag{26}$$

Using the above equations it can be seen that to create the strongest possible trap for a given wire, the trap must be as close to the wire surface as possible, with the smallest wire width possible.

However other factors impose significant restrictions on the gradient. The most important of these are the maximum current density and the maximum sustainable power in the wires. The maximum power sustainable can vary greatly depending on the fabrication materials and the cooling methods used. A power of a few watts can be sustained without active cooling techniques providing there is a good thermal conductivity to a surface outside of the vacuum. Assuming a square cross section the total power (P) can be calculated using:

$$P = J^2 w^3 \beta \rho \tag{27}$$

where J is the current density, w is the wire width, β is the length to width ratio and ρ is the resistivity. For a wire of width 100 x 100 μm with a current density of 10^{11} A/m^2 the total power is therefore 22 kW. If the wire width is reduced at constant J the total power drops considerably.

Electromigration can also cause failure of the wires. This occurs when electrons transfer momentum to the metal ions. This causes the ion to move within the lattice and can create a void. Once a void has formed in the wire the local current density increases due to the reduced cross sectional area. This then leads to further electromigration and localised heating of the wire until eventually the wire breaks

down. The smaller the wire the higher the current density will become for a given current. This increases the chance of electromigration occurring. A full review of the effects and causes of electromigration can be found in ref. [112]

In many atom chip projects the magnetic field variance has set limits prescribed by the experiment itself. This variance V has been shown to be dependent on the surface qualities of the wire and can be expressed as [111]:

$$V_{\max} = 0.274\left(\frac{\sigma\xi}{d^3}\right)\left(\frac{\mu_0\kappa}{2\pi}\right)^2 x_0 \tag{28}$$

where σ is the root mean square (RMS) roughness of the sidewall of the wire, ξ is the correlation length, d is the height above the wire of the trapping point, μ_o is the permittivity of free space, and κ characterizes the heat flow across the interface between the wire and the substrate and x_0 is the thickness of the wire.

Using this formula the minimum distance the trap can be placed with respect to a wire's surface can be calculated as well as the maximum field gradient.

$$B_{\max} = \frac{\mu_o I_{\max}}{2\pi d_{\min}^{\ 2}} = \left(\frac{\mu_o \kappa x_o^{\ 1/2} V_{\max}}{0.568\pi\sigma^2\xi}\right)^{1/3} \tag{29}$$

3.2. Fabrication of microwires for atom guiding

Three methods are investigated for their suitability to fabricating gold microwires on atom chips. The fabrication processes are depicted in Figure 44 and Figure 47. Each method involves a thick deposition of gold which is either etched or grown into the pattern required for the gold microwires. The surface quality of wires is the main concern as previously discussed.

3.2.1. Electrochemical deposition into a mould

First electrochemical deposition into a mould is investigated. This technique is very promising due to its versatility and ease of integration into fabrication flows at almost any stage during the process.

The electrochemical deposition process must first be characterised to allow the best results to be achieved. Initially all tests were performed on unpatterned gold coated silicon wafers. To do this silicon wafers were taken and 600 nm thermal oxide was grown. A 40 nm adhesion layer of chromium was then evaporated onto the wafers followed by a 150 nm gold seed layer. This wafer was then cleaved into rough squares for testing the electroplating.

The electro deposition was setup as shown in Figure 30. The deposition was performed using a commercial cyanide free gold plating solution containing 10 g/dm^3 gold from Metalor. The initial results were performed using ECF60 and an additive E-3. The additive is a brightener designed to give better uniformity of deposition. However using this electroplating solution the deposits created contained large amounts of stress which led to lift off and peeling of the deposited films. A new solution ECF64 was then obtained from the same company which has been designed to produce low stress deposits. Initial results showed this to be true as no further lifting of the films was observed.

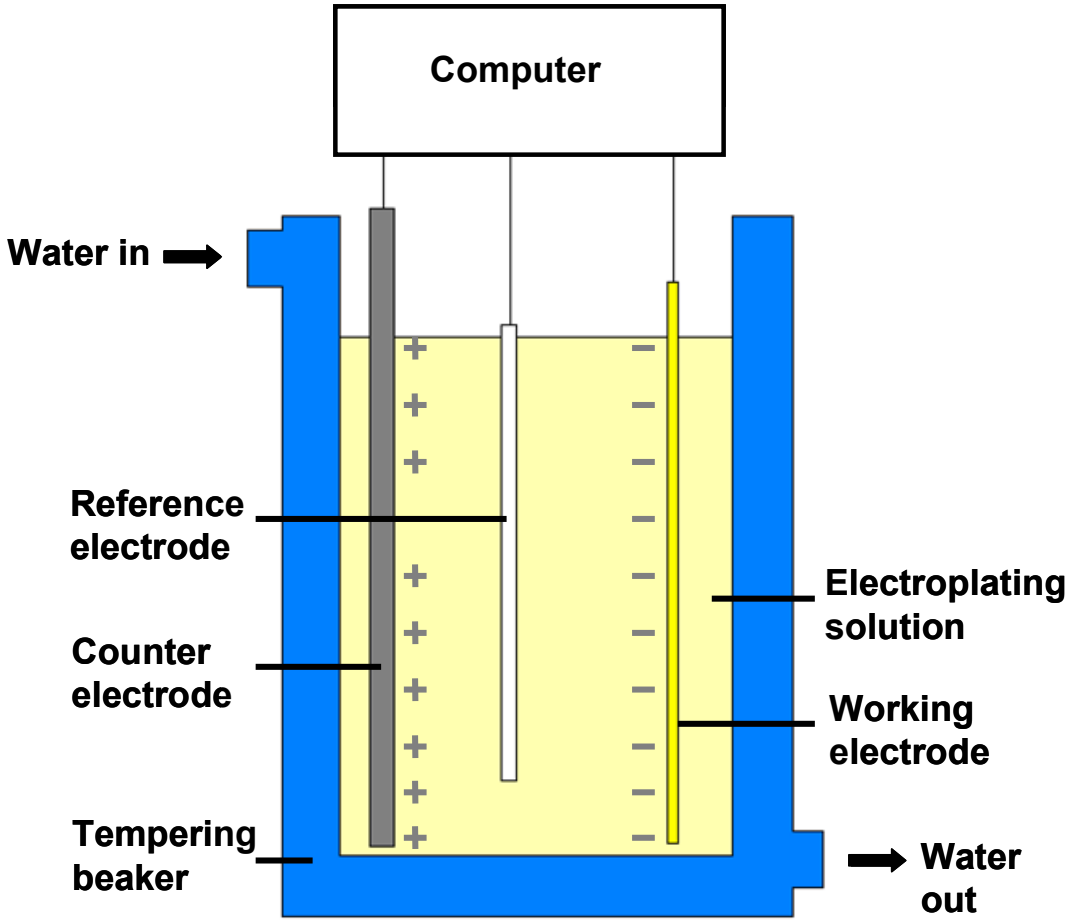

Figure 30: Image showing the electro deposition setup

Having produced depositions that were optically reflective and did not show signs of high stress, a more detailed investigation was performed. This was designed to find the best conditions for electrochemical deposition with respect to creating atom guides. This primarily meant creating as smooth a surface as possible; also the wire shape and profile is important as well as the optical reflectivity.

To perform these experiments four inch <100> silicon wafers were used as the substrate for all the electro deposition samples. A pattern used on an actual atom chip was chosen as the mask for the electro deposition. This mask contained wires of width 25 and 50 μm as well as bond pads (see figure 54 and table 6). To create the samples, the wafers were cleaned using fuming nitric acid. The wafers then had a 40 nm layer of chromium deposited by thermal evaporation. This layer is required to help the gold adhesion to the wafer. A 150 nm thick gold seed layer was then evaporated onto the chromium seed layer.

Next the electroplating mould was created. The wafers were spun with AZ9260 to create a 10 µm thick layer. The wafers were then exposed with the wire pattern. Finally the wafers were then cleaved into individual chips so they could be individually electroplated.

The electro deposition was setup as shown in Figure 30. All the depositions were performed using ECF64 gold plating solution containing 10 g/dm^3 gold from Metalor. A tempering beaker was used to control the temperature of the solution. This was attached to a FH16D digital flow heater from Grant instruments. This allowed the temperature of the water to be controlled while being circulated around the tempering beaker. This setup was chosen over a hot plate to reduce the convection currents produced which were found to cause variations in the deposition. The deposition was controlled using an Autolab PGSTAT30 [113]. A standard three electrode setup was used with a platinised titanium mesh counter electrode.

3.2.2. Results

In this section the results of the electrochemical deposition experiments are presented. The effects of stirring the solution, temperature and current density on the quality of the deposition are all investigated.

3.2.2.1. Solution stirring

Initially the solution was stirred using a magnetic bar placed into the beaker during deposition. It was however found that this had the effect of creating a peak on the side of the wire facing the direction of the fluid flow as shown in Figure 31.

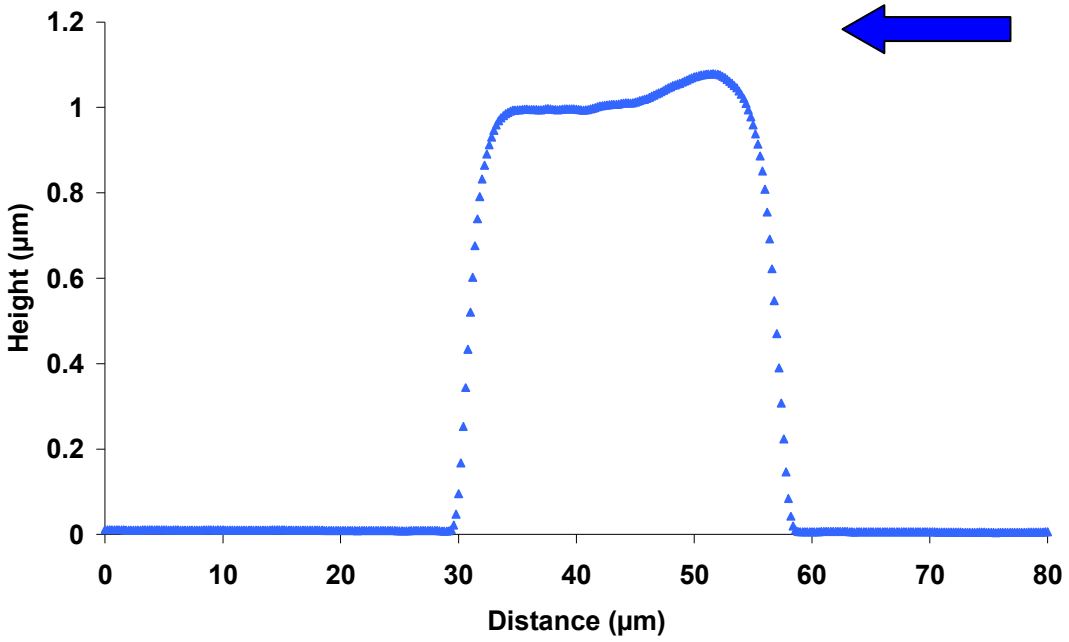

Figure 31: Graph showing a wire created by electro chemical deposition into a photoresist mould. The electroplating solution was agitated using a magnetic stirrer during the deposition. The arrow shows the direction of fluid flow.

This effect can be explained by the effect of mass transport. The concentration of the solution will be higher to the right of the wire. This is because deposition occurs as the solution flows over the wire surface therefore producing higher local deposition rates on the side receiving fresh solution. As the solution washes over the wire it will become slightly depleted causing a lower local concentration and therefore a lower deposition rate.

3.2.2.2. Temperature

The manufacturer states the optimum temperature for deposition is 50 ^{o}C. Using this as a guide, wires were deposited at different bath temperatures. The wires were then characterised to determine which was most suitable for atom chip wires. First the RMS roughness was measured using an Atomic Force Microscope (AFM). A 2 µm by 2 µm scan was used in each case. A typical scan is shown in Figure 32.

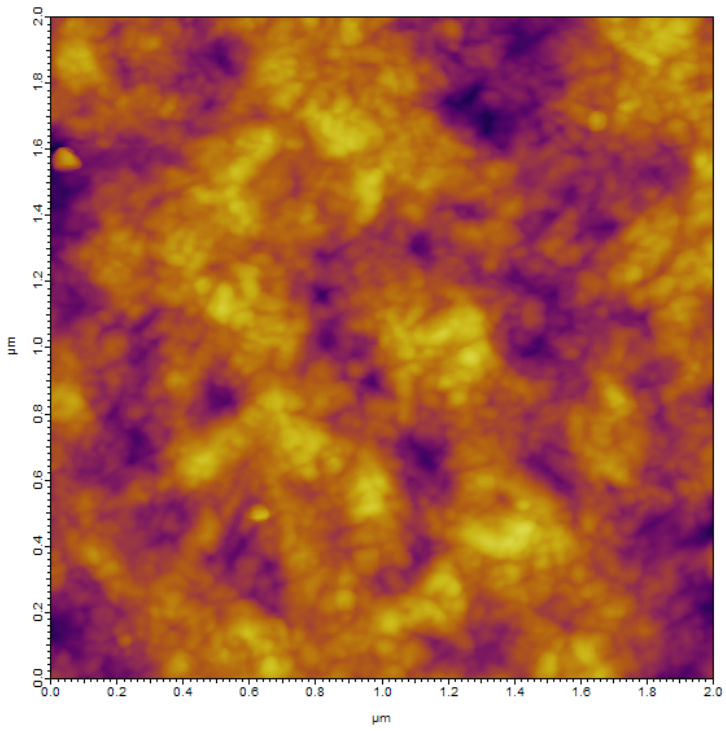

Figure 32: AFM scan of the top of a wire created by electrochemical deposition in a 40 ^{o}C bath

Each sample was measured in five different spots to obtain and average for the RMS roughness. The results are plotted in Figure 33. These results show that 50^{o}C had the lowest RMS roughness however due to the error in the measurement this temperate may not produce the smoothest wires in reality.

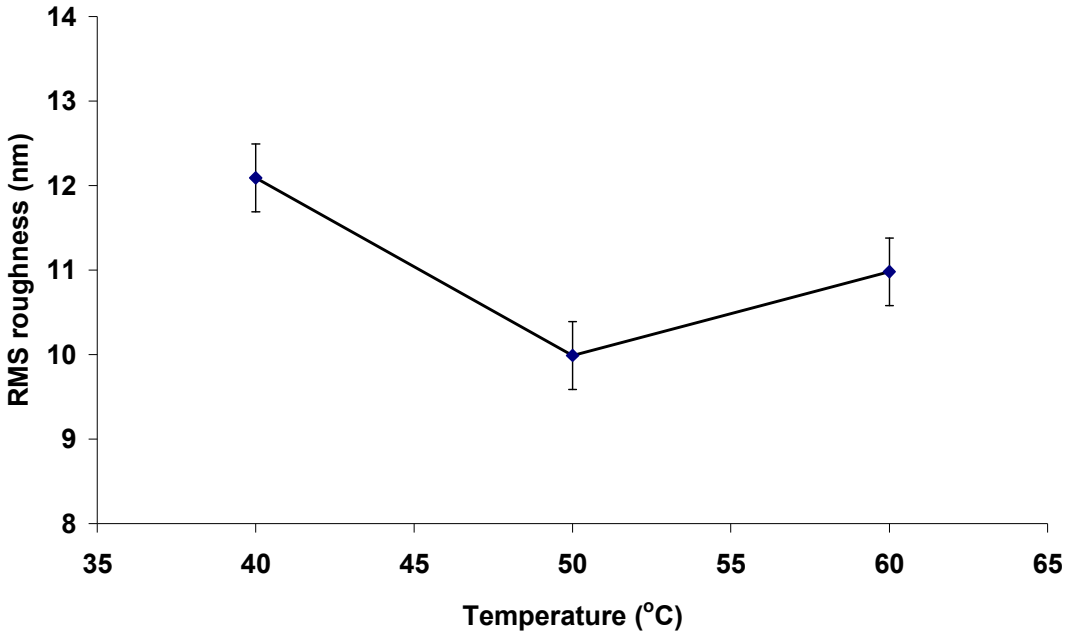

Figure 33: Graph showing the effect of deposition temperature on the roughness of electroplated gold.

Next the reflectivity of the gold deposits were measured using a Jasco UV/VIS/NIR spectrophotometer. First an evaporated layer of gold was measured to create a baseline for comparison. The reflectivity of all the samples were then compared to this value as shown in Figure 34. The results show the reflectivity of light with a wavelength of 780 nm which is the wavelength used for creating the MOT and trapping atoms in our experiments. Again, these results show that 50 ^{o}C create the best results. This is expected as smoother surfaces give better reflection.

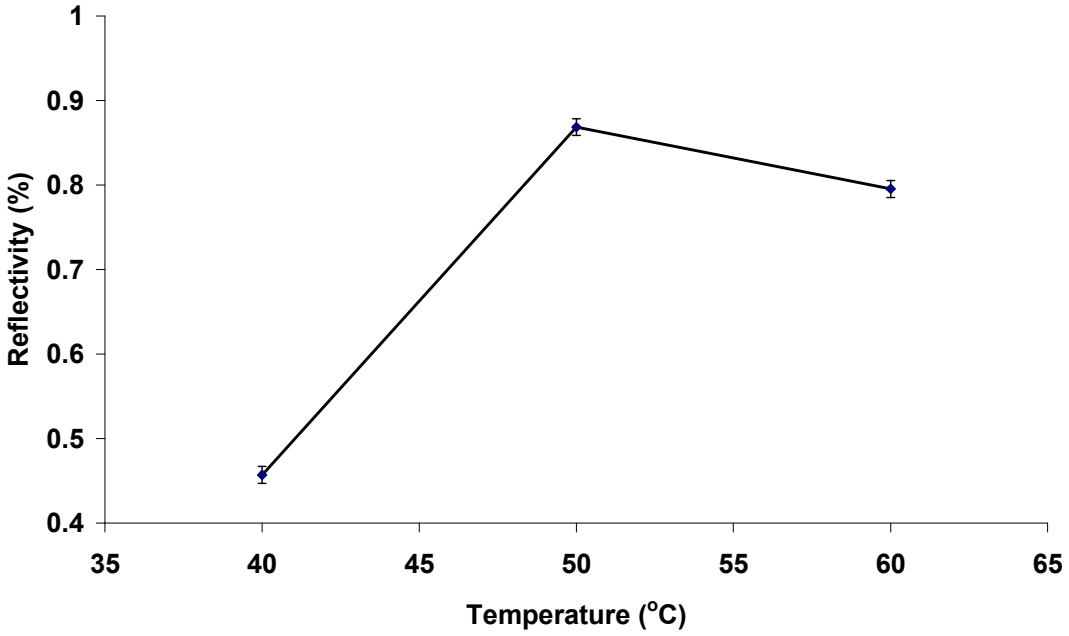

Figure 34: Graph showing the effect on the reflectivity of electro depositions at different temperatures.

Finally the height and shape of the top surface of the wire was measured using a KLA tencor P-16+ stylus profiler as shown in Figure 35. The top surface's shape is independent of the sidewalls shape, as the shape of the sidewall is also determined by the photoresist masks used. The ideal shape is a smooth square wire profile. The side walls of the wires cannot be examined using the stylus due to the profile of the tip. The tip itself is conical with a 60 degree tip angle and so the slope of the wire sidewall is just a product of the tip's shape. The difference in height is attributed to the current crowding effect which will be explained in section 3.2.3.

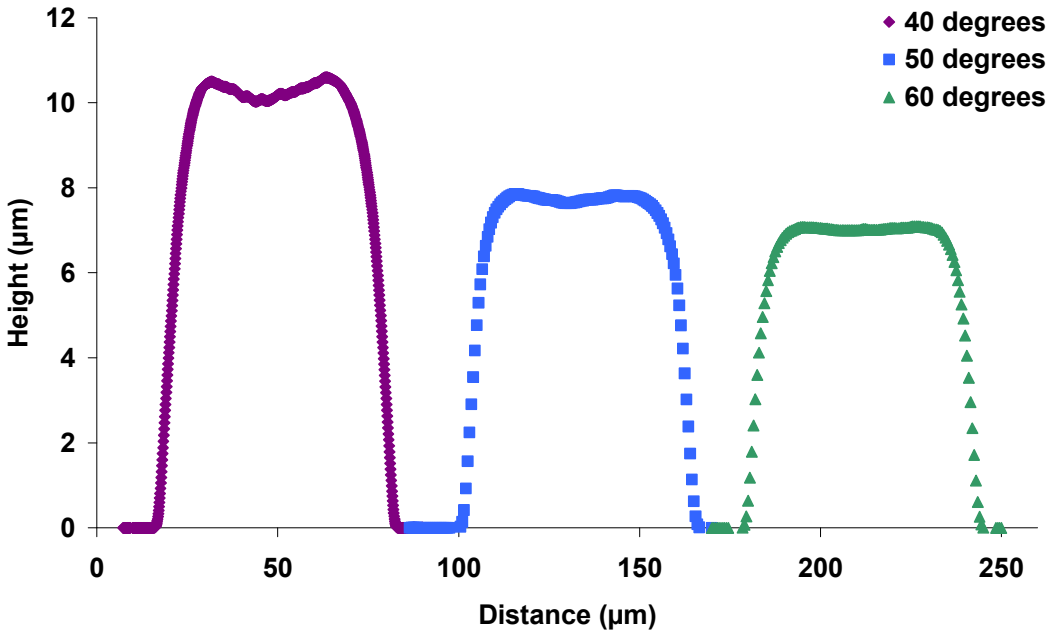

Figure 35: Graph showing the profile of wires created by electro deposition at different temperatures.

The wires also become flatter with increasing temperature. This is due to the higher temperature inducing higher thermal energies and therefore beginning to counter the effect of current crowding at the wire edges.

It should also be noted that while a higher temperature produces a thinner wire height this is not because the rate of deposition has decreased. The overall deposition rate over the whole wafer will in fact increase with increased temperature as predicted by [96]

$$\upsilon = \frac{k_B T}{h}\left(\frac{-\Delta G_e}{RT}\right) \tag{30}$$

where υ is the rate of the deposition reaction, k_B is Boltzmann constant, T is the absolute temperature, h is the Planck constant, ΔG_e is the electrochemical activation energy and R is the gas constant. Figure 35 only shows the wire heights and so the average deposition rate over the whole wafer can not be implied from these results.

All these results are in agreement with the manufacturers specifications showing that 50 ^{o}C gives the best quality results for each test performed. The shape profile

however does show an improvement with temperatures above 50 °C. The wires created at 60 °C show squarer profile with smaller peaks present at the edges. This is shown to be less important in section 1.2.4 as the shape is tuneable using the current density.

3.2.3. Current crowding

In order to gain an insight into the cause of the shapes found during electrochemical deposition of wires a Femlab simulation was created. All the dimensions were made to a scale based on typical values used during an actual deposition. The setup used is shown in Figure 36.

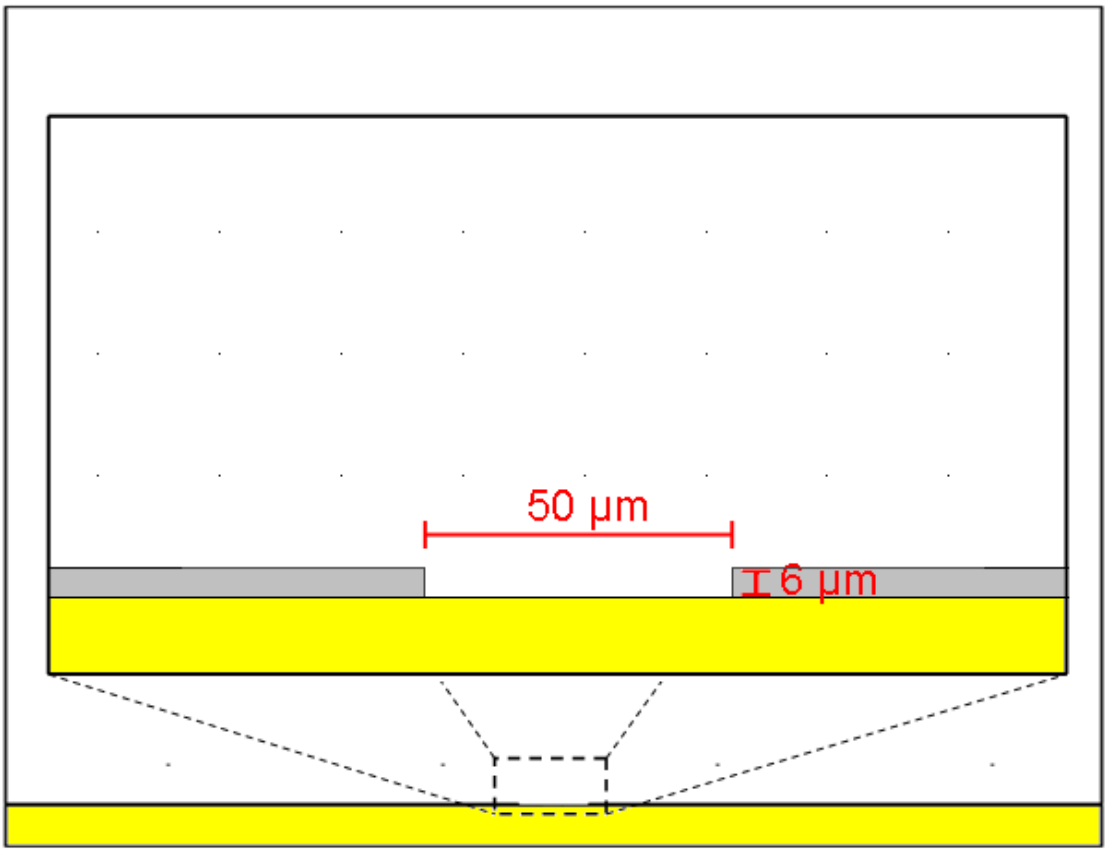

Figure 36: Figure showing the Femlab simulation setup. A large volume is used to represent the plating bath. The yellow box at the bottom represents the sample being electroplated and the grey areas represent the photoresist mould.

A large volume was first created and a voltage was applied to the bottom surface while the top surface was set to ground. This represents the two electrodes of a

simple electrochemical deposition setup. On the bottom surface a 6 µm thick insulator was placed with a 50 µm wide hole representing the openings present in the photoresist mask used to create a typical wire guide.

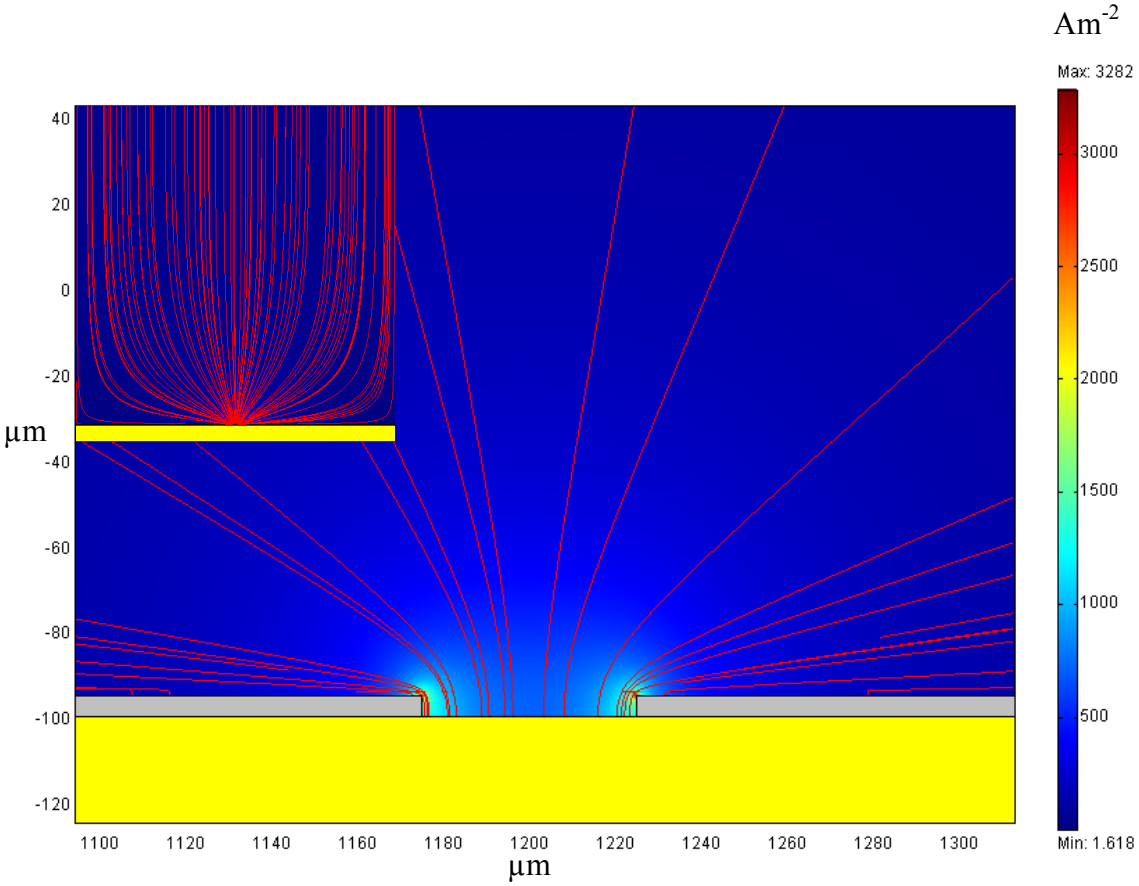

Figure 37: Plot showing a close up of the electroplating openings, the electric field lines are shown in red. The background colour represents the current density in the solution. Top left shows the whole simulated system. The slight non symmetry shown is present due to the opening not being exactly central in the simulation space as well as some anomalies with the meshing process used.

Figure 37 shows the results of the simulation. The insulating layer act to channel the electric field lines into the opening. This has the effect of creating a high field at the edges closest to large areas of photoresist. This means there will be a high current density and therefore a higher deposition rate in these areas.

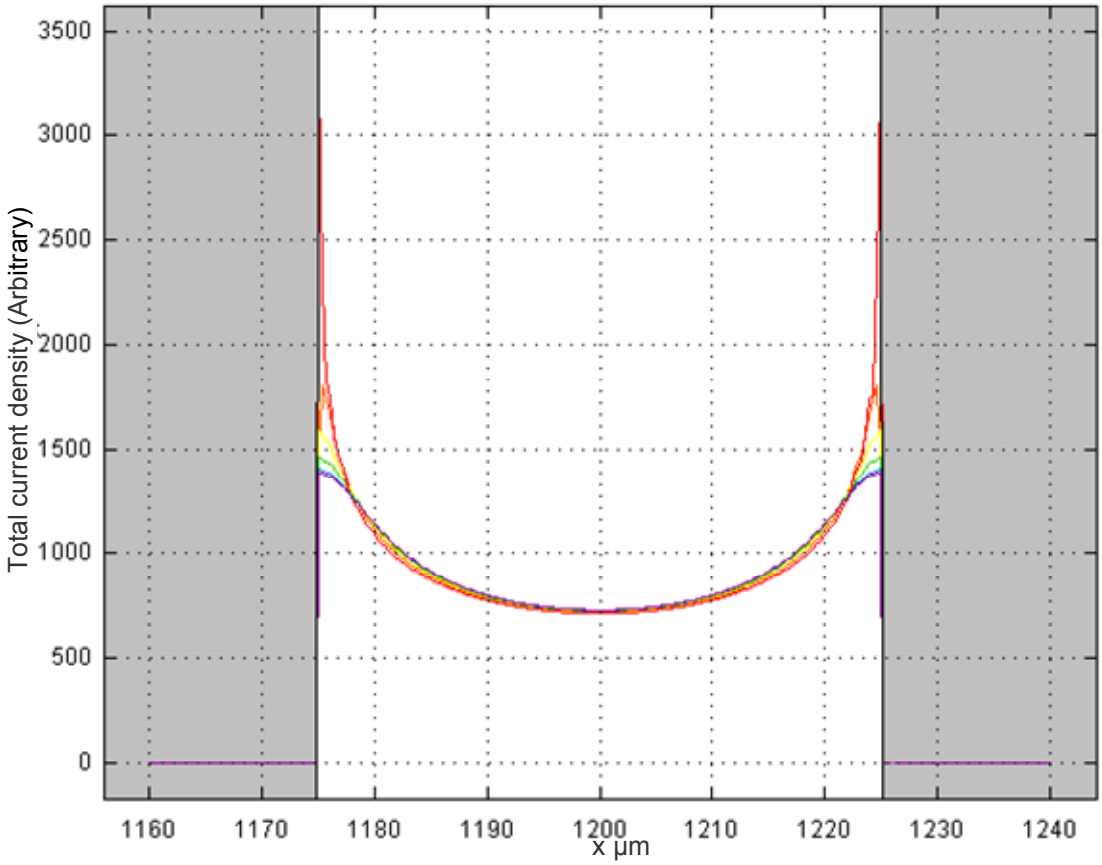

Figure 38: Graph showing the simulated current density as a function of position in a line on the charged surface (purple); 1 µm (blue), 2 µm (green), 3 µm (yellow), 4 µm (orange) and 5 µm (red) above the surface representing the wafer. The x coordinate corresponds to the position of the line in Figure 37. The grey area represents the area where photoresist is present and the white area represents the opening in the photoresist.

The simulated current density inside the wire mould is shown in Figure 38. This represents the current density in a line 1,2,3,4 and 5 µm above the wafer surface going from x-coordinate 1160 – 1240 µm. The current density is proportional to the thickness deposited as shown by the equation [114]:

$$d = \frac{i\eta tE}{\rho} \tag{31}$$

where d is the thickness, i is the current density η is the current efficiency t is the time E is the electro equivalent and ρ is the density of the deposited metal. This means

where the current density is high, a higher local deposition rate will also be present. This explains the peaks seen at the edge of the wires in Figure 35.

3.2.4. Current density

Next the effect of the current density was investigated. This was done by fixing the temperature of the bath at the previously determined optimum temperature of 50 ^{o}C. Figure 39 shows the effect of both time and current density on the electro deposition from the electroplating bath. The deposition rate is shown to be constant over time. As a constant current is used during the deposition process this follows the theory.

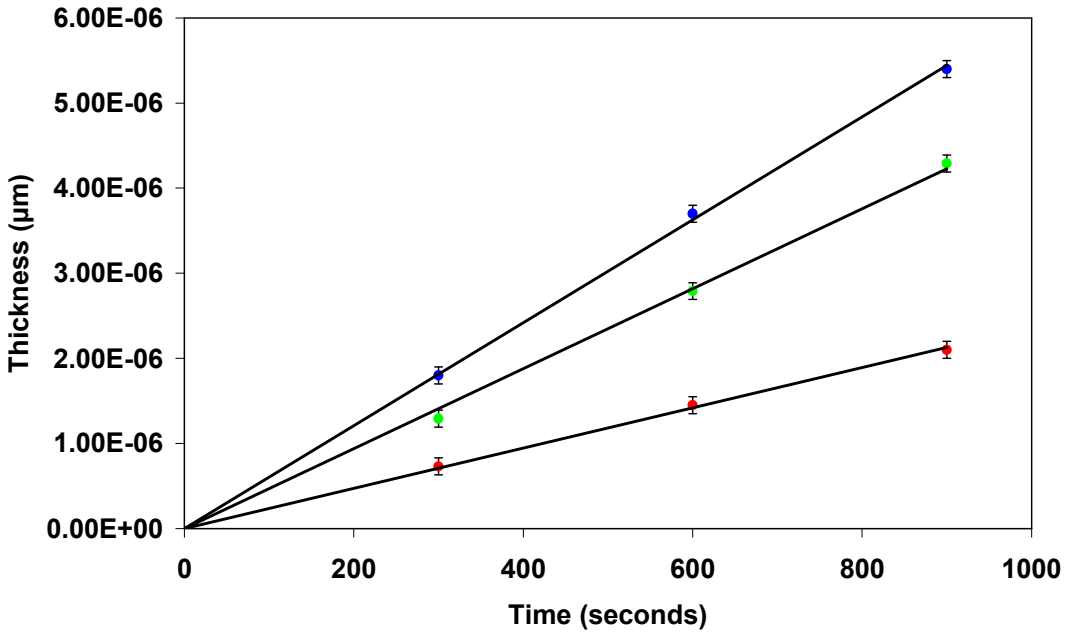

Figure 39: Graph showing how the thickness varies with time for different current densities; 23.1 A/m^2 (red) 38.5 A/m^2 (green) 46.2 A/m^2 (blue).

The effect of varying current density is also shown. The higher the current density, the thicker the deposition layer for a given time. This again is consistent with theory as the current density is directly proportional to the current and therefore the deposition rate achieved in the bath.

Figure 40 shows the effect of varying the current density in more detail. This figure shows the deposition rate against the current density. The deposition rate was calculated by simply measuring the height of the deposited wires and dividing by the total deposition time. This is then compared to the theoretical rate as calculated from Faraday's laws (see equations 11-16).

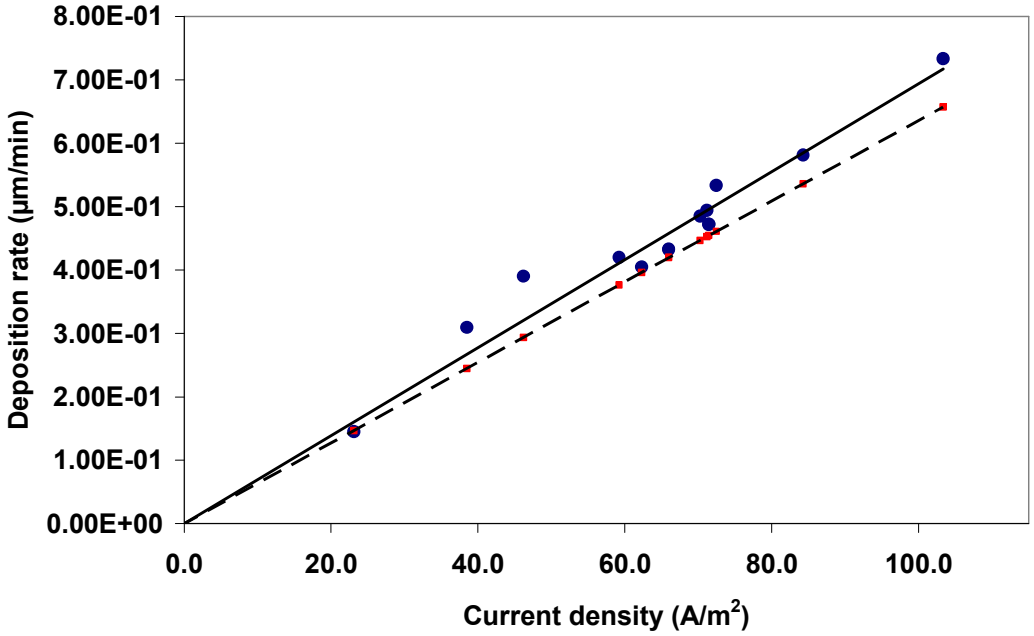

Figure 40: Graph showing the effect of the current density on the deposition rate of electroplated wires. The solid line represents a best fit line of the experimental data while the doted line is theoretical data.

The experimental results are in close agreement with the theoretical results however they do show a slightly higher deposition rate. This discrepancy comes from the method used to calculate the deposition rate. The deposition rate over the whole sample is not constant as it is dependent on the size of the features being deposited. Areas with small features show higher deposition rates than large open areas due to the afore mentioned current crowding effect. As the deposition rate was calculated by measuring the wire thickness it is expected that this will give a higher rate than the actual average rate over the whole wafer.

As with the previous samples the surface roughness and the reflectivity were measured as shown in Figure 41 and Figure 42, respectively.

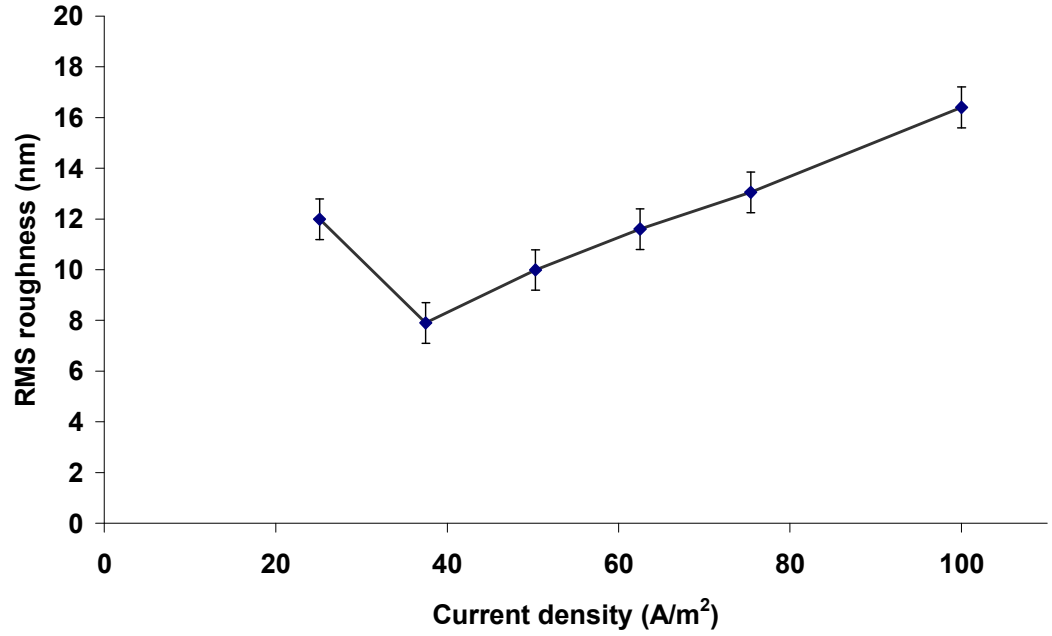

Figure 41: Graph showing the effect of the current density on the roughness of electroplated gold.

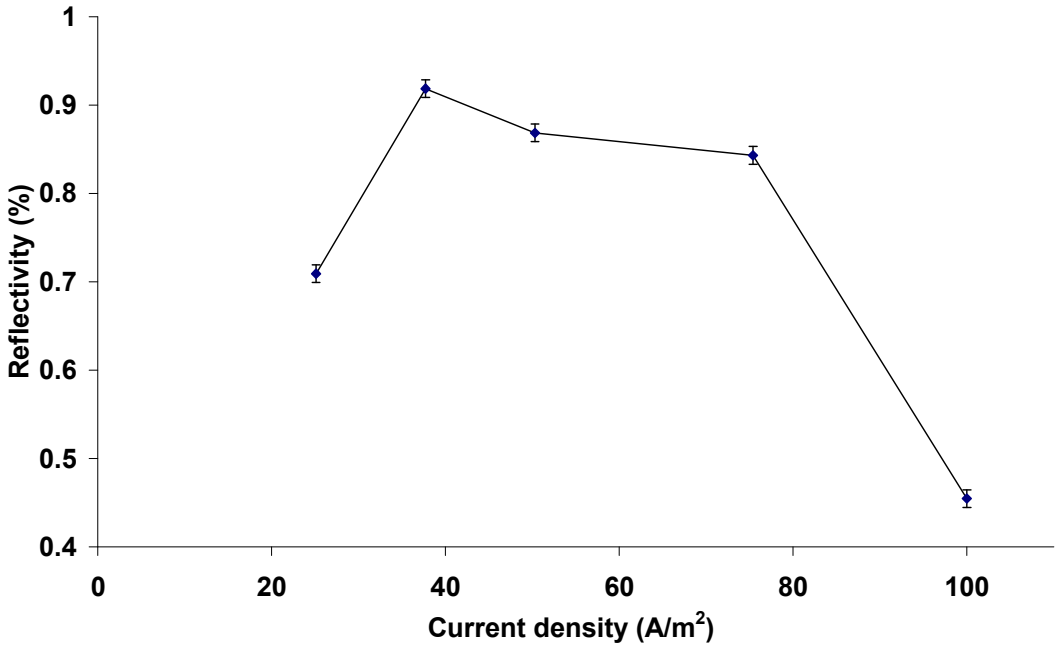

Figure 42: Graph showing the effect of current density on the reflectivity of electroplated gold at 780 nm.

Finally the shape was measured on a stylus profiler as shown in Figure 43. Here the effect of current density is clearly shown. At high current density the wires produced have highly peaked edges. This effect decreases with decreasing current density until the reverse effect begins to be seen. At low current densities the wires begin to take

on a humped shape with the middle growing thicker than the edges. In between these two extremes it is possible to produce a flat topped wire.

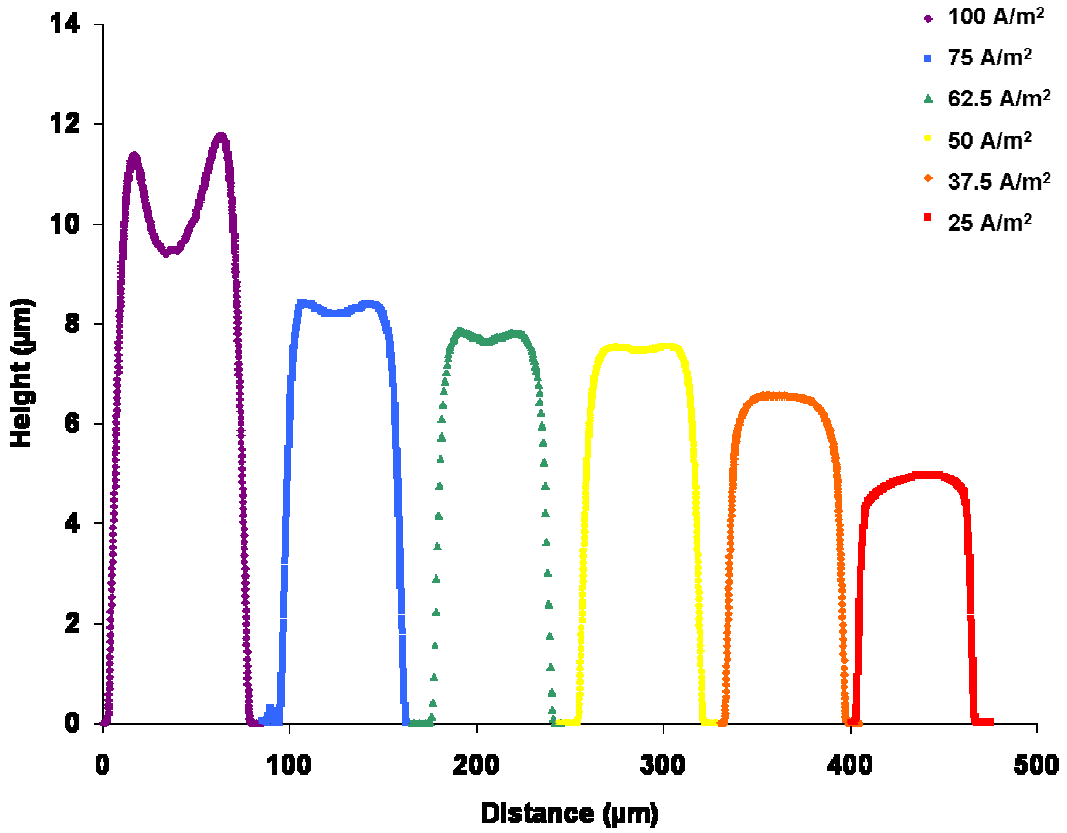

Figure 43: Graph showing the profile of wires created by electo deposition at different current densities. Each wire was electroplated at a different current density.

At higher current densities thicker wires are produced than those at lower current densities. This corresponds to the data shown in Figure 40 and is exacerbated by the current crowding effect which increased with higher currents.

All the optimisation performed on the electroplating process was done using single parameters. A more accurate method would be to use multi parameter optimisation as this takes into account that the parameters are interdependent. This would result in a truly optimised process. However the method presented in this thesis produced wires capable of performing all the functions required and so further the optimisation presents was sufficient.

From the experiments carried out it can be concluded that the optimum condition for electroplating gold wires for atom guides with regard to their shape, smoothness and optical reflectivity is at a temperature of 50 ^{o}C with a current density of 37 Am^{-2}. The effect of stirring the solution during electroplating was also found to be detrimental to the shape of the wires produced.

3.2.5. Atom guide fabrication

Having created a process by which electrochemically deposited wires could be created, this and two other methods were investigated for their suitability in the fabrication of an atom chip. The other two methods are based on etching a thick layer of gold to the desired pattern. Two etching methods are investigated, wet etching and ion beam milling. The three fabrication processes are depicted in Figure 44 and Figure 47.

The first method described is the electrochemical deposition of the gold wires into a photo resist mould. The process begins with a 4 inch silicon wafer cut on the {110} plane. The wafer was cleaned using a standard RCA and fuming nitric acid. It then underwent a process of wet oxidation in a furnace at 1000 ^{o}C to produce a 600 nm thick oxide layer (Fig 44a). This oxide layer acted as an insulating layer between the silicon and the wires. The wafers then had a 40 nm layer of chromium deposited by thermal evaporation. This layer is required to help the gold adhesion to the wafer. A 150 nm thick gold seed layer was then evaporated onto the chromium seed layer (Fig 44b). The wafer was then given another FNA clean.

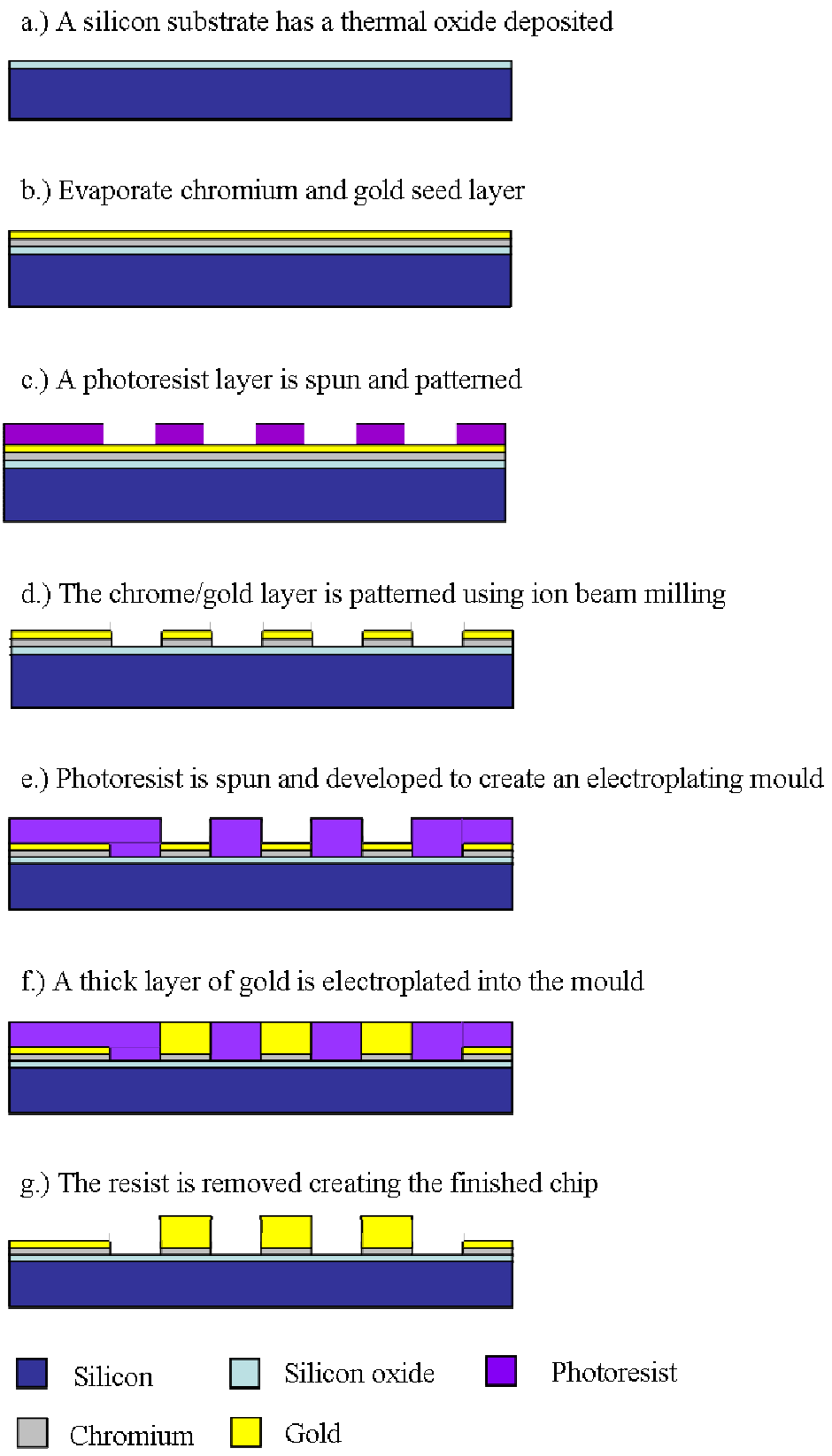

Figure 44: Process flow an atom guide with electroplated wires.

Next, this seed layer had to be patterned using ion beam milling. To achieve this, a photoresist mask was used (Fig 44c). The wafers were spun with S1818 at 500 rpm for 10 seconds followed by 2000 rpm for 30 seconds. This created a 2.2 μm thick layer. This layer was then patterned with the design shown in Figure 45. The design not only has the final chip pattern on it but also some features needed for the electrochemical deposition stage. This comprises of a single large contact pad for applying the charge to the chip via a crocodile clip and also wires connecting this pad to all the area of the chip that require electrochemical deposition.

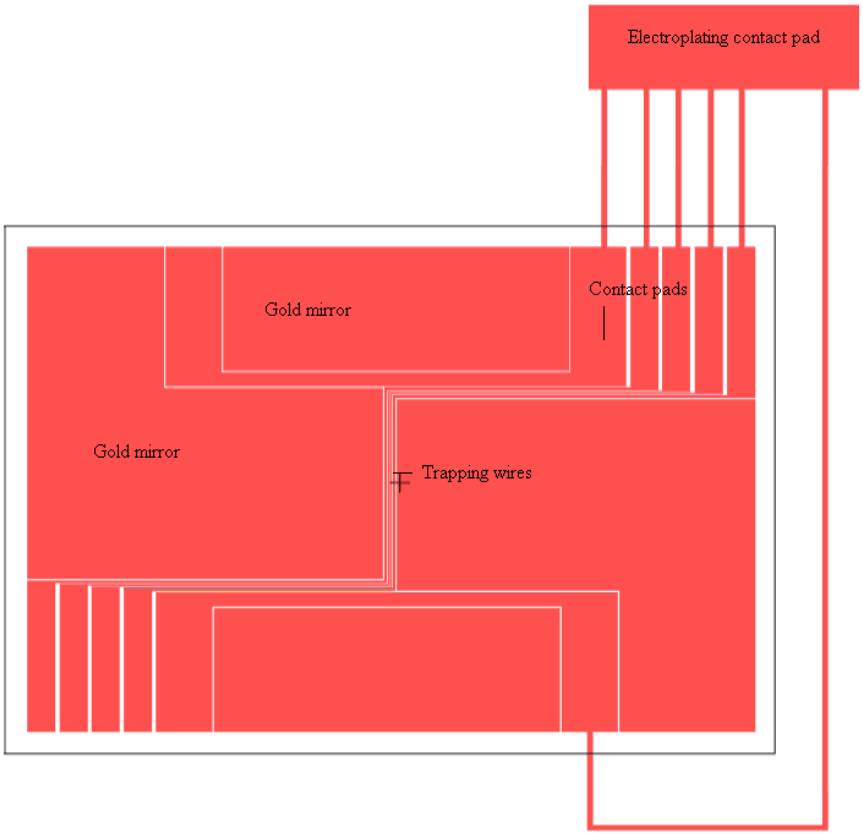

Figure 45: Mask design used for wire fabrication. The design contains the trapping wires in a Z shape, contact pads for connecting the chip into the MOT, gold mirrors to allow a mirror MOT to be formed from the chip and a large contact pad to allow a crocodile clip to easily be applied for electroplating the sample

The seed layer was then patterned using ion beam milling. The milling was performed on an IONFAB 300+ by Oxford Instruments [115]. The beam voltage and current was set to 388 V and 200 mA, respectively, with the accelerating voltage set to 276 V. The wafers were cooled to a temperature of 21 ^{o}C using helium. This recipe was taken from a database of standard recipes available at the cleanroom at the

University of Southampton. The wafer was milled to a depth of 200 nm (Fig 44c). The resist protects areas of the chip, represented by the red in Figure 45, from any damage. The resist was then stripped using a plasma asher set to 110 ^{o}C with 600 W for 60 minutes. A plasma asher is used before a fuming nitric acid resist strip as the process of ion beam milling can polymerise the resist. This makes it hard for the fuming nitric to remove it, often leading to patches of remaining resist. The plasma asher removes this polymerised resist allowing a fuming nitric acid clean to be used to remove any remaining resist.

Next the electroplating mould was created as shown in Figure 46. The wafers were spun with SPR 220-7 at 500 rpm for 10 seconds followed by 4000 rpm for 30 seconds. This created a 7 μm thick layer. The wafers were then cleaved into individual chips so they could be individually electroplated (Fig 44d).

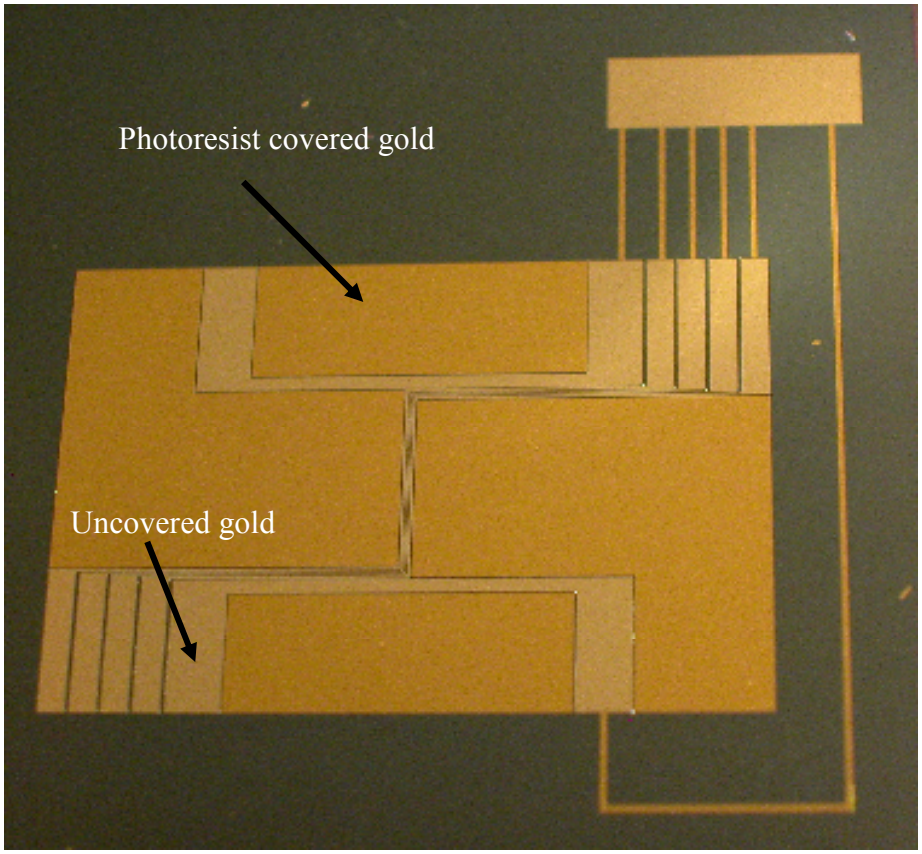

Figure 46: Atom guide with plating mould in place. The resist is covering all areas except the wires and contact pads which appear as a lighter gold colour.

The electrochemical deposition was performed using ECF64 cyanide free gold plating solution containing 10 g/dm^3 gold from Metalor. The deposition was controlled using an Autolab PGSTAT30. A standard three electrode setup was used with a platinum counter electrode. The deposition bath was placed in a water bath kept at 50 ^{o}C. Using the optimum current density of 37.5 Am^{-2} the experimental current is calculated. This was then set as a constant and the deposition process runs until the desired thickness is acquired (Fig 44e). Having deposited the desired thickness the resist is stripped in fuming nitric acid, leaving the gold wires (Fig 44f).

3.2.6. Ion beam milling

Having created an atom guide using electrochemical deposition, another method for producing gold microwires was investigated. While electro chemical deposition is a very versatile method the resultant layers are grainy and this can lead to disturbances in the magnetic field produced as discussed previously [102]. Sputtered gold layers are more homogeneous and therefore can create smoother trapping potentials [116]. Therefore instead of growing thick wires, a thick layer of gold was deposited and then patterned into the wires. The complete process is described below and shown in Figure 47.

A silicon wafer was cleaned using a standard RCA clean. It then underwent a process of wet oxidation in a furnace at 1000 ^{o}C to produce a 600 nm thick oxide layer (Fig. 47a). This was followed by a fuming nitric acid clean. The wafers then have a 40 nm layer of chromium deposited using a thermal evaporator (Fig. 47b). A 3 μm thick gold layer was then evaporated. This was done in five steps of 600 nm to prevent overheating of the evaporator (Fig. 47c). The wafer was then given another fuming nitric clean.

The wafers were then patterned with a 2.2 μm thick layer of HPR504 photoresist. Spinning was carried out at 500 rpm for 10 seconds, followed by 30 seconds at 1500 rpm. This process was followed by a soft bake at 90 ^{o}C for 120 seconds. The wafers were then exposed on a Karl Suss MA8 for 9 seconds at 6.5 mW/cm^2 (Fig. 1d).

Next, the wafers were ion beam milled. The milling was performed on an IONFAB 300. The beam voltage and current was set to 388 V and 200 mA, respectively, with the accelerating voltage set to 276 V. The wafers were cooled to a temperature of 21 ^{o}C using helium. The wafers were milled for 50 minutes which results in a maximum depth of 4.4 μm (Fig. 47e). This means the gold is over etched in some places, causing the mill to go through the silicon oxide layer and into the silicon substrate itself. The ion beam milling does not etch uniformly across a wafer and therefore the overetching is a necessity to ensure all the chips present on the wafer are fully etched.

The resist was stripped in a plasma asher set to 110 ^{o}C with 600 W for 60 minutes (Fig. 47f). Once all the resist has been removed the wafer is cleaned using fuming nitric acid.

The resistivity between the wires was checked after fabrication using a standard multi-meter. During the over etching of the silicon substrate, when the ion beam milling is performed, some redeposition can occur potentially creating a short between the gold wires and the base wafer. This manifests itself in a low resistance between wires that should be electrically isolated. To address this issue the wafers with low resistance between wires are given a 5 second buffered Hydrofluoric acid dip (7:1) followed by a 5 minute Potassium hydroxide etch. This causes slight undercutting of the gold wires, however it does eliminate any shorts present ensuring electrical isolation between the wires.

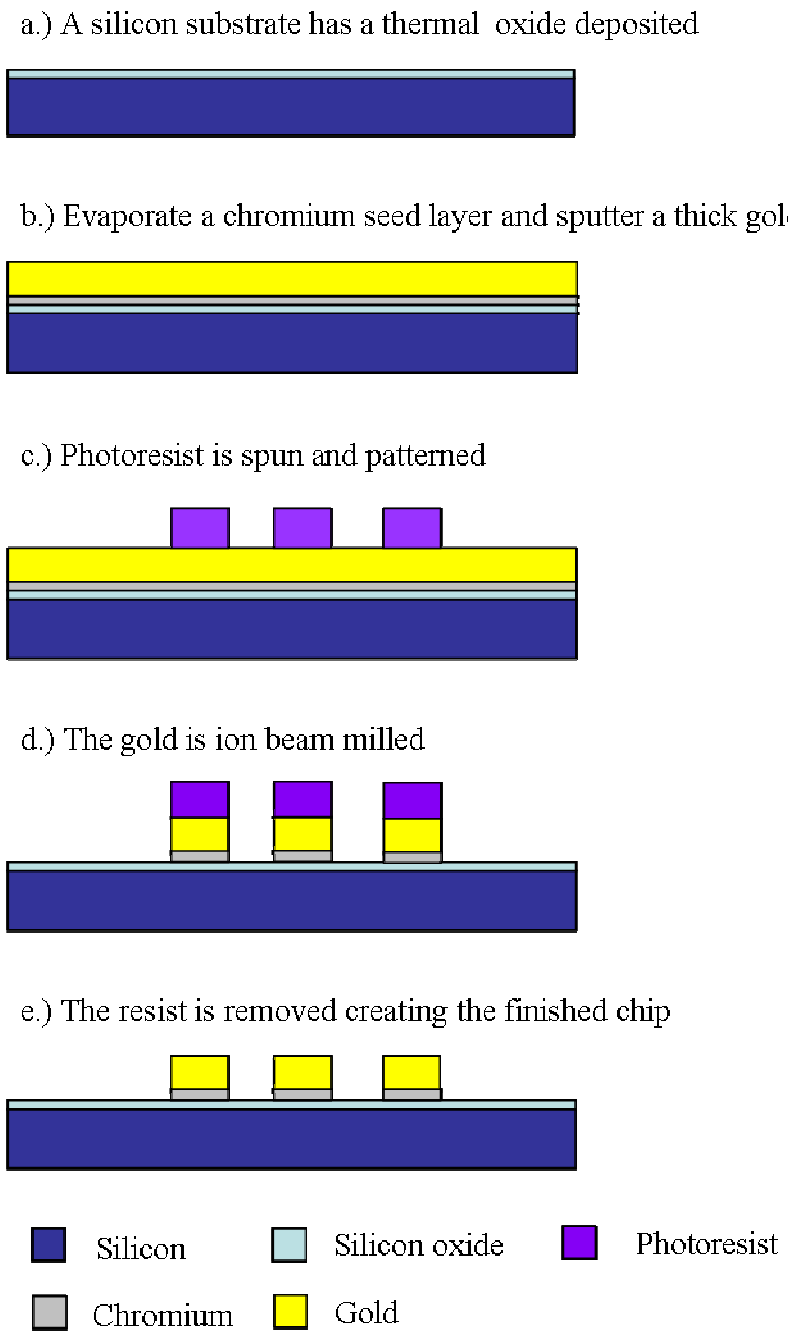

Figure 47: Process flow for fabricating the gold wires via ion beam milling.

3.2.7. Wet etching

This process is identical to the one described in section 3.2.6, but wet etching is used instead of the ion beam milling technique. The gold was etched using an aqueous KI_3 solution (4 g KI, 1 g I_2 in 40 ml H_2O) at room temperature for 8 minutes while the wafer was agitated manually. The chromium seed layer was then etched in a mixture of ceric ammonium nitrate and nitric acid (5g $H_8CeN_8O_{18}$, 4 ml HNO_3 (70%) in 5 ml H_2O). This produces wires with vertical side walls with no over etch into the silicon substrate.

3.3. Results

Having created atoms chips by the three methods described in section 3 the results were compared. Figure 48 shows both the wafer and an individual atom chip produced by the electro chemical deposition method.

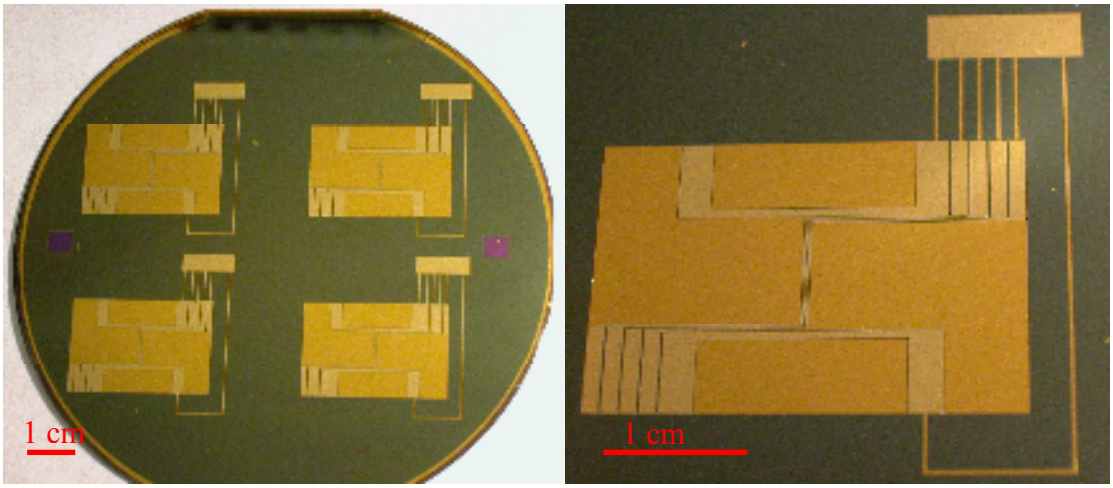

Figure 48: Image of the wafer and an individual atom chip.

3.3.1. Profile measurements

To check the quality of the wire profiles, an SEM measurement of the cross section and side walls of the wires was performed. The chips were first cleaved

perpendicular to the trapping wires to allow an SEM inspection. Figure 49a shows a cross-sectional SEM view of the wires produced by electrochemical deposition into a mould and Figure 49b shows a magnified view. This method produced the smoothest side walls of all three methods described previously as determined by a visual inspection on an SEM. The lifting of the gold pictured is an artefact from the cleaving process.

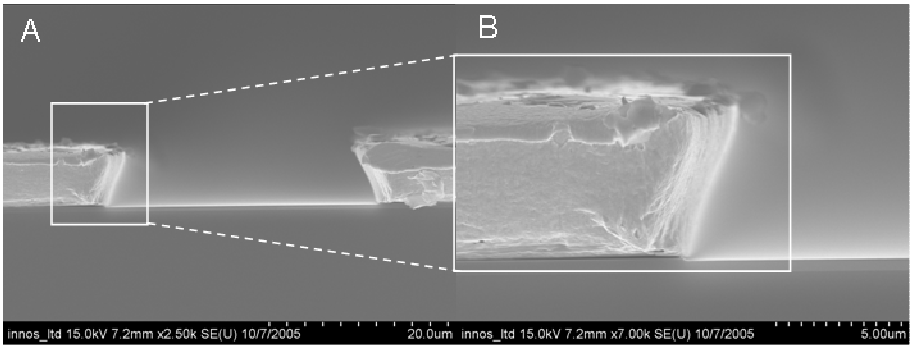

Figure 49: Scanning electron microscope images of microfabricated wires. A: Cross section of two wires. B: Magnified view of one wire edge.

Figure 50a shows a cross-sectional SEM view of the wires produced by the ion beam milling process and figure 50b displays a magnified view of the same wires. The wires produced by this method have a sloped side wall. This is not an inherent feature of the ion beam milling process. The sloping occurs due to the reflow of the resist prior to the milling. This is commonly performed to reduce strings of resist forming that can be very difficult to remove. Figure 50 clearly shows over etching of the silicon. While this is not a problem for the performance of atom chips it did produce some unexpected complications. When the resistance between wires was measured they were all showing an electrical short. After some experimentation it was discovered this was due to silicon redeposition over the oxide barrier. To remove this all the ion beam milled chips had to be given a short KOH dip. This increased the resistance from the order of kilo-ohms to 1 mega-ohm.

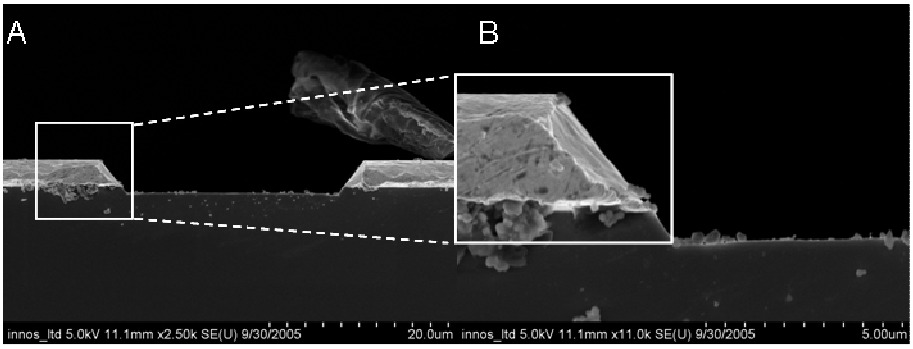

Figure 50: Scanning electron microscope images of microwires fabricated by ion beam milling. A: Cross section of two wires. B: Magnified view of one wire edge.

Figure 51a and 51b show the cross sectional view of the wires produced by wet etching at different magnifications. This method produced wires with vertical edges. There is some undercutting and lift off at the wire edges as seen in Figure 51b. It is thought that this occurs due to over etching of the chromium causing undercutting of the gold wires. The wires are then free from the silicon and the residual stress present in the film causes it to curl away from the silicon. Figure 51c shows that the side walls are rough compared to the other method and non uniform in both the planes.

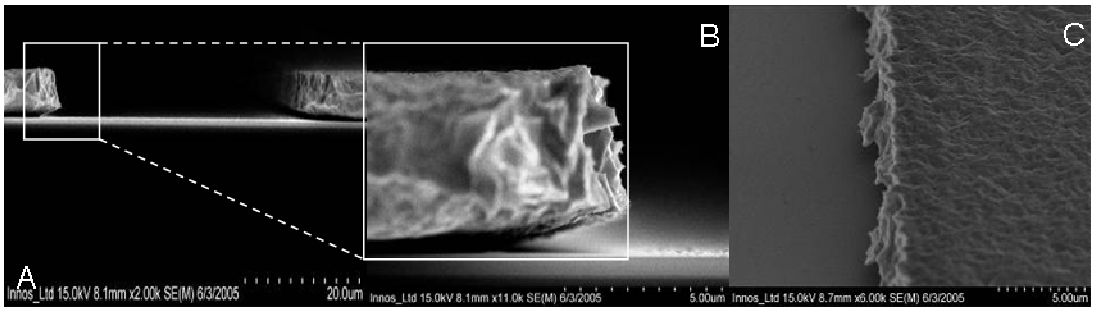

Figure 51: Scanning electron microscope images of microwires fabricated by wet etching. A: Cross section of two wires. B: Magnified view of one wire edge. C: Top view of the wires sidewall.

All three methods can be used to successfully create atom chips and each has its advantages and disadvantages. Overall the method that created the best wires was sputtering a thick layer and then ion beam milling. While electroplating was considered to have the smoothest sidewalls, the granular structure proved problematic in creating a smooth trapping potential and so the collaborators at Imperial College London decided that the ion beam milled atom chips gave the best wires for trapping ultra cold atoms

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3.3.2. Resistance measurements

Below is an image showing the chip used to perform the resistance measurements. This chip was fabricated using the method described in section 3.2.6. The wire and electrodes are labelled arbitrarily.

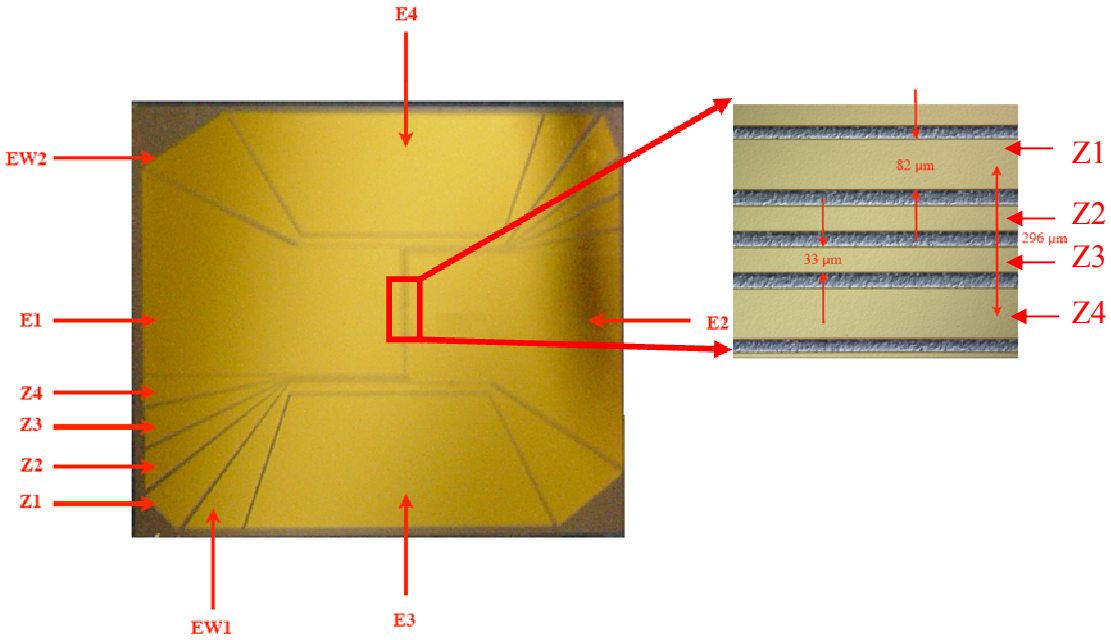


Figure 52: Layout of the atom chip showing the whole chip and a close up of the central trapping region. Four current carrying wires can be seen creating the Z trap across the centre of the chip (Z1-Z4) and two end wires EW1,2 which provide additional axial confinement.

Table 4 shows typical values of the resistance for the wires as measured by a digital ammeter. The difference in resistance seen is due to the varying dimensions of the wires. Z1, Z4; Z2, Z3 and EW1, EW2 share the same dimensions and correspondingly the same resistance. The larger the wires the smaller the resistance measured, as expected. Table 5 shows the resistance between the wires. Initially these were in the order of ohms and therefore shorting until the cause was discovered and rectified as described previously. After solving the problem all the values were increased to kilo ohms and mega ohms in the best cases.

	Z1	Z2	Z3	Z4	EW1	EW2
R (MΩ)	1.8	3.4	3.4	1.8	0.5	0.5

Table 4: A table showing the resistance in mega ohms of the chip wires as measured by a digital ohm-meter.

The maximum continuous current densities that could be run through the wires, both separately and in parallel, were measured. They were measured until a temperature rise of approx. 100 ^{o}C was observed. The maximum current density should be limited by thermal dissipation of heat from the chip wires to the vacuum flange via the chip mount. The results of the measurements are shown in table 6. The maximum continuous current achieved was 1.8 A in the large wires, and 1.3 A in the small wires. The corresponding current densities are 9.6×10^{9} Am^{-2} and 1.1×10^{10} Am^{-2}. The maximum current that could be run in series in the two large wires was reduced to 1.3 A, corresponding to a current density of 6.9×10^{9} Am

Wires	Current (A)	Density (A/m^2)
Z1 (Z4)	1.8	9.6×10^{9}
Z2 (Z3)	1.3	1.1×10^{10}
Z1 & Z4	1.3	6.9×10^{9}
Z2 & Z3	1.25	1.1×10^{10}

Table 5: A table showing the current density each wire could safely contain.

Using this device, atoms have been trapped at Imperial College London [117]. The chip is loaded from a cold atomic beam and trapped using the mirror MOT created using the atom guides surface. From there the atoms are transferred into a magnetic trap formed by running current through the chip Z-wires and controlling external bias fields. The cloud is then cooled to form a BEC via radio-frequency forced evaporation. In a typical experiment a BEC is produced with up to 10^{6} atoms in this trap.

The BEC is imaged from both side-on and end-on. From side on an elongated cloud can be seen as shown in Figure 53a. Figure 53b shows the imaging beam in relation to the atomchip used to produce Figure 53c. In this figure, an end on view of the BEC is seen, showing that it has been split into two components.

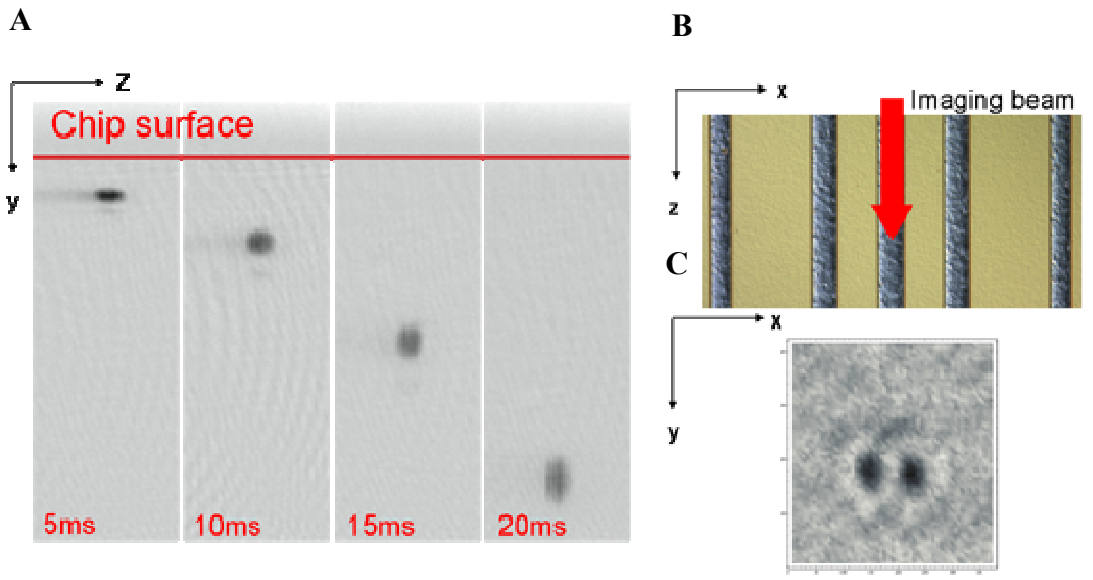


Figure 53: Image showing a BEC with ~2x10^5 atoms that have been trapped on the atom guide. a) Shows atoms in free fall having been trapped and confined on the atom guide, b) shows the close up of the atom guide used to trap these atoms and c) shows a double well potential having split the BEC into two separate wells (Taken from ref[118]).

The relative phase between the two split components can be measured by releasing the clouds and allowing them to overlap in time-of-flight as shown in Figure 54. Quantum interference between the two possible paths taken by the matter wave results in a distinctive modulation of the density of the overlapping components. The wavelength of these interference fringes is inversely proportional to the initial splitting distance in the double well potential. The relative phase of the two components can be read out directly from the phase of the interference fringes.

This ability to create interference patterns out of a BEC allows the creation of an atom interferometer on a chip. Currently atom interferometers are used as precision measurement tools in applications such as fundamental science and engineering projects. However these are often very large machines, filling a room. The ability to perform the same function on a microchip opens atom interferometers up for use in more portable real world applications. Examples could include inertial sensors such as gyroscopes or gravimeters. This would have applications from space satellites to oil exploration.

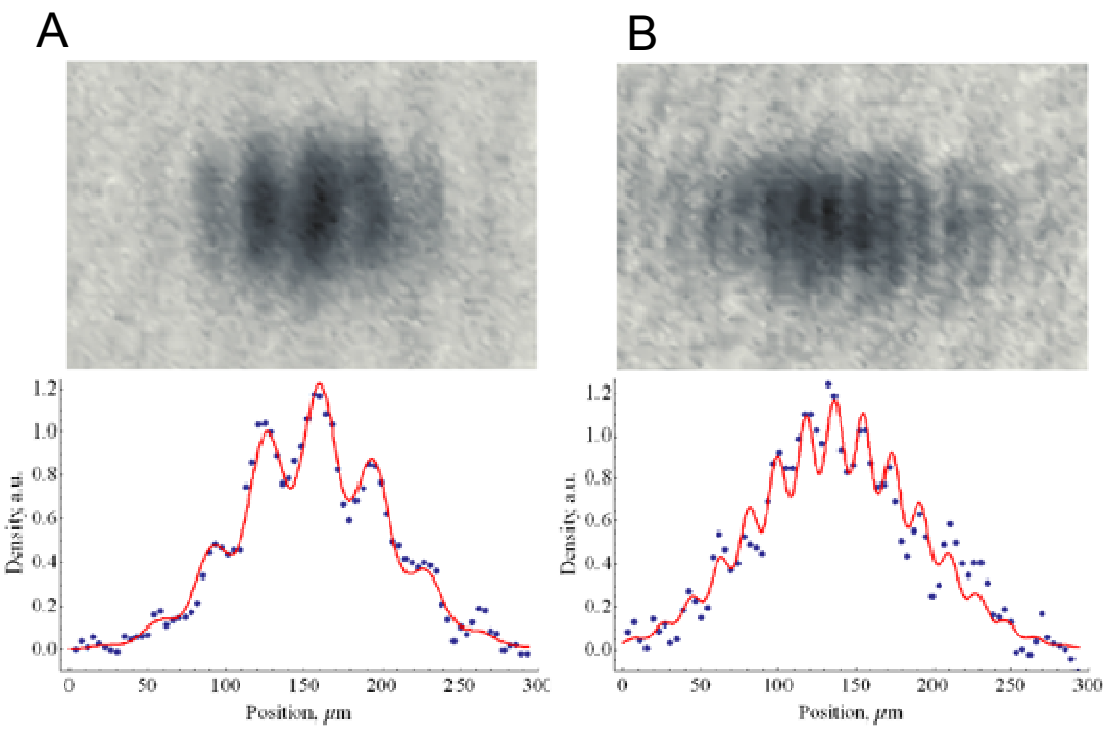


Figure 54: Interference fringes visible after 16ms time of flight. Both A and B show the fringes produced by the quantum wave interference. B shows a cloud split by a higher RF-intensity than A, leading to a larger well separation and smaller fringe spacing. The red line shows the curve fit of a modulated Gaussian envelope and the blue dots represent the density measured by absorption imaging (Taken from ref [118]).

3.4. Conclusion

In this chapter the theory, design, fabrication and results of the atom guides have been presented. Three methods for producing such a chip have been presented along with the characterisation of the devices for their suitability to trapping atoms. An electroplating procedure has been presented and optimised for use in creating atom guides on atom chips.

It has also been demonstrated that atom guides fabricated by these methods are capable of both trapping and splitting a BEC on chip. This is the first important step toward creating integrated atom devices for use in real world applications.

Chapter 4

Pyramidal Micro-mirrors

As discussed previously in chapter 3 using small scale current-carrying wires fabricated on silicon, one can readily produce strong gradients of magnetic field near the surface of the chip, forming strong traps for paramagnetic atoms. In order to load these magnetic traps, it is usual to start with an MOT typically some 5 mm from the surface. This uses a combination of circularly polarised light beams and magnetic fields to collect atoms from a tenuous room-temperature vapour and to cool them to around 100 μK. The atoms are then further cooled in optical molasses to a few tens of μK before being magnetically trapped. Finally, this macroscopic atom cloud, typically 1 mm in size, has to be compressed into a much smaller volume and moved to the surface of the chip in order to load the microscopic magnetic trap. This sequence of loading and transfer is complicated and could be eliminated if the MOT was integrated into the chip. Moreover, this would open up the possibility of building arrays of MOTs to prepare large numbers of independent cold atom clouds.

A new approach has been developed and is presented in this chapter which would allow microscopic MOTs to be integrated into a silicon chip to collect small atom clouds that are automatically well positioned with respect to the traps on the chip removing the complicated loading and dispensing techniques previously needed.

The key proposal is to have an array of miniature pyramid MOTs [61] on the chip, which automatically prepares all the required light beams from a single circularly polarised input beam by reflecting the light in a concave square pyramid of mirrors as shown in Figure 55. This greatly reduces both the number of expensive optical components needed to prepare the light beams and the amount of laser power needed. Integrated wires encircling the base of the pyramid produce the required magnetic field with modest electrical power consumption and accurate positioning. The fabrication of an integrated MOT array on a chip represents an important step towards a truly integrated atom chip for portable applications.

In this chapter, the design, fabrication and results of the pyramidal micro-mirrors are presented. First the design parameters and decisions are described. Then the fabrication and integration of the pyramids into an atom guide are discussed. Finally, initial functionality tests are presented showing the chips' viability for use in atom traps.

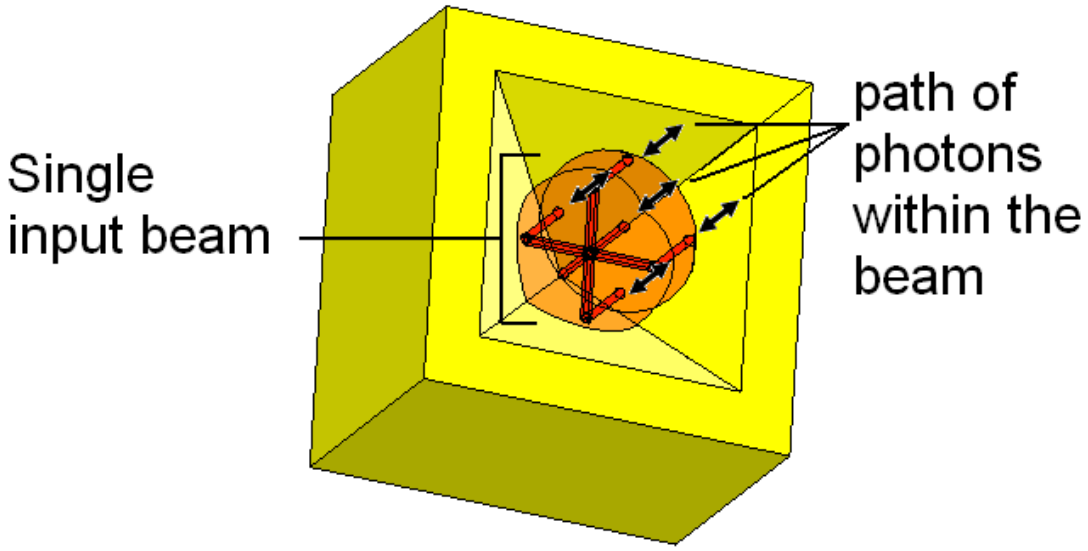


Figure 55: Diagram showing a laser beam incident on a pyramidal pit. Within the laser beam the standard six beam MOT is created by the incident and reflected photons.

4.1. Design

4.1.1. Silicon etch properties

Silicon consists of a face centered cubic structure as shown in Figure 56. This allows silicon wafers of various orientations to be manufactured. The anisotropic etching of various silicon wafer orientations using KOH has been well documented. This anisotropy arises from the different etch rates attributed to each silicon crystal plane.

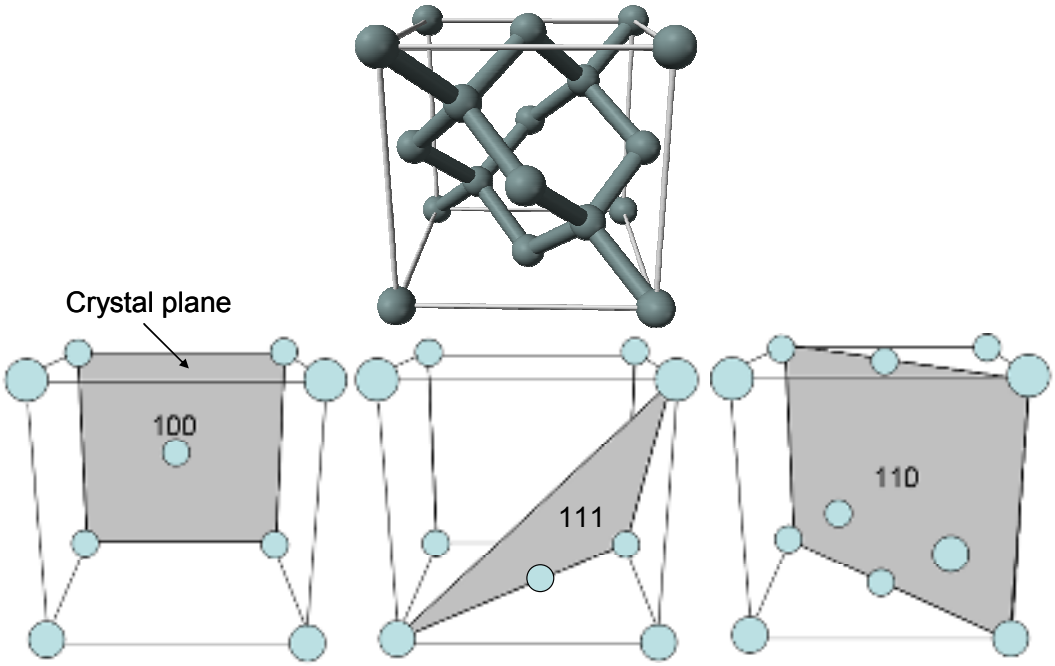


Figure 56: A face centered cubic unit cell as formed by silicon. Also shown are some of the crystal planes (Adapted from ref [119]).

To create a pyramid shape a silicon wafer orientated to the {100} plane must be used. When a wafer of this orientation is etched for a sufficiently long time in KOH through an arbitrarily shaped mask, a square or rectangular based pyramid will be created, whose size is determined by the <100> directions bounding the mask openings edges. This shape is created from the slowest etching {111} planes which will be revealed as the etch progresses. Therefore any openings etched for a sufficient time will result in hollow pyramidal pits in the surface of the silicon bounded by the four most slowly etched surfaces $\{1,\bar{1},1\}$, $\{\bar{1},1,1\}$, $\{\bar{1},\bar{1},1\}$ and {1,1,1}. The angle between opposite faces will therefore be 70.52 °. This is shown diagramatically in Figure 57.

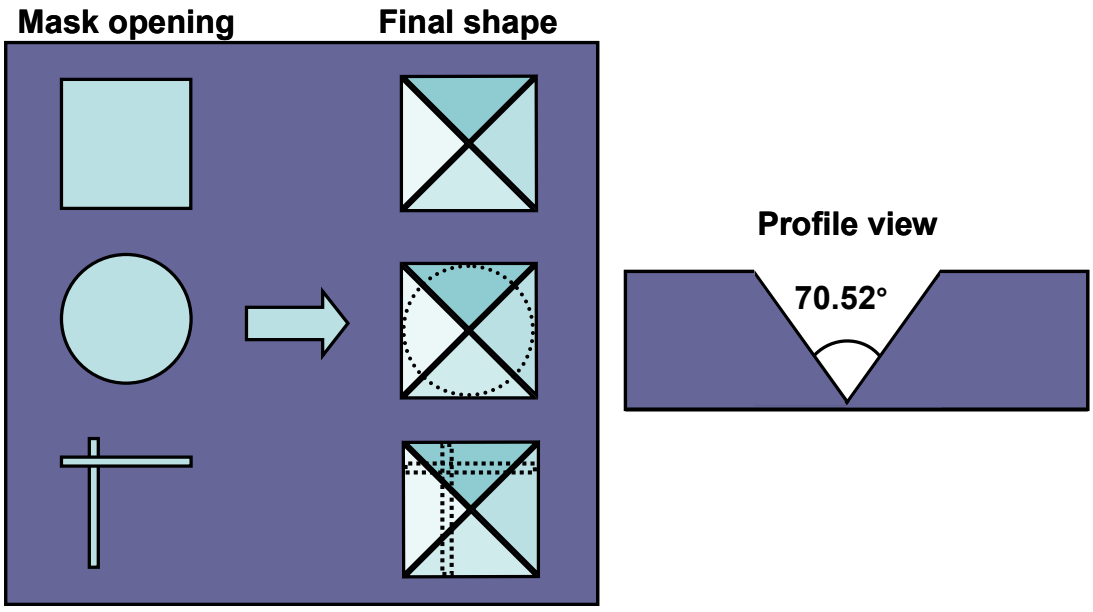


Figure 57: Picture showing the effect of different openings on the final etch shape after placing {100} wafers into KOH.

4.1.2. Chip design

In the chip presented here a range of sizes from 200 μm to 1.2 mm was created. For simplicity a square opening of the exact size needed was used. A large range of sizes was chosen as the exact size required for successful atom trapping was uncertain. The exact design for the chip created in this chapter is shown in Figure 58. Six sets of pyramidal sizes were used with each size split into a set of 5 and a set of 3. A single wire connects each set of pyramids starting at a large bond pad and circulating each pyramid in the set. The details of the wires are shown in Table 6.

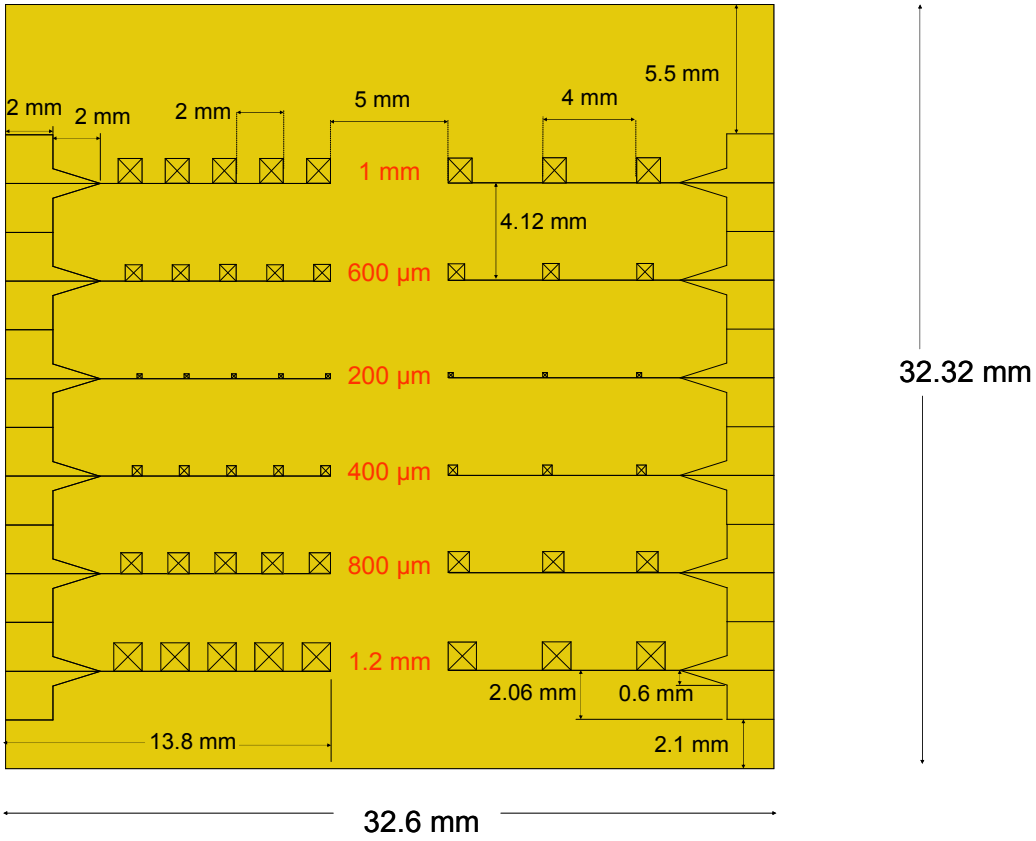
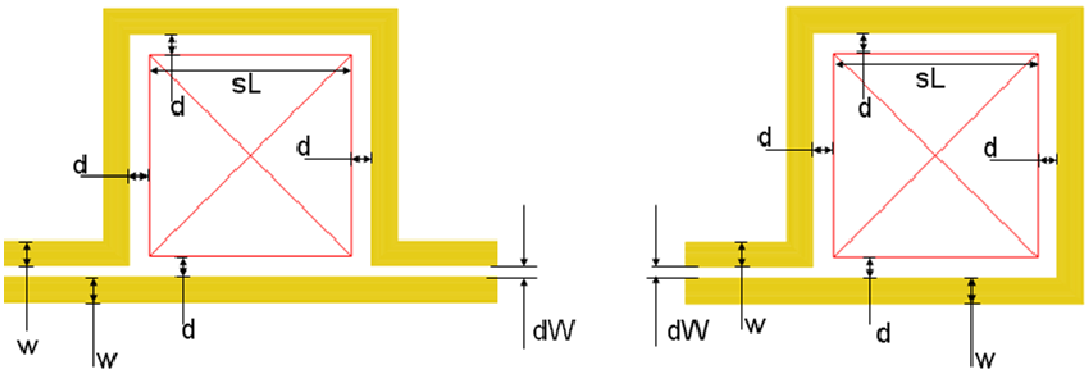


Figure 58: Schematic showing the design of the pyramidal chip. The squares with crosses represent the pyramidal pits while the lines represent the wires circulating and connecting the sets of pyramids together. To the left and right of the chip large bond pads are seen these are needed for wire bonding the chip into a package. The red writing denotes the size of the pyramidal opening. For a more detailed view of the wire see table 6 or figure 60.



Side Length sL (µm)	Wire Width w (µm)	Wire Separation dW (µm)	Edge distance d (µm)
200	25	10	20
400	25	10	20
600	25	10	20
800	50	10	20
1000	50	10	20
1200	50	10	20

Table 6: Table showing the different dimensions of the pyramids and wires present on the atom chip.

Care must be taken to ensure the openings are aligned to the crystal plane indicated by the wafer flat. This was achieved by using an MA8 mask aligner that contained a flat finder. Any misalignment with respect to the crystal plane will cause the initial opening to be rotated with respect to the crystal plane. When the wafers are then placed in the KOH etch bath, they etch to a square along the crystal planes not parallel to the initial openings as shown in Figure 59

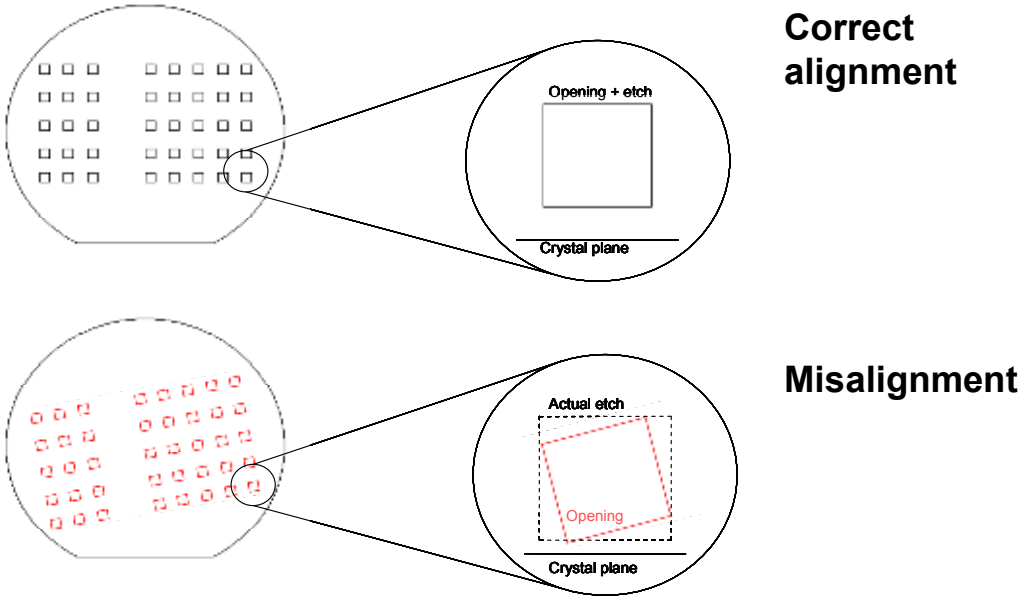


Figure 59: Diagram showing the result of misalignment of the initial opening on the subsequent KOH etch of the pyramids.

The results of any misalignment can cause a failure of the devices. This happens because the pyramids grow bigger than the initial opening size. This can easily be calculated using:

$$L = I\cos\theta + I\sin\theta \tag{32}$$

where L is the resultant length of the pyramid edge, I is the initial opening size in the mask design and θ is the angle of misalignment. This increase in size can cause complete failure of the device as the circulating wires must be placed close to the edge of the pyramid so an increased pyramid size will cause the wires to be cut completely.

The alignment can also be done on the wafer, instead of using a flat finder on a mask aligner. This can be done using an alignment technique suggested by Ensell [120]. This allows the crystal plane to be identified to an accuracy of 0.2 ^{o} and therefore aligned accurately.

If the only issue is the size of the pyramids growing larger than planned, circular openings could be used as these will not grow any larger than the circle diameter. In

this chip however this would not prevent chip failure due to misalignment as the wires are designed to fit around squares whose edges are parallel to the rows, see Figure 60.

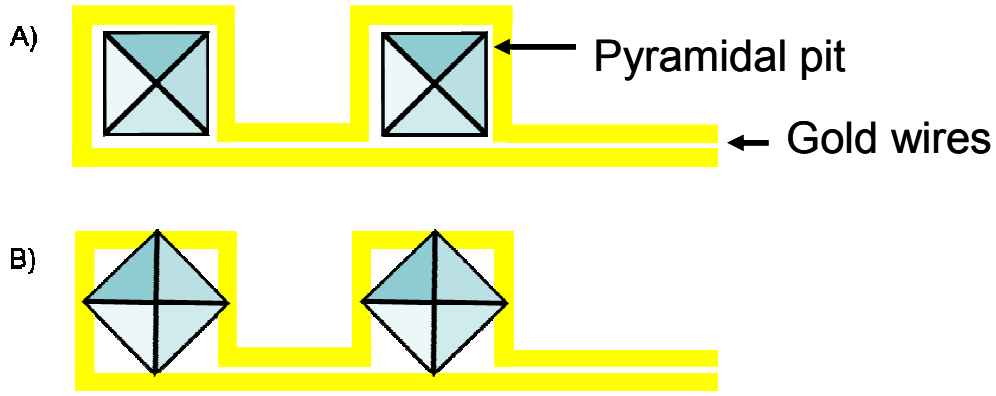


Figure 60: Image showing the problem of misalignment to the crystal planes on the wire placement. A) shows the correct alignment while B) shows pyramids of the same size but created with the rows of pyramids not aligned to the crystal planes. The wires can clearly not be rotated to fit this new orientation.

4.1.3. Optical properties

In an ideal MOT, a perfect pyramid with 90^{o} between the faces would be used. As shown earlier a KOH etch gives a pyramid with faces separated by 70.5 °. To determine whether this is still suitable for an MOT, the optical properties of these pyramidal cavities were investigated by experiments performed on macro scale pyramids and pyramids without integrated wires [121]. The initial pyramids used for this experiment are shown in Figure 61.

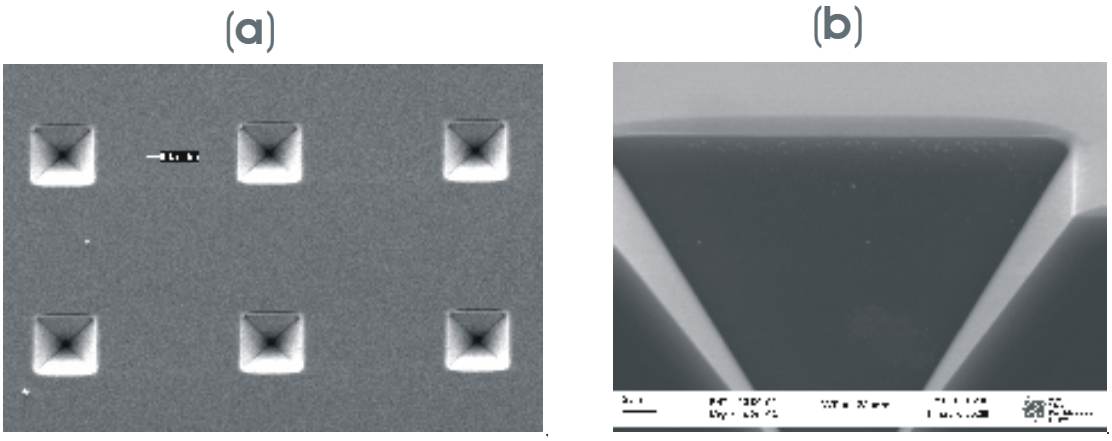


Figure 61: SEM images of etched and gold coated pyramids: (a) showing the top view of an array of pyramids with pitch 100µm, (b) showing a cross section of a single pyramid with an opening 30µm wide corresponding to a depth of 21.3µm.

In previous work, performed at Imperial College London in conjunction with the Southampton group [121], the optical properties of the pyramidal micro-mirrors were investigated. The pyramid was illuminated using a collimated 1mm diameter laser beam of wavelength 633 nm, propagating normal to the axis of symmetry. Circularly polarised light at normal incidence on the chip is reflected in the four mirrors that form the pyramid. At each reflection the helicity of the light is reversed. If the pyramidal cavity had a 90 ^{o} angle between opposite faces, these reflections would produce three counter-propagating pairs of light beams that are mutually orthogonal. However the departure from a right angle causes the beams to be reflected into a variety of directions. These beams were modelled by Imperial College London and classified as Type 1, 2, or 3, according to the region of the pyramid where the first reflection occurs, as shown in Figure 62.

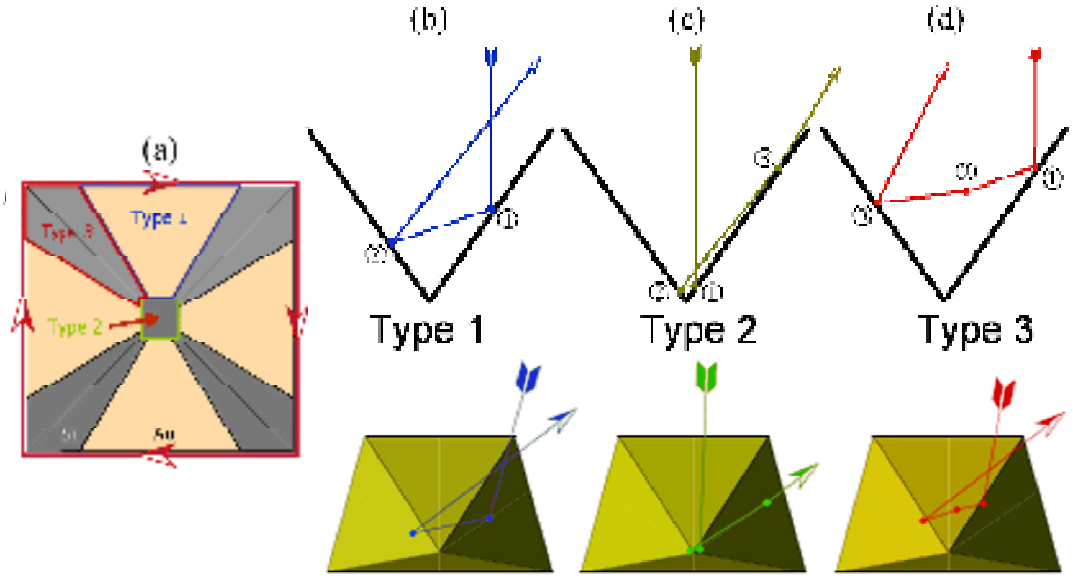


Figure 62: (a) Plan view of pyramid showing the three regions of reflection and the encircling current. (b) Cross section through pyramid and 3D projection showing a type-1 reflection. (c) Type-2 reflection. (d) Type-3 reflection where the ray is intercepted by the adjacent mirror at the point marked 2.

Type-1 rays are reflected on two opposite sides of the pyramid before leaving, as illustrated in Figure 62b. Type-2 rays also reflect on opposite faces, but strike the original face again before leaving, as shown in Figure 62c, making a total of three reflections. After the first reflection in Figure 62d, type-3 rays head towards the opposite face, but on the way they are intercepted by the adjacent face because they are close to the diagonal edge of the pyramid. Here they undergo a grazing reflection, marked (2) in the figure, where the helicity of the light is reversed. Finally, the opposite face is reached for a third reflection. Type-3 rays destabilise the MOT because they have the wrong helicity, and because they create an excess of light forces which pushes the atoms out of the pyramid instead of trapping them.

A mock pyramid was created with the same properties as a KOH etched pyramid but on a larger scale. The pyramid had an opening of length 16.3 mm and an angle of 70.5 ^{o} between the faces. Each face was coated in a gold layer. Preliminary experiments conducted using this pyramid failed to produce an MOT because of the presence of the type-3 rays. Once the gold was removed from the areas where the type-2 and type-3 rays are produced a MOT was successfully created. Using this setup a cloud of 1.6×10^{8} atoms was trapped [121].

These results showed that a standard pyramidal etched pit with a reflective coating is not the best setup for making these micro-mirrors. In a standard pyramid lateral confinement is achieved using the first reflections of the type 1 beams and vertical confinement is given by the input and the second reflection of the type 1 beams. The presence of the type 2 and 3 beams can disturb the balance of forces. Therefore by removing the reflective coating from the area where type 2 and 3 beams are created they can be removed or significantly dampened.

4.1.4. Magnetic field properties

The magnetic quadrupole field required for the MOT is generated by electroplated wires encircling the pyramid base, as shown in Figure 63a and a uniform bias field generated using a large external coil of current carrying wires. The design and fabrication detail of these wires has been discussed in detail in chapter 3. A current I in this loop generates a magnetic field as shown in Figure 63a. The field strength B_z, at the centre of the loop, in the plane of the wire is given by

$$B_Z = -\frac{2\sqrt{2}}{\pi}\frac{\mu_o I}{L} \tag{33}$$

where μ_o is the permittivity of free space, I is the current flowing in the wires and L is the width of the square created by the wires.

A uniform vertical bias field is superimposed in order to create the quadrupole field configuration required by the MOT, as shown in Figure 63b. The light beams needed to create the magneto-optical trap inside the pyramid are formed from the incoming circularly polarised beam by the first and second reflections of the type-1 rays, as shown in Figure 63c.

Figure 63 shows the basic formation of a pyramidal MOT. First the magnetic field due to the current carrying wires circulating the pyramidal pit is shown in a). This setup creates a field maximum at the centre of the pit as represented by the red arrow.

Next the field due to the wires and an external field bias is shown. The external field interacts with the field from the wires to produce two spots of field minima, one above the pit and one inside the pit. Finally a single laser beam is shown incident on the pit. The reflections off the side walls focus all the photon paths into a point that can be tuned to be coincident with the field minima. This combination of light and magnetic fields allows atoms to be trapped.

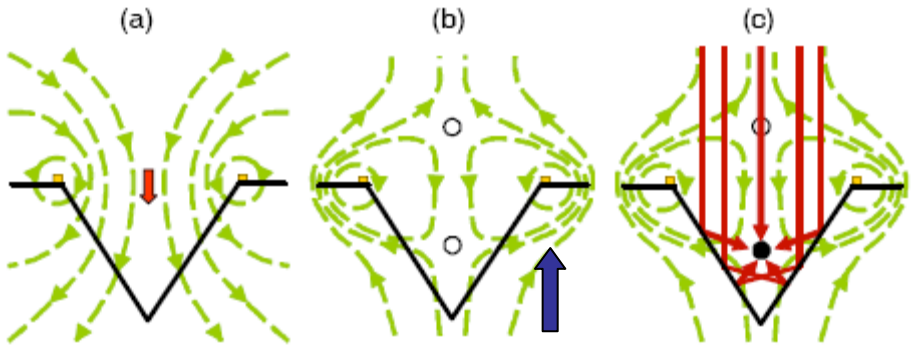


Figure 63: (a) Dashed lines: magnetic field created solely by the wires around the pyramid opening. Block arrow: maximum field strength is at the centre of the loop. (b) With the addition of a uniform bias, whose direction is indicated by the blue arrow, the net field acquires two minima, indicated by solid circles. (c) Circularly polarised light creates a magneto-optical trap at the field minimum indicated by a filled circle. The beams that contribute are shown as solid arrows.

Under typical operating conditions used in most MOT experiments, the gradient is approximately 0.15 Tm^{-1} [122]. This is readily achieved on the chip because of the small scale: for example in the 1mm loop it requires 0.1 A. For detailed information about magnetic trapping of neutral atoms refer to chapter 3.

By combining the techniques described above arrays of pyramids can be fabricated with the magnetic quadrupole fields being created using existing micro fabrication methods to produce current loops around each pyramid. It is estimated that these pyramidal MOTs will be able to trap as many as 1000 atoms or as few as 1 depending on the operating parameters [121].

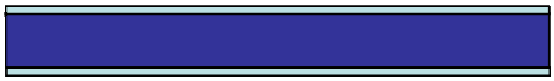
Two fabrication processes for producing pyramidal micro-mirrors were therefore designed. The first creates pyramid arrays with trapping wires surrounding them. The second produces the same layout but with the addition of patterning inside of the

pyramids to remove the undesirable beams; this has been termed the flower design. The process flows of both methods are described in the following section.

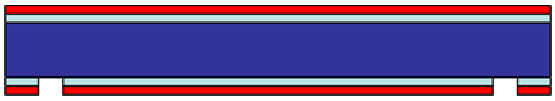
4.2. Fabrication

The entire fabrication process for both versions is depicted in Figure 64. It starts with preparation of the wafer and etching of the pyramids. The whole surface is then coated with gold and patterned to remove the gold from the type 2 and type-3 regions and to form the wires tracks. Finally, the wires are electroplated to a thickness of 5 μm. Covering the whole wafer with a uniform resist layer for this step posed the main fabrication challenge due to the depth of the pyramidal pits. The fabrication process is described in full detail below.

a.) A <100> silicon substrate has a thermal oxide grown

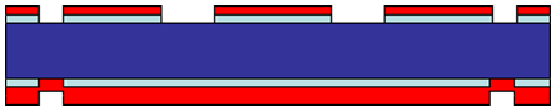


b.) Silicon nitride is deposited and alignment marks are etched into the back using RIE etching

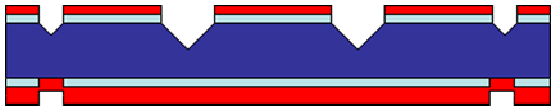


c.) Square openings are etched into the front of the wafer

d.) The back side alignments are protected with a PECVD silicon nitride layer



e.) The pyramids are etched using KOH



f.) The front side silicon nitride and oxide are stripped

g.) A TEOS silcon oxide is deposited followed by a Chromium and gold evaporated layer

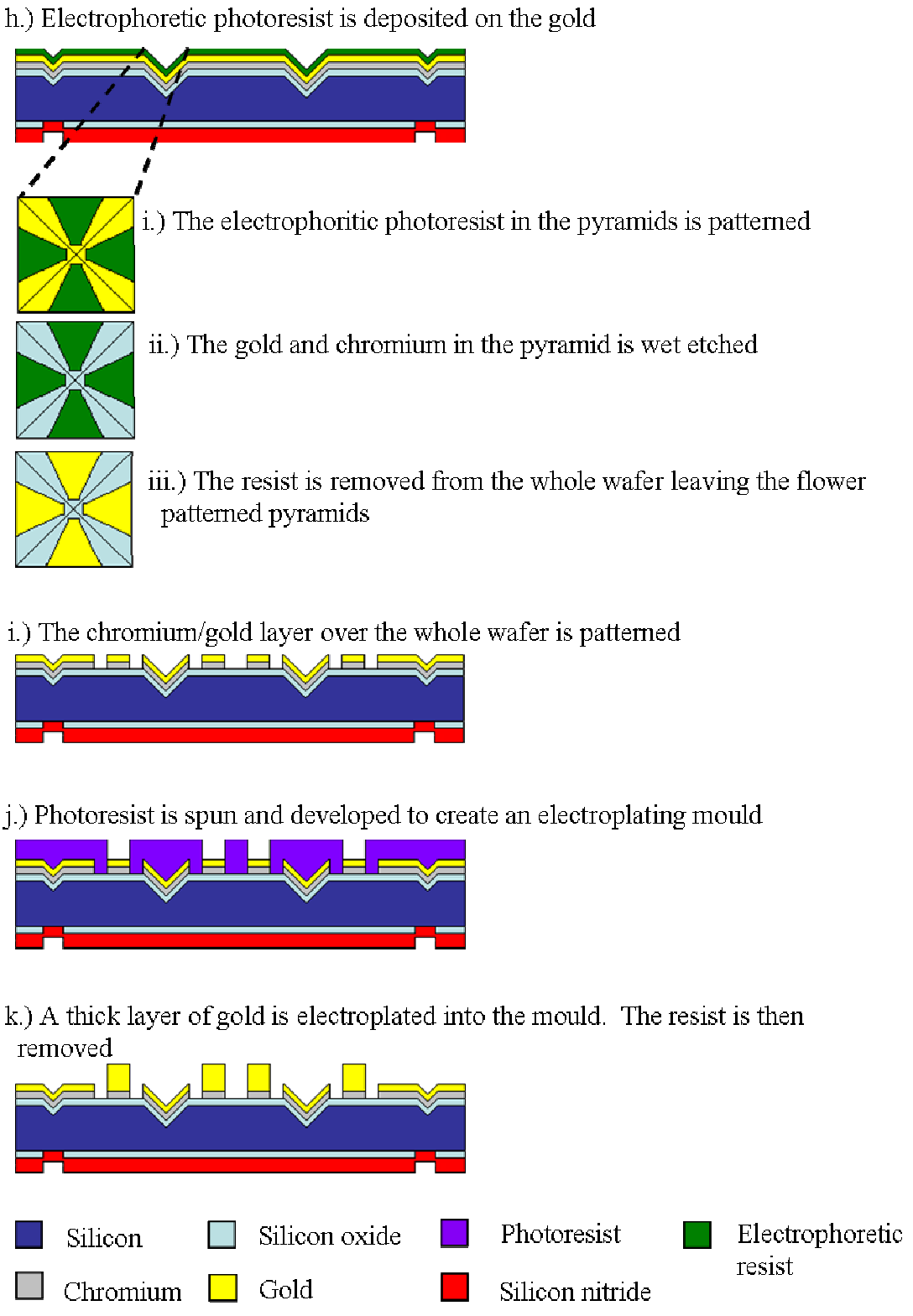


Figure 64: Process flow for the creation of pyramidal micromirrors.

The process begins with a 4 inch, 1 mm thick silicon wafer cut on the {100} plane. The specific orientation is required for the potassium hydroxide etch to produce the pyramidal shaped etches and the wafers must be 1 mm thick to allow the larger

pyramids to form fully without etching through the wafer. The wafer was cleaned using a standard RCA and fuming nitric acid. A layer of silicon dioxide and silicon nitride must then be deposited. A 170 nm thick oxide layer of silicon dioxide is grown by wet oxidation in a furnace at 1000 ^{o}C (Fig.64a). This acts to insulate the components created on the chip from the silicon wafer. A 50 nm layer of low stress silicon nitride was then deposited on both sides by LPCVD. The wafer is then placed in another fuming nitric acid clean to remove any contamination that the wafer has picked up during the processing. A reactive ion plasma etch was then used to make alignment marks on the back side of the wafers for the accurate positioning of all masks used in the fabrication process (Fig. 64b). Back side alignment is required due to the long KOH etch performed on the front of the wafer which would destroy any front side alignment marks.

In order to make the pyramids, 1 μm layer of photo resist AZ6612 was spun onto the wafers. An array of square openings was then patterned into the resist using a photo mask on a Karl Suss MA8 contact mask aligner. Using these openings the silicon nitride and dioxide layers were etched down to the bare silicon wafer using a dry plasma etch (Fig.64c). The resist is then stripped in a plasma asher.

The backside alignment marks had to be protected to prevent etching during the potassium hydroxide etch (Fig. 64d). To achieve this, a layer of PECVD nitride 1μm thick was deposited onto the backside of the wafers.

With openings created in the front side of the wafers and the alignment marks protected the pyramidal pits could be etched. To protect the wafer edges during the long etch, PTFE tape was wound round each wafer. The wafers were then etched for 19 hours in KOH at a concentration of 33 % by volume and at a temperature of 80 ^{o}C as this had been shown previously to create highly smooth pyramidal surfaces (Fig. 64e) [121]. This produces pyramidal pits bounded by the four most slowly etched surfaces $\{1,\bar{1},1\}$, $\{\bar{1},1,1\}$, $\{\bar{1},\bar{1},1\}$ and {1,1,1}; see Figure 65. The silicon (111) faces produced are very smooth because of the layer by layer etching mechanisms involved [123, 124] and have been shown to have a RMS surface roughness as low as 0.5 nm [121]. The wafers were then once again cleaned in a fuming nitric acid bath.

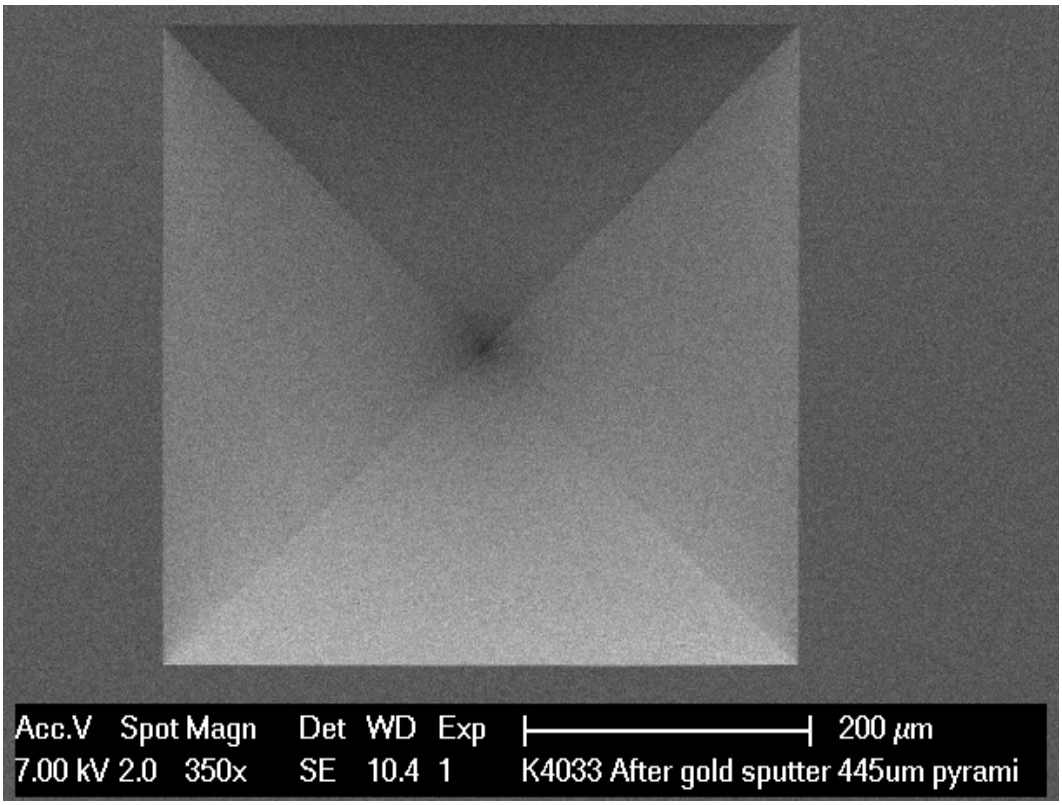


Figure 65: SEM image of a 400μm wide pyramidal etch.

The wafers then had the silicon nitride layer stripped from the front side using a dry plasma etch (Fig 64f). To ensure a uniform, unbroken layer of oxide remained to isolate the current carrying wires, the remaining silicon oxide was removed in a Hydrofluoric acid (HF) dip and a new Tetraethylorthosilicate (TEOS) PECVD oxide layer 170nm thick was deposited.

The wafers were then placed into an evaporator, where a 50 nm layer of chromium was deposited. This layer was required to help the gold adhere to the wafer. A 100 nm thick gold layer was evaporated onto this adhesion layer (Fig. 64g). The wafers were then cleaned using fuming nitric acid.

With the pyramids created the flower patterning was now required. To test pyramids both with and without flowers half the wafers in the batch were removed at this point and rejoined the flow after the flower patterning had occurred

In order to pattern the flowers a uniform layer of resist is required inside the pyramids. Spinning a layer of resist in the pyramids themselves was not considered a viable method as it would have left a highly non-uniform layer of resist inside the pyramids and rendered flower patterning impossible. Also due to the presence of the pyramidal pits striation of the resist would result causing thick waves around the inside edges of the pits and thinning in the spin shadow of the pits. If this layer becomes too thin it may cause etching of gold where the wires must be created. Therefore to enable the pyramids to be patterned a uniform layer of resist layer is required over the pyramid sidewalls as well as the wafer as a whole.

In order to avoid this problem electrophoretic deposition of Eagle 2100 negative photo resist was used. This method creates a uniform resist layer over non uniform topology. The wafers were first connected up to a voltage source so it would act as a cathode. They were then placed into the resist bath heated to 33 ^{o}C and a voltage of -125 volts was applied. The wafers were left until the current drops to zero and removed. They were then placed into a conservation rinse for 10 seconds to reclaim dragged out resist and remove the bulk excess still on the wafers. The wafers were then rinsed in deionised water and dried in a vacuum oven at 65 ^{o}C. At this stage the resist remains tacky. To prevent any contamination of the contact mask during photolithography the wafers were dipped into eagle 2002 topcoat for 30 seconds and again dried in the vacuum oven (Fig 64h).

Next, the wafer is exposed for 77 seconds at 6.5 mW/cm^2, using a mask designed to remove the gold from the type-2 and type-3 regions thus creating the flower (Fig. 64h(i)). This pattern was developed using Eagle 2005 developer heated to 40^{o}C, which was sprayed onto the wafer for 4 minutes as shown in Figure 66. In this figure two levels of focus are shown, a) is focused at the middle of the pyramid and shows the pattern has been exposed correctly and the resist has cleared well in the desired areas. Image b) has the focus at the apex of the pyramid. This image shows that the pattern has also been correctly exposed at the bottom of the pyramid therefore creating the desired pattern.

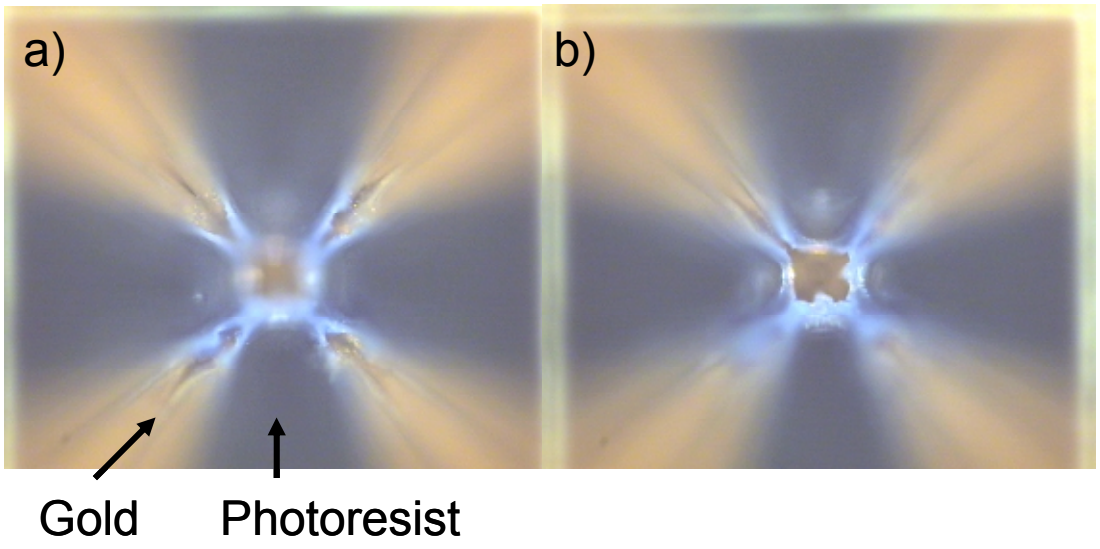


Figure 66: Microscope images of the pyramidal micro-mirrors with patterned electrochemically deposited photoresist before gold etching the flower pattern. The images show the same image with an increasing focal depth. a) shows the focus at the middle depth of the pyramid while b) shows the focus at the apex of the pyramid.

The wafer is then dipped for 1 minute in 80 ^{o}C water to remove the resist residues and to smooth the edges of the resist as shown in Figure 67. The wafers were rinsed in deionised water and dried in a vacuum oven before being de-scummed for 3 minutes in oxygen plasma at 110 ^{o}C.

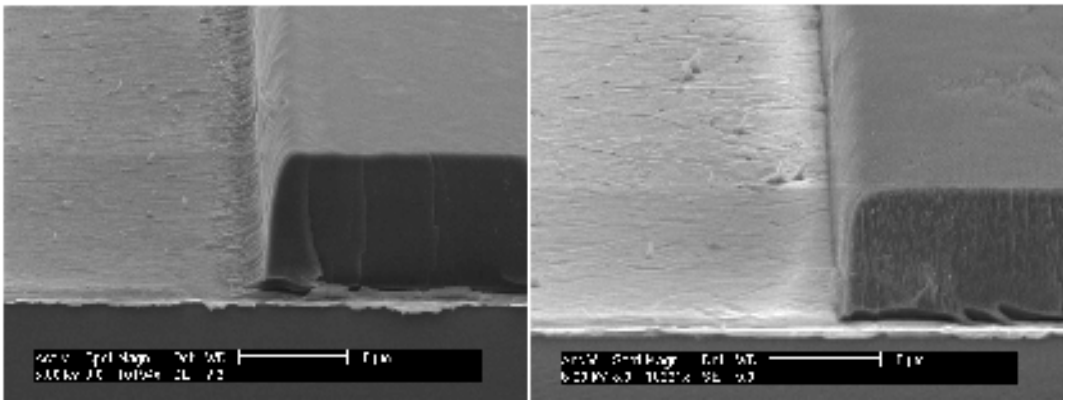


Figure 67: Patterned electrochemically deposited photoresist after standard development (left) and patterned electrochemically deposited photoresist after development and a hot water rinse (right) (Taken from ref [89]).

The exposed gold was removed by a 35 second potassium iodide etch, which is followed by a 5 second etch in transene chromium etchant type 1020 to remove the chromium (Fig. 64h(ii)). The wafers were sprayed for 15 minutes with 50 ^{o}C Eagle

2007 remover, which strips the resist, then placed in an asher for 1 hour at 600 W and 110 ^{o}C (Fig. 64h(iii)). Using this process it was possible to successfully pattern flowers inside the pyramids as shown in Figure 68.

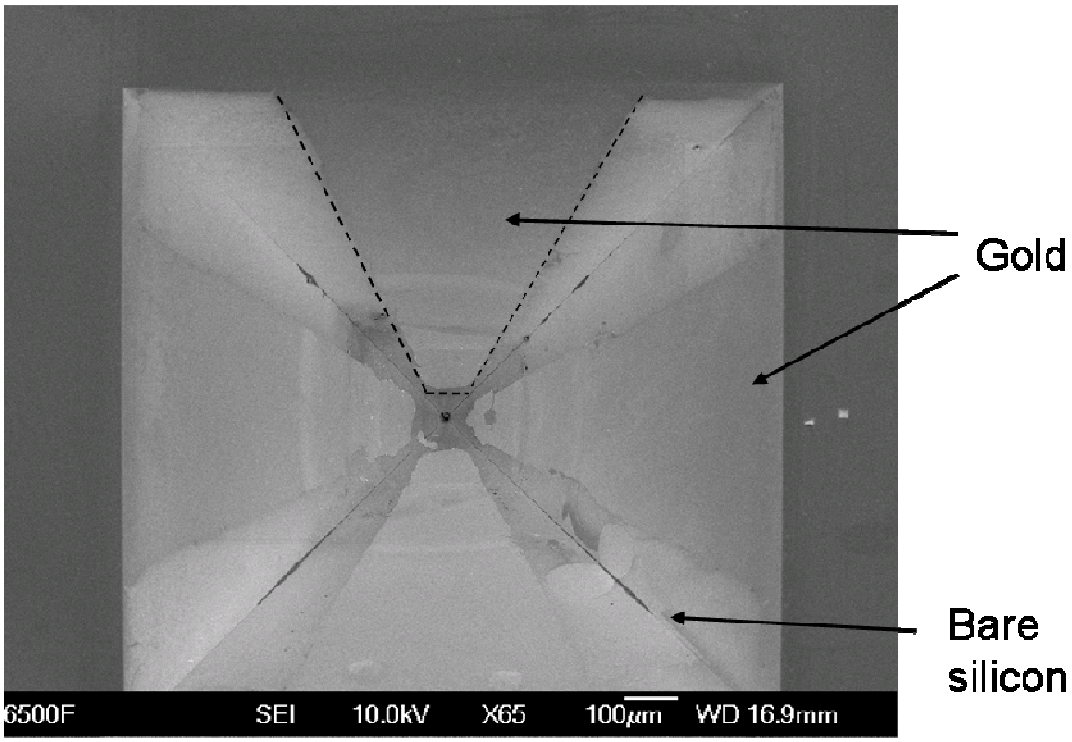


Figure 68: SEM image showing the flower pattern created on the side walls of all the pyramids. Due to difficulty in achieving a uniform exposure of the resist inside the pyramid, resist residue can be seen in the diagonals and at the apex of the pyramid as dark areas. The colour of the silicon surface also varies due to differential charging during the SEM session.

Having created the flower pattern all the wafers were again combined for the final fabrication steps. To finish the fabrication the current carrying wires had to be created. This is done by creating the track pattern on the gold coating and subsequently the wires are electroplated to provide the 3 µm thickness required for carrying the electrical current.

The wire tracks were patterned using optical lithography. Again spinning a uniform layer of resist proved very challenging since the radial flow is interrupted by the presence of the pyramid. However this time the uniformity in the pyramids themselves was not a problem as they were not being patterned. To achieve complete coverage both in the pyramids and in the spin shadow of the pyramids a thick, viscous resist was required, therefore AZ4533 was chosen.

Spin spreading of the resist alone could not be relied upon to ensure the pyramidal etches and the areas behind them were covered, so the wafers were completely flooded with the resist before the spinning began. The wafers were then spun at 500 rpm for 10 seconds followed by 2000 rpm for 30 seconds. This created a 5 µm thick layer in clear areas and varied by approximately ±3 µm where the pyramids caused striation. The photo resist was then exposed using a photo mask to create the isolated wires surrounding the pyramidal pits as shown in Figure 69.

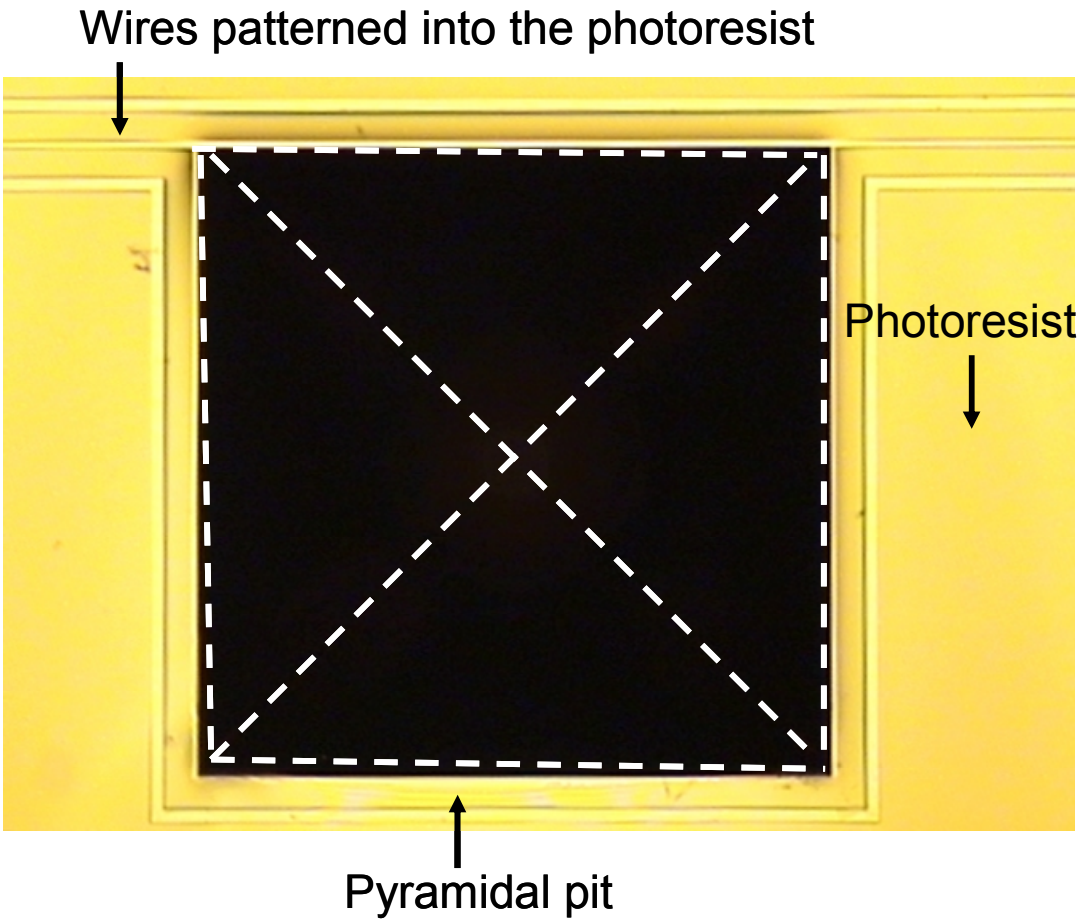


Figure 69: Microscope image showing the resist mask around a pyramid that allows the gold to be wet etched to create isolated wires.

The chromium and gold layer was then patterned using a wet etch. First the gold was etched in potassium iodide for 35 seconds and then the chromium was etched using a commercially available titanium etchant for 5 seconds (Fig. 64i). The resist is then stripped off the whole wafer.

Next the electroplating mould was created on the wafer using AZ9260. Again the wafer had to be flooded with resist to ensure good coverage. The wafers were spun at 500 rpm for 8 seconds followed by 4000 rpm for 30 seconds. This created a 6 μm thick layer of resist, which varies by approximately ±3 μm where the pyramids interfere with the flow (Fig. 64j). The uniformity of the resist substantially improves around pyramids smaller than 1 mm. The thickness variations of the photo-resist led to overexposing which results in a thinning of the wire tracks around the larger pyramids as shown in Figure 70.

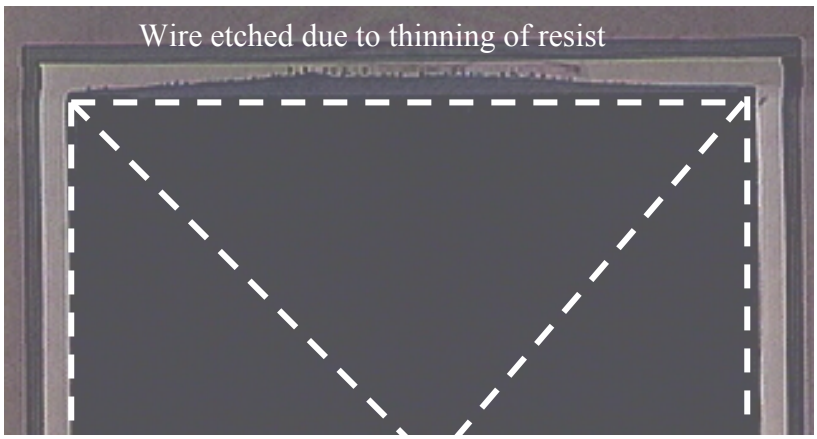


Figure 70: Photograph showing the edge of the pyramid and its circulating wire. Due to poor resist coverage because of the problems of spinning over large topological structures the wire has become etched almost to destruction.

This layer is then exposed at 200 mW/cm^2 for 30 seconds to create the plating mould of a minimum thickness of 3 μm see Figure 71. The electrochemical deposition is controlled by an Autolab PGSTAT30 from Eco Chemie [125]. A commercial cyanide-free gold plating solution containing 10 grams of gold per litre of solution, from Metalor Technologies UK was used. A standard three-electrode setup is used with a platinum counter electrode. The deposition bath is placed in a water bath at 50 ^{o}C and the solution is agitated throughout the deposition process using a magnetic stirrer. The current is fixed at 6 mA, corresponding to a current density of 5 mA/cm^2, and the plating is run for 15.3 minutes to achieve a 3 μm thick gold deposit (Fig. 64k). These figures were chosen as they were shown to give the best results (see chapter 3). Finally, the resist is stripped to leave the free-standing gold wires.

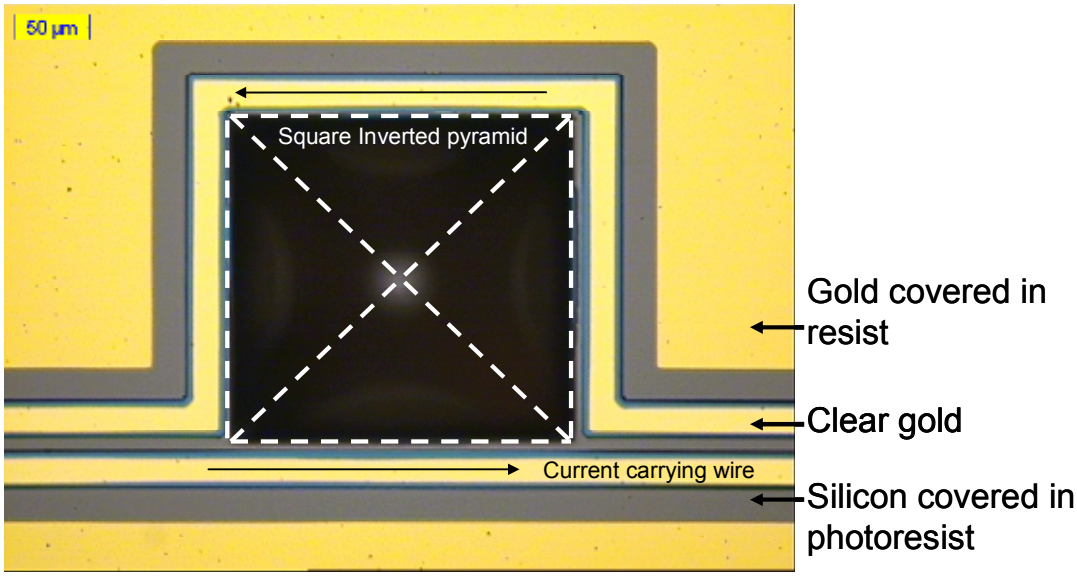


Figure 71: Microscope image of the tracks around the pyramid with the electroplating mould in place all around the wire edges.

4.3. Results

In the fabrication of this batch many problems were overcome. The initial fabrication process was modified until a successful method was produced as described above. The first batch of pyramid micro mirrors was successfully completed. The atom chip that was fabricated has 6 rows of pyramids, ranging in size from 200 µm to 1200 µm, serviced by 12 separate wires to produce the magnetic fields. For pyramids up to 600 µm, the encircling wires have a width of 25 µm. The larger pyramids are serviced by wires of 50 µm width. In total there are 48 pyramid MOTs. The whole chip is packaged into a ceramic pin grid array (CPGA) with multiple wire bonds to bring high currents in and out of the chip and with careful heat sinking to remove the power dissipated. The silicon sidewalls of the pyramids are coated with gold to create micro-mirrors for reflecting the laser light. A photograph of the chip is shown in Figure 72.

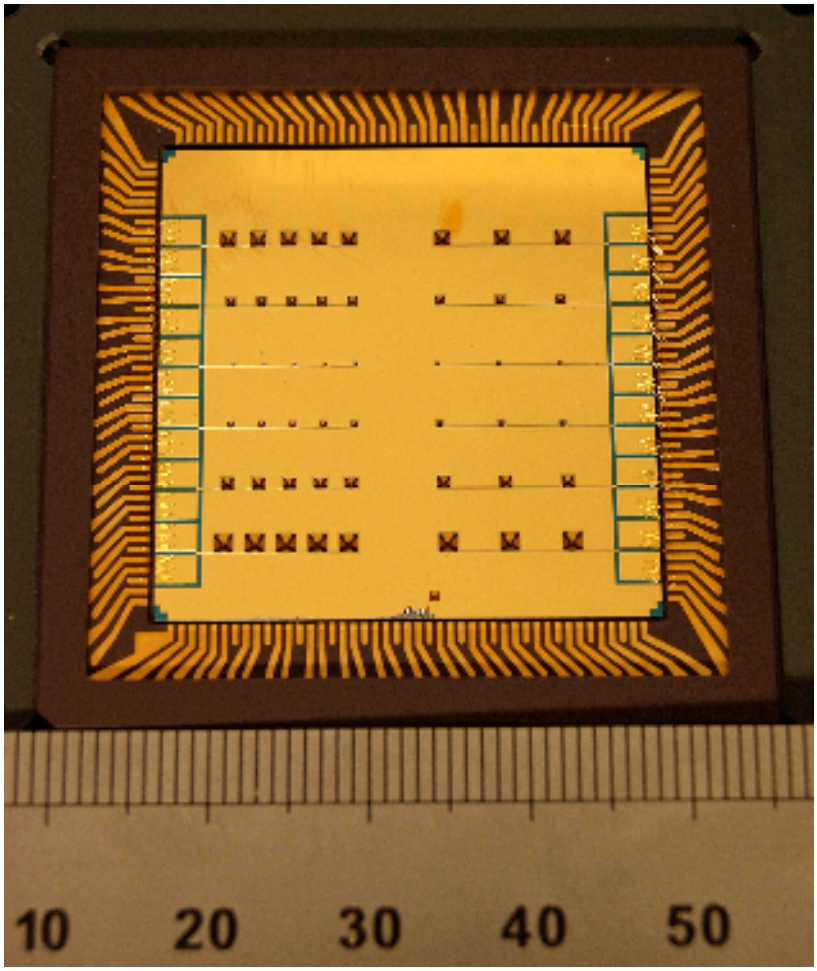


Figure 72: Photograph of the gold, flower design pyramid chip wire bonded into a ceramic pin grid array package. The inside of the pyramids clearly show the flower patterning. Nine bond wires are used on each chip pad to safely allow large currents to be applied.

The biggest problem in the production of these devices is creating a uniform resist layer over the wafer once the deep pyramid etch has been performed. Failure to get a good coverage can result in damage to the wires especially in wires close and around the pyramids. Figure 70 shows a typical problem that can arise when spinning resist over the pyramids. The resist will flow around the pyramid rather than over it creating thinning on the side facing the edge of the wafer and thick waves to the sides. When this is developed it can leave areas uncovered and therefore no longer protected leading to undesired etching.

4.4. Device characterisation

In this section the magnetic and optical properties of the device are characterised. It is demonstrated that the micro-fabricated wires can create the quadrupole magnetic field required for magneto-optical and purely magnetic trapping. The thermal properties of the device are also analysed. These measurements allow the maximum depth and gradient achievable in the trap to be inferred. Finally, it is shown that the patterning of the pyramid coating leads to the desired suppression of Type 3 beams. The measurements shown in section 4.4.1 and 4.4.2 were performed by the project collaborators at Imperial College London.

4.4.1. Magnetic field measurements

The wires on the chip almost form a square loop of side *L* around the pyramid base. In order to calculate the magnetic field of the MOT it is adequate to approximate this to a fully closed loop. Using Biot-Savart law

$$dB = \frac{\mu_o}{4\pi} \frac{Id\hat{l} \times \hat{r}}{r^2} \tag{33}$$

where μ_o is the permeability of free space, I is the current, r is the distance from the wire at which the field is being calculated dl is a vector whose magnitude is equal to the differential element of the wire and dB is the differential contribution of the magnetic field, the magnetic field at the centre of the square loop can be calculated. If a current I is applied, the magnitude of the magnetic field at the centre of the loop is given by:

$$B = \frac{2\sqrt{2}\mu_o I}{\pi L} \tag{34}$$

This was verified on the chip, using a Hall probe (Lakeshore 421 Gaussmeter) to measure the magnetic fields generated around an 800 μm pyramid encircled by a wire

of cross-section 50 µm by 3 µm with a current of 480 mA. The Hall probe was translated horizontally across the loop and vertically away from the surface. The measured position-dependence of the magnitude of the magnetic field is shown in Figure 73. The solid line shows the calculated value based on a closed square loop while the red dots represent the measured data. The two are consistent.

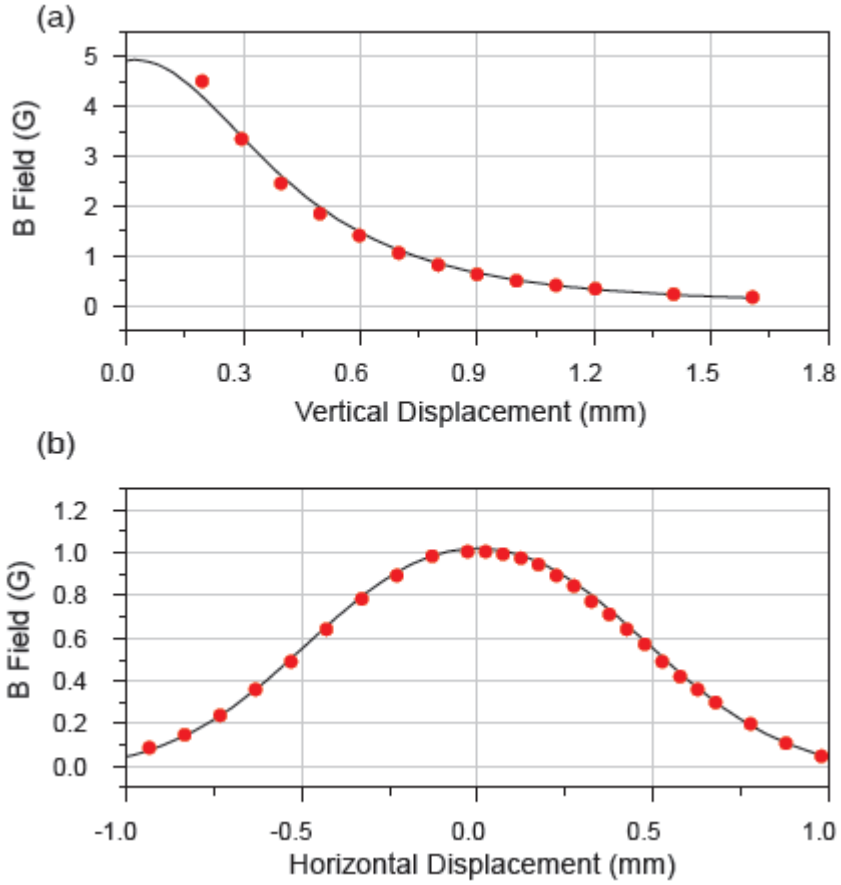


Figure 73: Graph showing the vertical component of the magnetic field above an 800 µm pyramid with 480mA in the wire. Showing the probe a) translated perpendicularly away from the chip surface along the pyramids central axis, b) translated parallel to the chip and the pyramid rows at a height of 0.7 mm, across the centre of the pyramid.

In order to operate an MOT a quadrupole field is required. This can be achieved on the chip by adding a uniform bias field (B_T) acting perpendicular to the chip's surface of

$$B_T = \frac{8\sqrt{2}\mu_o I}{3\pi\sqrt{5}L} = \frac{0.54\mu_o I}{L} \qquad (35)$$

which makes the net field go to zero inside the pyramid, half way between the base and the apex at a distance $\frac{1}{2\sqrt{2}}L$ from the surface of the chip. The field gradient at that point is

$$\frac{dB}{dx} = \frac{26\sqrt{2}B_T}{15L} = \frac{2.45B_T}{L} \tag{36}$$

The small scale of the loop makes it easy to achieve the required gradient of ~30 G/cm with modest currents.

Once atoms have been collected and cooled in the MOT, the light can be switched off. At this point, the magnetic field gradient can provide a purely magnetic trap, with a depth of order $\mu_B B_T$, where μ_B is the magnetic moment of the atom. There are two trapping points, symmetrically placed with respect to the plane of the loop, one inside the pyramid and one outside as shown previously in Figure 63. Their separation can be adjusted by changing the strength of the uniform bias field. The maximum depth and gradient of the trap is limited by heating of the assembled components, as described in the following subsection.

4.4.2. Wire load tests

The current flowing through the chip wires will generate heat due to their finite resistivity, eventually leading to wire failure. This will occur as the wire approaches the melting temperature of gold, 1064 ^{o}C. Far before that, namely at 120 ^{o}C, the epoxy used to bond the silicon chip to the ceramic pin grid array (CPGA) will begin to decompose and outgas, thereby compromising the ultra-high vacuum conditions necessary for the experiments and the stability of the chip. This limiting temperature sets the maximum current that can be run through the wires, and thereby the trap's field and field gradient that can be attained.

With the chip mounted and placed under moderate vacuum (10^{-5} mbar), the quantity of current that could be passed through individual bond wires was examined. Each

bond wire was 50 μm in diameter and 2-3 mm in length. It was found that they blow at approximately 1.8 A, but can survive indefinitely at 1.5 A. Since each chip pad is normally connected by 9 wires in parallel, failure of the bond wires is not a limiting factor. In order to determine the operating currents for the chip wires, the temperature of the assembly at several points was monitored using thermocouples while the temperature of the wire itself was measured by monitoring the increase of its resistance. Passing a current through the 50 μm-wide chip wires, the time it takes for the wire to reach 120 ^{o}C was measured, the results being shown by the filled circles in Figure 74. In all cases the chip itself was much colder than the wire. Below 1 A, the temperature limit was never reached, but at 1.3 A, the wire approached 120 ^{o}C in 10 seconds. For the 25 μm-wide wires, the operation was continuous below 0.5 A and was limited to 10 seconds at 0.75 A, as illustrated by the open squares in Figure 74.

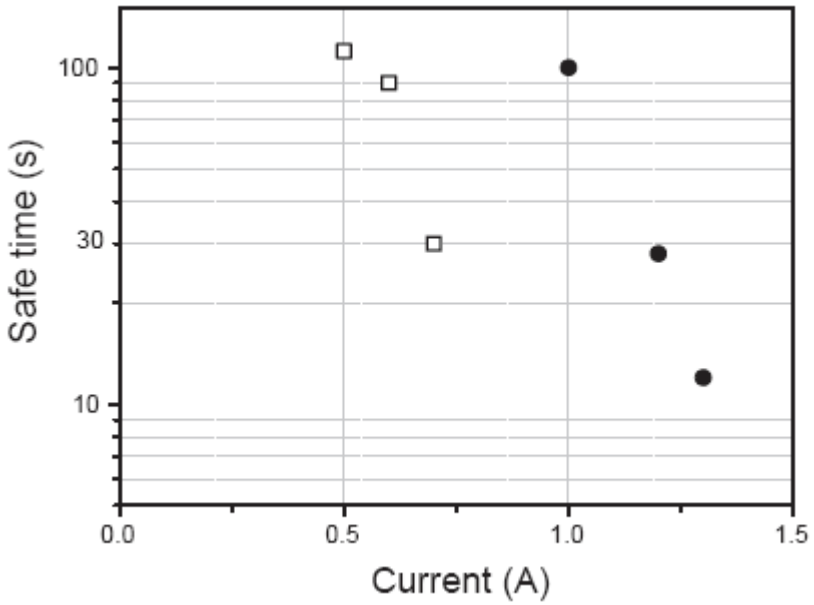


Figure 74: Time taken for the chip wire temperature to reach 120 ^{o}C for various currents. Filled circles represent 50 μm wire wires while open squares represent 25 μm wide wires.

Since a suitable field gradient for the MOT is 0.15 Tm^{-1}, the normal operating current is 5 mA for a 200 μm pyramid and 100 mA for a 1 mm pyramid. At these low currents there is negligible heating of the chip. By contrast, the 1 mm loop needs to operate at 1 A if it is to make a purely magnetic trap for a 100 μK cloud of atoms. This cannot be sustained indefinitely, as shown in Figure 74 but substantially less than one second should be sufficient for most experiments. Since the field scales as I/L, the

situation is even better for purely magnetic trapping in the smaller loops. In the course of these measurements, it was found that the resistivity of the gold wire on the chip is 3.9×10^{-8} Ωm, approximately 1.6 times higher than that of bulk gold [126]. This was expected and is typical of electro-deposited gold [127]. The main consequence is slightly higher power dissipation than would be obtained using the book value for the resistivity.

4.4.3. Optical properties

As discussed previously the flower patterning is designed to remove the type-2 and 3 rays. Pyramids both with and without patterning were therefore imaged with unpolarised light, linearly polarised light with a parallel analyser and linearly polarised light with a crossed analyser.

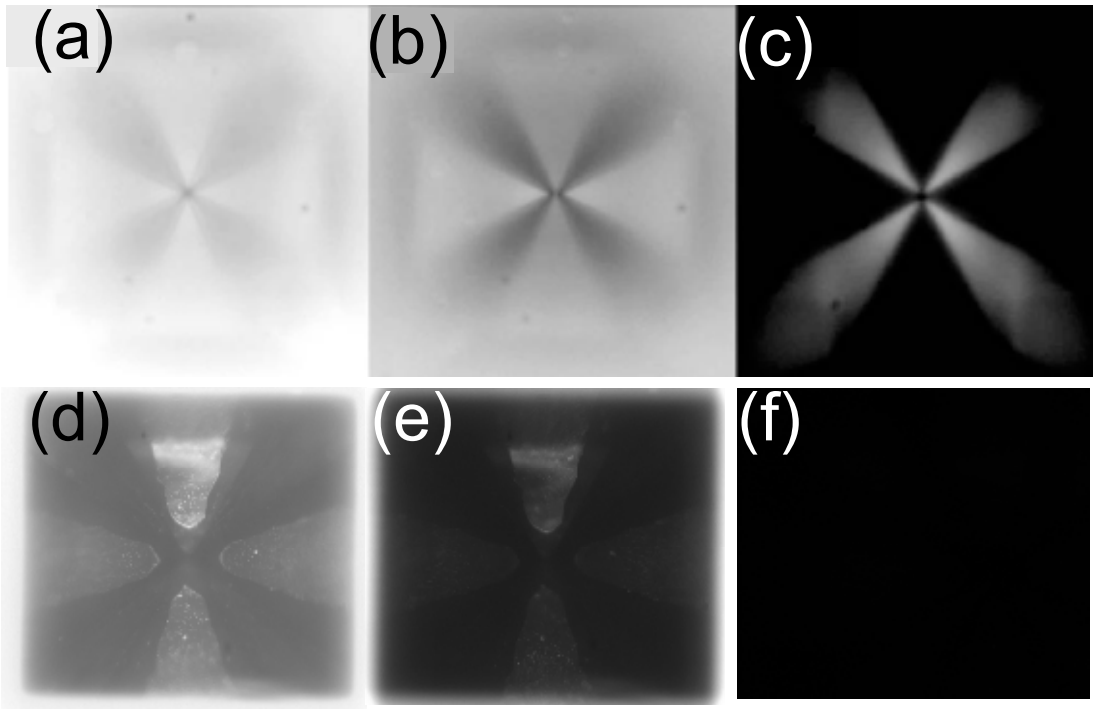


Figure 75: Views of the pyramidal mirror under an optical microscope. The top row shows photographs of unpatterned pyramids, the bottom row shows patterned pyramids. Images (a, d) are without polarizers; (b, e) have parallel polarizer and analyzer and (c, f) have crossed polarizer and analyzer.

Figure 75a shows the image for unpolarized light with the microscope focussed in the

plane of the apex of the pyramid. In this figure most of the area is bright. In Figure 75b an image for linearly polarized light, viewed through a parallel analyser, which suppresses the type 3 contribution is shown. This leads to a reduction in the intensity of reflections from the corner region. In Figure 75c, the analyzer is crossed with the polarizer and only type 3 rays contribute, making the corner region bright. The corresponding intensity patterns observed in a patterned pyramid are shown below in Figure 75d-f. It can clearly be seen in this figure that the type 3 reflections have been removed.

4.5. Conclusion

It has been demonstrated above that pyramidal cavities are ideal candidates for trapping atoms on silicon chips. The exact number of atoms that can be trapped will greatly depend on the operating conditions such as the laser detuning from the atomic transition, the positioning of the magnetic field zero, the balance of the light beams inside the pyramid and the pressure of the atomic vapour. Normally the laser beams of an MOT are one or two centimetres in diameter, whereas these pyramids are less than a millimetre across. According to the well-established model first described by Wieman et al. [128] the number of atoms N captured in an MOT is expected to scale as $N/L^2u_c^4$. Here the L^2 factor derives from the area of the laser beam, which in this case is set by the area of the pyramid opening. The quantity u_c is the capture velocity, i.e. the speed of the fastest atoms captured by the MOT from the thermal background vapour. Using the model of Ref. [128], u_c was calculated numerically, setting the maximum allowed stopping distance equal to the vertical height of the pyramid. The circles in Figure 76 show the results on a log-log plot for a variety of pyramid sizes, with the laser detuning optimised separately to maximise u_c for each size. For pyramids larger than 1mm, the empirical scaling law $u_c/L^{0.37}$ was found, leading to the result $N/L^{3.48}$. When the pyramids are smaller than that, the atom number drops more rapidly. It has been shown in a previous experiment [121] that a 16 mm pyramid made from glass blocks can capture large clouds of atoms (~1.6 x $10^{8)}$. With the help of this model, it was extrapolated from the 16 mm result to predict that a 1 mm

pyramid will capture some $6x10^3$ atoms. The smallest pyramids on this chip, having L = 0.2 mm, are expected, by the same argument to collect approximately 25 atoms.

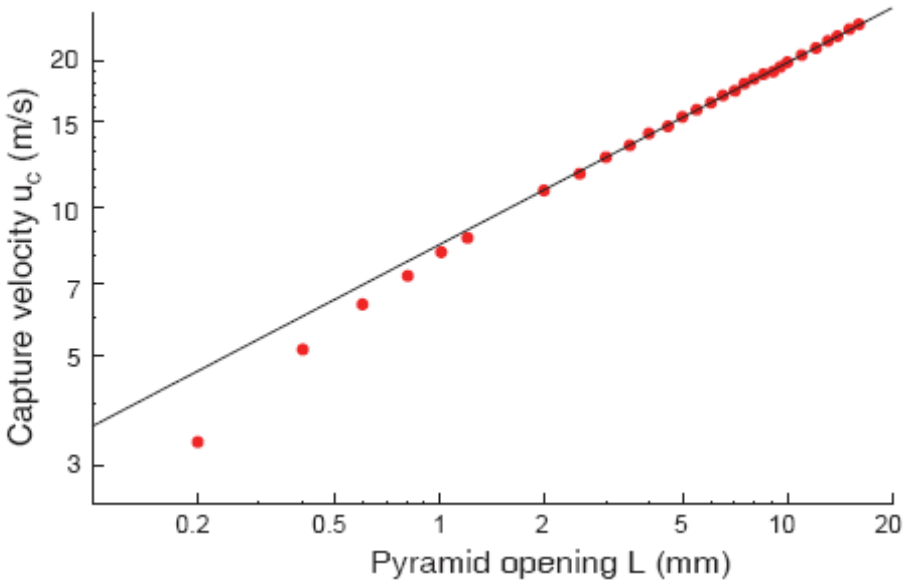


Figure 76: Graph showing the capture velocity against the size of the pyramid opening. This is calculated by numerical integration using the model described in [128].

Although this model is a reasonable estimate, it does neglect some aspects of the full 3-dimensional geometry. For example, it assumes that the atoms of the vapour have the normal thermal distribution close to the walls of the pyramid and it neglects the polarisation gradients in the laser field, which lead to additional Sisyphus cooling [57]. Experiments will have to determine how many atoms are actually captured. The number of atoms needed depends on the application. At one extreme, with an array of small clouds, each containing perhaps 100 atoms, the relative displacement of the clouds could provide a map of local magnetic field variations or be used to sense inertial forces. At the other extreme, the pyramids could serve as single-atom sources for loading integrated optical cavities which has recently been demonstrated in [129]. This would permit the production of single photons on demand for applications in quantum information processing.

A new approach for trapping atoms directly on a silicon chip was developed, based on the use of pyramidal mirrors surrounded by gold electroplated wires. It is shown that this can be achieved in a simple and elegant way which greatly reduces the cost and complexity on of an atom chip experiment.

An atom chip of 48 hollow micro-pyramids was micro-fabricated and packaged into a ceramic pin-grid array, and its optical and magnetic properties were tested. It was found that the chip wires can sustain high currents capable of supporting magnetic field gradients suitable for a variety of applications. The use of electrochemical deposition of photoresist allowed us to pattern a flower design on the reflective coating, a feature necessary for achieving the proper conditions for a magneto-optical trap.

A theoretical analysis of the pyramidal cavities was also performed and shows that arrays of atom clouds of different numbers can be trapped and further magnetically transported on a silicon chip. This represents an important step towards atom chip integration.

Chapter 5

Fabrication of Hemispherical Micro-cavities for Single Atom Detection

An important part of creating atom chips is the detection of the atoms themselves. Some of the proposed atom chip experiments such as an atomic interferometer would greatly benefit from measuring atom statistics and correlations at single atom levels [130]. Also, if single atoms are to be used as qubits then single atom detectors must be developed.

A single laser beam is not sensitive enough to enable single atom detection. In order to achieve this, the optical sensitivity must be increased. This can be done by making the light beam travel multiple times through the region the atoms are travelling, as in an optical cavity. Presented here is a method for creating a planar-concave micro-cavity that can be fabricated into a silicon wafer and therefore easily integrated into atom chips.

In this chapter the design, fabrication and results of the hemispherical micro-cavities is presented. First, the design parameters and decisions are described. Then the fabrication and integration of the hemispherical micro-cavities into an atom guide is discussed. Finally data is presented showing the feasibility of the fabricated devices, some of which was obtained by the collaborators at Imperial College London

5.1. Design

Using the methods investigated previously [131] hemispherical micro-cavities were created in silicon wafers. The cavity is formed by combining a planar optical fibre with a reflective coating above the hemispherical micro cavity as shown in Figure 77.

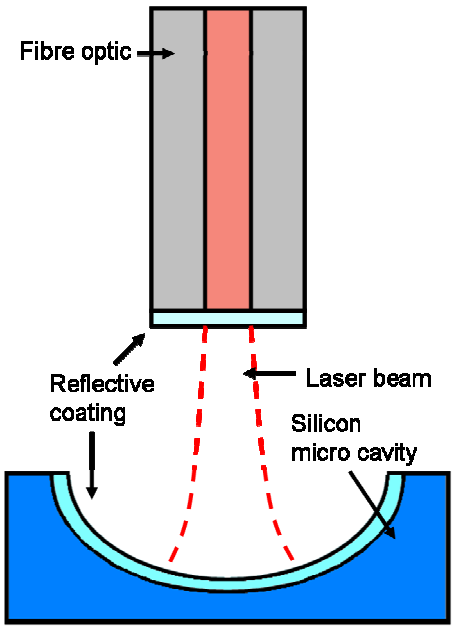


Figure 77: Schematic diagram of the hemispherical optical cavity.

These micro-cavities are easily tuneable and have a high finesse. The structure also allows atoms direct access to the high intensity part of the field, which increases the interaction strength between the photons. This design can easily be scaled to any size due to the micro fabrication methods used. Combined with the advances in producing waveguides as well as three dimensional actuators [75] these cavities are ideally suited for integration into MEMS fabricated devices.

The most important factors in the function of the cavities are the surface roughness and the shape profile both of which have a strong dependence on the processing parameters. In order to study the evolution and controlling factors of these parameters an experiment was setup that created a large array of cavities with different initial openings and allowing different etching times to be studied.

As a feasibility study the mirrors are integrated into an atom guide, the fabrication of which is discussed in section 5.3. The main constraint of this process is that the hemispherical mirrors must have atomically smooth surfaces to act as a high finesse micro-cavity. This means that once formed they must be protected at all times from future processing steps while still allowing them to be uncovered, undamaged for the final device.

5.2. Fabrication

To create the micro mirror templates P-type silicon wafers, <100> orientated, with a thickness of 600 µm were used. The process flow is shown in Figure 78. A 60 nm layer of silicon nitride was deposited over the wafer by LPCVD. The wafers were then primed using hexamethyldisilazane (HMDS) vapour and coated with a 1.3 µm thick photoresist HPR-504. The wafers were then lithographically patterned to form circular openings of sizes varying from 20 – 80 µm diameter. The silicon nitride layer was then opened using an anisotropic RIE etch, see figure 60a. The selectivity of this etch between silicon and silicon nitride is low, so care must be taken not to over-etch into the silicon wafer. The etch was performed using an RF power of 515 W, a gas flow of CHF_3 5 sccm, CF_4 25 sccm, Ar 60 sccm and a gas pressure of 40 mTorr for 20 seconds. This recipe was taken from a data base of standard etches from Innos Ltd.

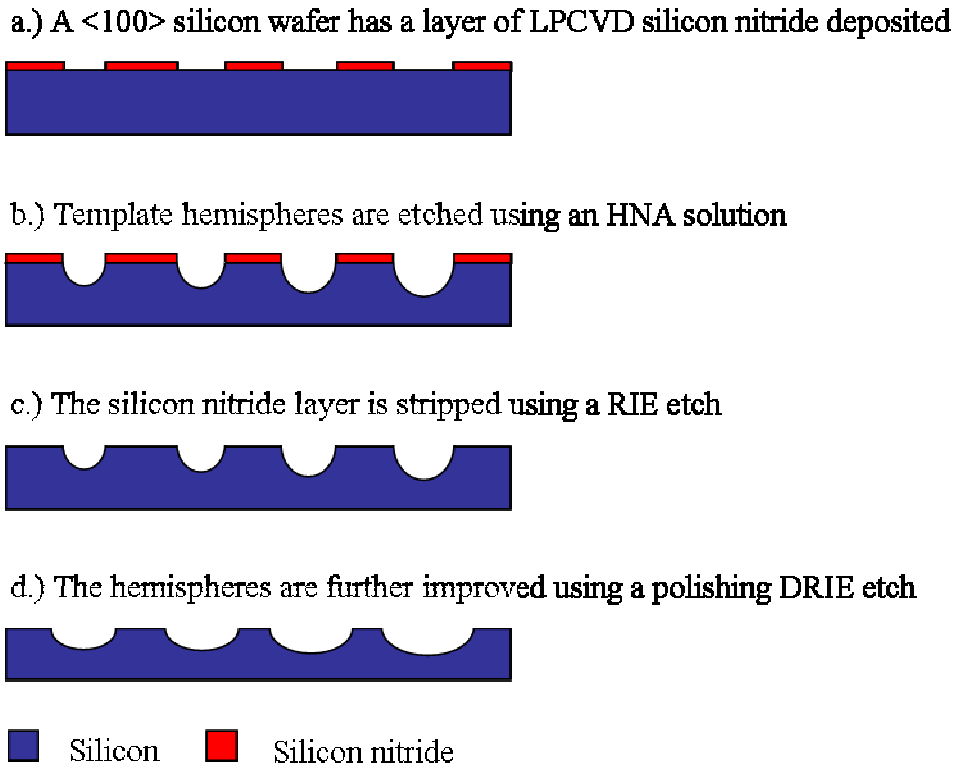


Figure 78: The fabrication process for the silicon microcavities.

The initial hemispherical shape was fabricated by wet etching all the wafers using a wet hydrofluoric, nitric and acetic acid (HNA) etch, see Figure 78b. The etch rate and

shape profile of the resultant silicon surface is highly dependant on the composition and agitation of the solution [132, 133]. In our earlier work [72, 131] a composition was developed that gave repeatable surface profiles with 6 nm RMS roughness. This recipe consisted of HNA in the following composition; 30 parts hydrofluoric acid (49 % concentration), 43 parts Nitric acid (70 % concentration) and 27 parts acetic acid (99.5 % concentration). Using this solution the wafers were etched for 2 minutes at room temperature and under constant agitation. This resulted in an approximately hemispherical template as shown in Figure 79.

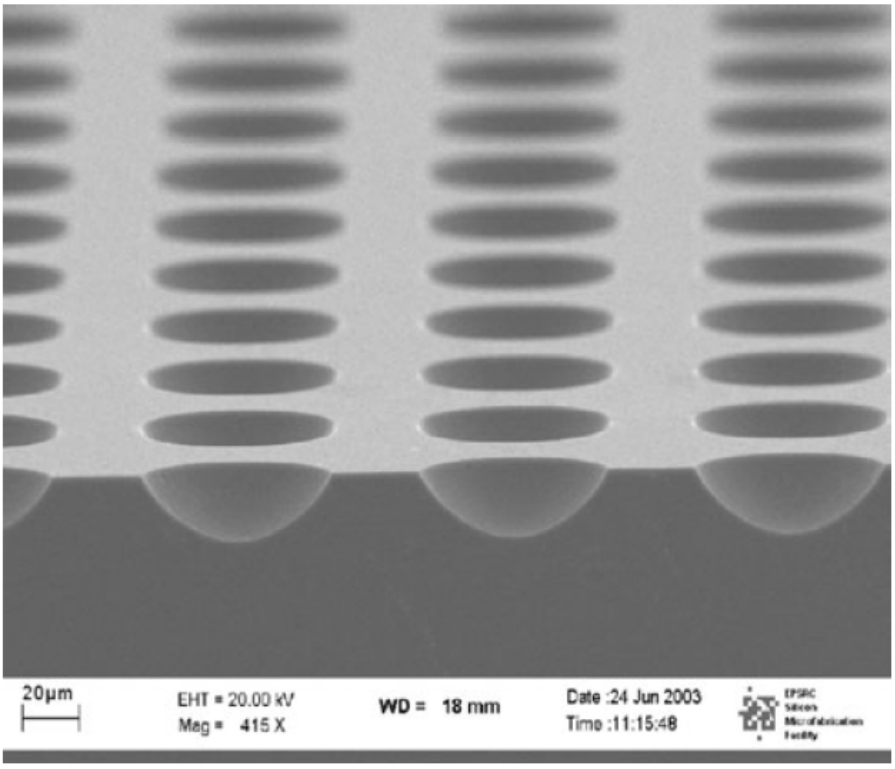


Figure 79: SEM image showing a cross-sectional cut through micro-cavities 21 μm deep. These are formed by etching through 15 μm holes in a SiO2 mask for 72 min using a 9:75:30 HNA solution. The mirrors are 67 μm in diameter.

While this template is roughly hemispherical, anisotropies can clearly be seen when examined closer, see Figure 80. The roughness at this point of the fabrication process was investigated with an AFM and yielded a RMS roughness of 5.4 nm.

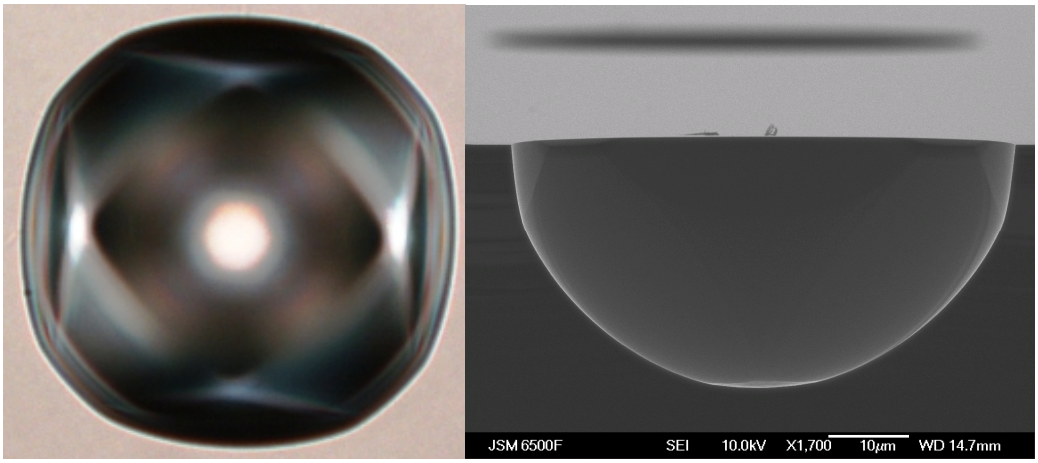


Figure 80: Left, An optical microscope image of a 20 μm initial opening hemisphere wet etched for 2 minutes in HNA. Right, An SEM image of the cross section of the cavity. Both images clearly show anisotropy.

With the template shape created the wafers were then polished to reduce the surface roughness. Studies into the effect of inductively coupled plasma (ICP) polishing etches both with and without masks have been performed [134, 135]. These studies have shown that maskless etches produce a more consistent shape while allowing other parameters to vary. A maskless etch was therefore performed. To achieve this, the masking layer of silicon nitride had to be stripped. This was done using the same recipe as previously stated to create the initial silicon nitride openings. While such an etch slightly etched the micro-cavities, tests on using a 160 ^{o}C orthophosphoric acid dip showed this etch caused visible degradation of the silicon surface so was less suitable, see Figure 78c.

The wafers were then subjected to a maskless isotropic ICP polishing etch, on an advanced silicon etcher (ASE) from STS, see Figure 78d. A set of parameters chosen from reference [134] was used which produced the lowest roughness value (~ 7 Å). This recipe was as follows; coil power 3000 W, platen power 16 W, pressure 10 mTorr, SF_6 flow rate 200 sccm and chuck temperature of 20 ^{o}C. The first wafer was etched for 2 minutes with each subsequent wafer being progressively etched for 2 minutes longer than the last, up to the maximum of 38 minutes. This allowed the time evolution of the etch to be easily studied.

Having created series of micro-cavities which allow the study of their formation and properties, a more practical fabrication was undertaken. Using the previous

fabrication as a starting point a process was developed that would allow them to be integrated into an atom chip.

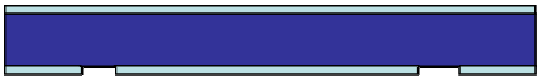
5.2.1. Fabrication of silicon micro-cavities integrated into atom chips

With integration into an atom chip, the micro-cavities can be used in a wide range of experiments such as single atom detection. The ability to guide atoms into the microcavities would create a more useful tool for future experiments. This integration will also show the practicality of the fabrication process developed for use in many MEMS structures. It is therefore important to integrate these cavities into the existing atom guides, the design and fabrication of which was discussed in section 3.

The main constraint of this process is that the hemispherical mirrors must have atomically smooth surfaces to act as a high finesse micro-cavity. This means that once formed they must be protected at all times from future processing steps while still allowing them to be uncovered undamaged for the final device. With this in mind the fabrication must be significantly modified to produce a suitable integrated micro-cavity.

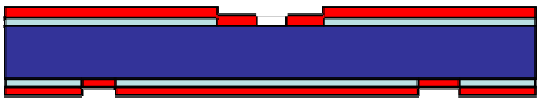
a.) A silicon substrate has a thermal oxide grown

b.) Backside alignment marks are RIE etched the oxide layer

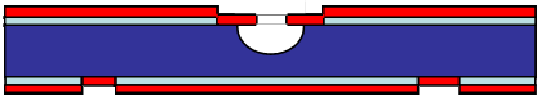


c.) The front side oxide layer is patterned

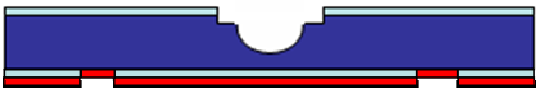
d.) Silicon nitride is deposited on both sides and patterned on the front side



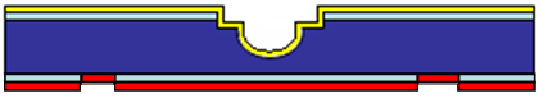
e.) The silicon is etched using an HNA solution



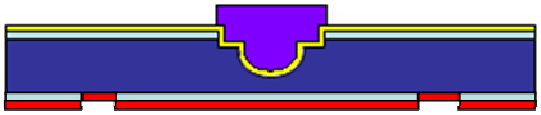
f.) The silicon nitride is stripped and the silicon is etched using an ICP isotropic etch.



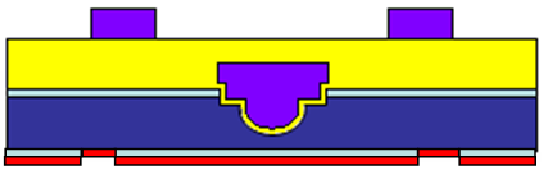
g.) A Chromium and Gold layer is sputtered



h.) Photoresist is spun and patterned to protect the cavity



i.) A thick layer of gold is sputtered and photoresist is spun and patterned



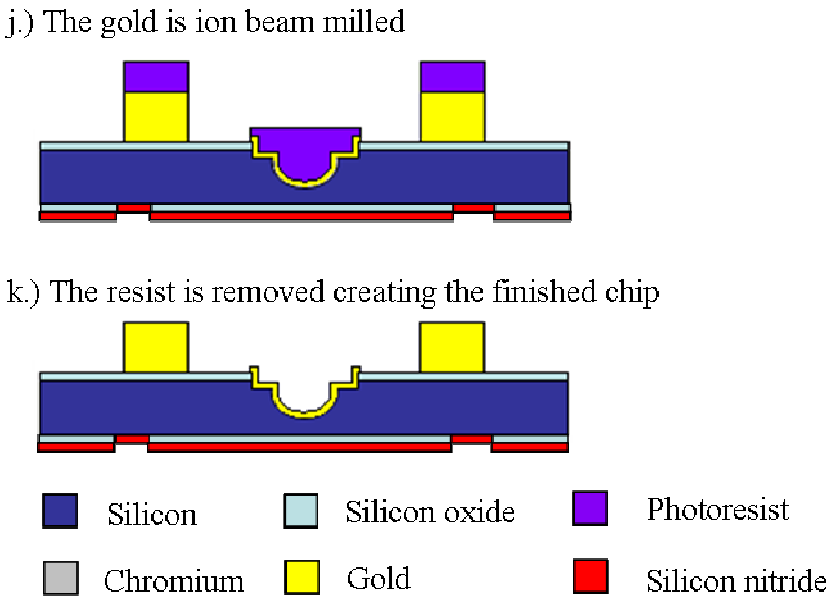


Figure 81: Process flow for the creation of hemispherical micro-cavities.

To create the micro mirror templates P-type silicon wafers, <100> orientated, with a thickness of 600 µm were again used. The process flow is shown in Figure 81. A 100 nm layer of silicon oxide was grown by thermal oxidation (Fig 81a). Next, backside alignment marks had to be created due to the aggressive front side etches that are used. To achieve this, the wafers were first primed using hexamethyldisilazane (HMDS) vapour and then coated with a 1.3 µm thick photoresist HPR-504 on the backside. The wafers were then lithographically patterned to form the alignment marks and the silicon oxide layer was then opened using an anisotropic RIE etch (Fig 81b). Next, the resist was stripped in the asher and the wafers were cleaned in fuming nitric acid.

The wafers were again spun with 1.3 µm of HPR504, this time on the front sides and again patterned. The wafers were then RIE etched to open a rectangle in the oxide layer on the fronts where the hemispherical micro-cavities will be created (Fig 81c). The wafers then had 100nm of LPCVD silicon nitride deposited on both sides of the wafer. This both protects the backside alignment marks and forms the mask for the hemispherical micro-cavities etch. Once again the wafers were spun with 1.3 µm of HPR504 and patterned. This allowed a silicon nitride RIE etch to open small holes in the nitride layer forming the openings where the hemispherical micro-cavities would be created (Fig 81d).

The wafers are now ready for the hemispherical cavities to be created. This is achieved using the same HNA mixture as mentioned in section 5.2. The mixture is placed onto a shaking table and the wafers etched for 2 minutes (Fig 81e). The masking layer of silicon nitride is then stripped off using the same RIE etch recipe as was used to create the initial openings.

The wafers were then subjected to a maskless isotropic ICP polishing etch, on an advanced silicon etcher from STS. This was done using the same recipe as discussed in section 5.2 (Fig 81e). This has the effect of making the cavities shallower and smoother. The wafers are cleaned using fuming nitric acid. A thin layer of 40 nm chromium and 60 nm gold was evaporated to give the mirrors a reflective coating (Fig 81g). This layer has to be protected for all future processing to ensure it keeps its high reflectivity. This is achieved by spinning 6 μm of AZ9260 onto the wafers and developing it so only the hemispherical mirrors have a resist coating (Fig 81h). This serves as the protective layer and gives a 2.2 μm tolerance for the ion beam milling stage performed later in the processing.

With the hemispherical micro-cavities protected the gold wires used for guiding the atoms can be created. First a 5 μm layer of gold was sputtered onto the wafers. The sputtering was done using a Kurt J. Lester sputterer and controlled using a PFG 1500 DC 1.5 kW power supply. The sputtering target used was a disk of 99.999 % purity gold. To achieve this thickness, a power of 100 W and argon flow rate of 10 sccm was used, which produced a rate of 23 nm/min.

The wafers were spun with AZ9260 at 500 rpm for 10 seconds followed by 6000 rpm for 60 seconds. This created a 5.5 μm thick layer. This layer was then patterned to protect the gold which would form the wires (Fig 81i). The wires were then ion beam milled into the gold whilst simultaneously uncovering the layer of resist protecting the micro-cavities. This was done using an Ionfab 300+ from Oxford Instruments (Fig 81j). The Ionfab machine only has the capability to load 4 inch wafers. This combined with a limited number of processed wafers meant the individual chips were cleaved off the wafer and milled separately. This allowed the milling to be optimised

without ruining all the samples. In order to improve the thermal contact of this wafer fragment a silicone paste was used on the back of the chip.

Initial milling tests showed that during this process the resist became burnt and blackened. This made it very hard to remove completely from the wafer, while leaving the optically reflective surfaces needed intact. With the wafer cooling already at the maximum another solution had to be used. It was found that if the milling was performed in 10 minute steps with 5 minute cooling stages, the resist did not become as burnt and was therefore easier to remove. The resist was removed using a 10 minute oxygen plasma ash. This was performed in the RIE 80+ etcher using 10 sccm of O_2 at 100 W and 50 mTorr pressure. This was followed by a 30 minute fuming nitric acid clean to remove the remaining resist (Fig 5k).

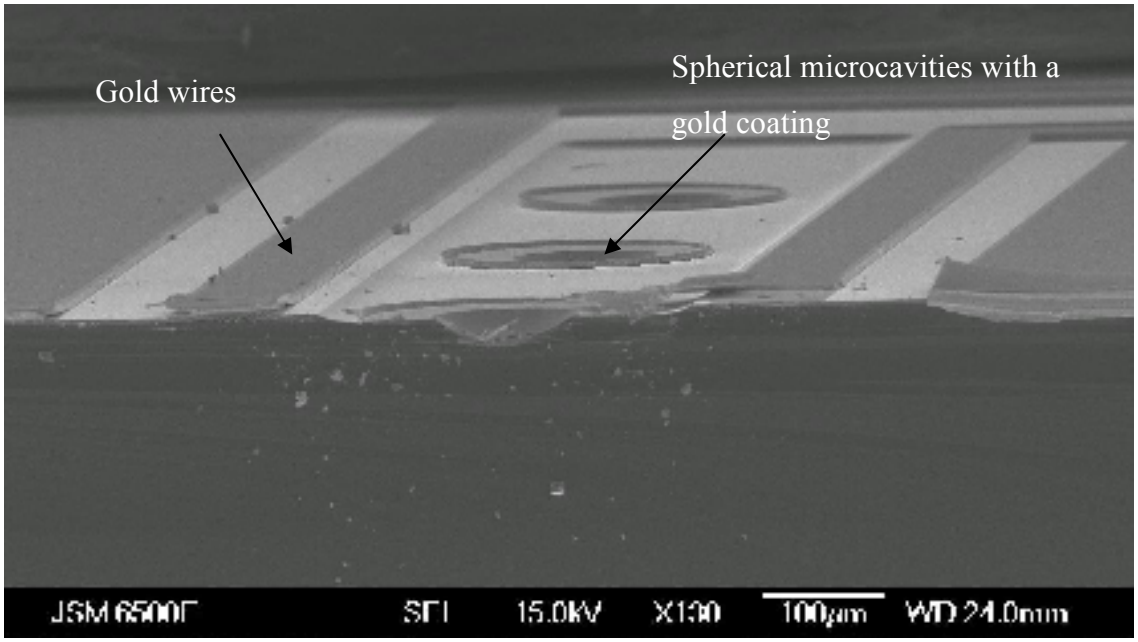


Figure 82: SEM image of the final atom chip. The image shows a cross section of a micro-cavity with gold microwires forming an atom guide positioned on either side.

5.3. Fabrication results

This fabrication produced arrays of hemispherical micro-cavities from varying initial opening sizes and with varying etch times. Using this batch the effects of the ICP etch on the micro cavity formation can be studied. The two most important factors in the micro-cavities are the surface roughness and the shape profile both of which affect

the performance of the cavities. The shape will affect the mode created, while the surface quality will affect the reflectivity.

5.3.1. Shape Results

Here, the initial shape created by the HNA wet etch, as well as the evolution of the ICP etching on the profile of the micro-cavities, was investigated. First the 2D circular opening of the micro mirrors is studied then 2D profiles into the cavity are presented before finally the profile of the 3D cavity as a whole is investigated.

5.3.1.1. 2D opening

The first noticeable property of the cavities openings is that they are not perfectly circular. The etches used are termed isotropic, however this cannot be strictly true if the results are not circular. The origin and extent of this anisotropy is therefore an important factor in making a hemispherical cavity. To characterise this anisotropy within the openings of the hemispherical etches, digitalised optical microscope images were used. The resolution of these images was 0.16 μm/pixel, except for two sets of data. The resolution was 0.08 μm/pixel on the smallest hemisphere (a = 20 μm and t = 0, where a is the initial opening size and t is the ICP etching time) and 0.4 μm on the biggest hemispheres (when $a \geq 50$ and $t \geq 24$).

The edge point was determined by first converting the image into black and white using Corel Photo-Paint 12 while setting the tonal threshold to a constant for each image. The image was then roughly cropped so only the micro-cavity itself was present. Finally the bright central spot was removed so only one edge was present. This was done to simplify the programming. The image was then run through an edge finding algorithm in Matlab (see appendix 1). A typical set of images obtained through this process is shown in Figure 83.

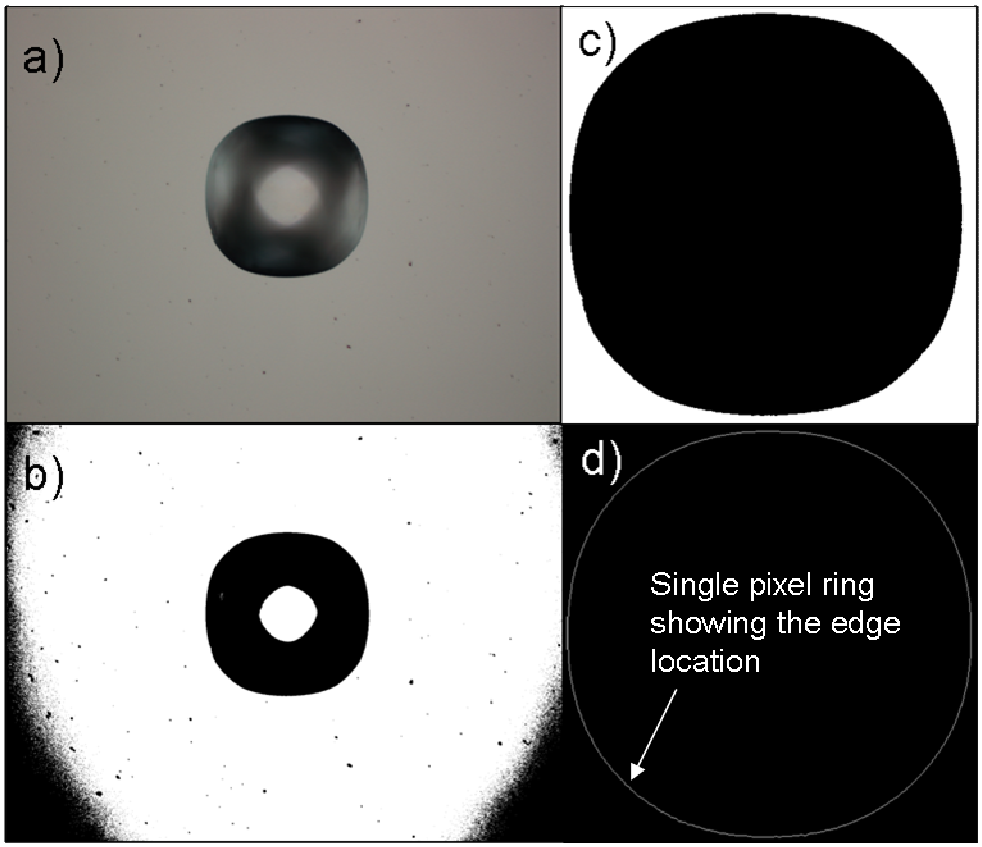


Figure 83: Images showing the process steps used to calculate the radius of the spherical micro-cavities. a) shows the image of a micro-cavity taken via a microscope b) shows the image turned into a 2 tone black and white image c) shows the image after it had been cropped and the central light spot removed d) shows the image after being processed through a Matlab edge finding algorithm.

The edge position for each pixel was then converted into polar coordinates allowing the radius for each set of angles (θ) to be calculated. Figure 84 shows how the conversion into polar coordinates was performed giving the zero point and direction theta was taken. This process gave approximately 2500 points per image. Using this data the anisotropy can be clearly plotted.

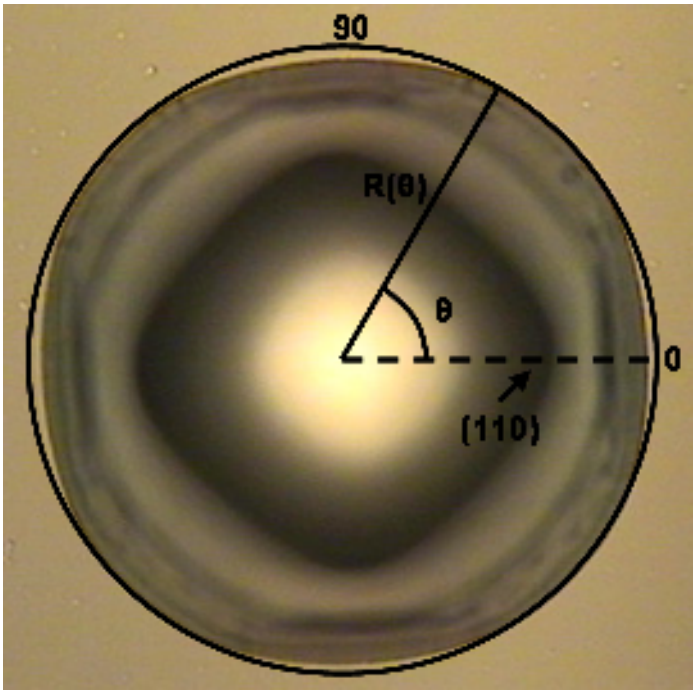


Figure 84: Representation of how the data was recorded showing the zero point and direction theta was measured.

Although both the wet etch in HNA and the ICP etch is considered isotropic, anisotropy is clearly seen when compared to a perfect circular opening. The initial wet etched template shows four fold symmetry, as shown in Figure 85. This is to be expected as silicon has a diamond cubic structure. This data is in agreement with results presented by Svetovoy et al. [136]. They also showed that the data could be fitted to a Fourier series with four fold symmetry which only allows non imaginary results:

$$R(\theta) = R_o + \sum_{n=1}^{\infty} R_n \cos(4n\theta) \qquad (37)$$

In this equation R_o represents a completely isotropic etch while R_n represents the anisotropy present and theta represents the angle at which the radius is calculated. The fitting of the data, from a 20 μm initial opening microcavity with no ICP etching, to equation 37 is presented in Figure 85.

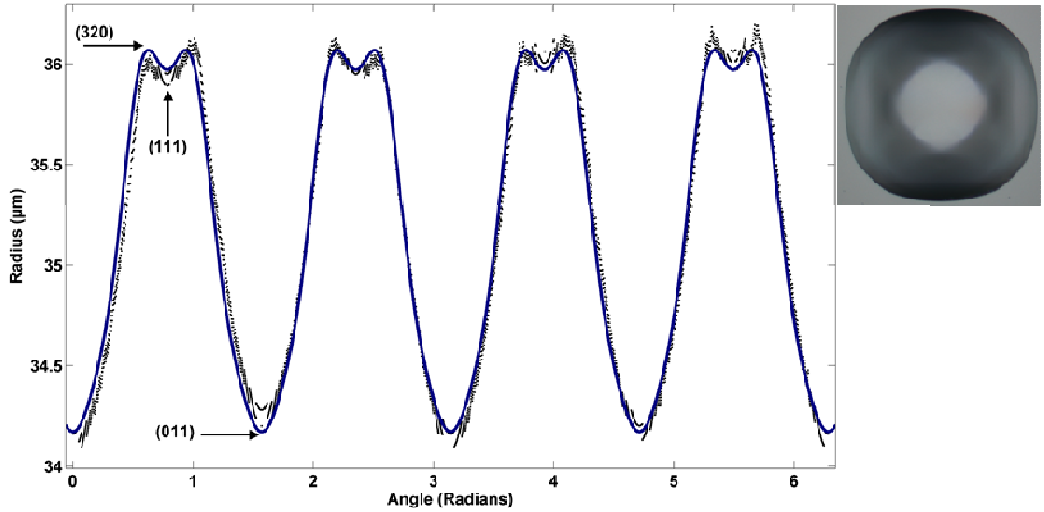


Figure 85: Graph of the 20µm initial opening hemisphere showing the anisotropy of the 2D circular opening, after a two minute wet HNA etch, as a function of the angle. The data has been fitted to equation 37. The raw data is shown as black circles while the fitting is shown as a solid blue line. The crystal planes for the points of significance are also shown. The optical image is also shown in the top right.

If the etch was truly isotropic then the graph would show a flat line at a given radius; however, the radius can be seen to fluctuate sinusoidally by ±0.8 µm. Minima with respect to etch rate are seen at the angles corresponding to the {011} crystal planes. Local minima can also be seen in the {111} planes leaving maximuma at the angles corresponding to the {320} planes. The data points departing from the fitting line at the 0, 1.57, 3.14 and 4.71 radians are present due to image processing. During the processing a limited pixel resolution is possible. This has the effect of flattening the edges making the image slightly squarer than the real cavities which in turn results in the disjointed steps in the data.

Having created the hemispherical template using the HNA wet etch, a maskless DRIE etch was performed. This is done to reduce the surface roughness, but it also has an effect on the shape. The most obvious affect is to increase the mean radius of the hemispheres as shown in Figure 86. The initial opening size has no effect on this rate of increase as this is a maskless blanket etch.

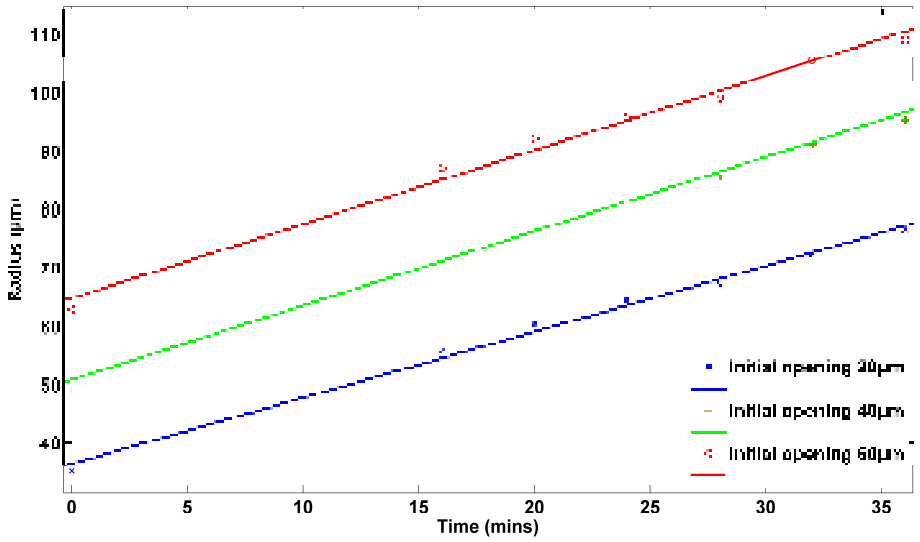


Figure 86: Graph of the 20µm (Blue) 40µm (Green) and 60µm (Red) initial opening hemispheres showing the mean radius of the 2D circular opening of the etch as a function of ICP etching time.

The mean radius increases linearly with time etched as expected. It is only when the variation in the radius as a function of angle is plotted that the anisotropy can be observed. Plotting the radius against angle reveals the difference in the etching characteristics between the HNA wet etch and the DRIE polishing etch as shown in Figure 87.

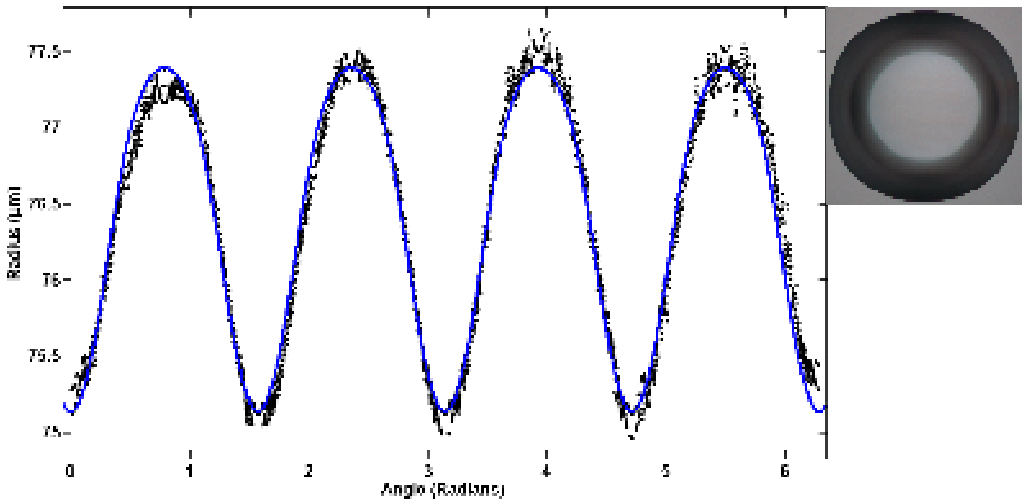


Figure 87: Graph showing the 20µm initial opening hemisphere showing the anisotropy in the 2D circular opening created after a 36 minute ICP etch on the wet etched cavities. The data has been fitted to equation 37. The raw data is shown as black circles while the fitting is shown as a solid blue line An optical image is also shown at top right.

The shape of this profile is different from that seen after wet etching in HNA alone. The slowing of the etch rate around the {111} silicon crystal planes shown previously in Figure 85 is no longer present. This is clearly shown by the change from a local minimum to a maximum at this angle. Graphs for other values of initial opening are not shown as they follow the same pattern as those presented for an initial opening of 20 μm.

The increased spread in the data points when theta is greater than 180 degrees is due to the wafer being slightly non uniform causing a small slope which means that both sides of the cavity can never be in correct focus at the same time. The variation between the maximum and minimum increases with time showing the {111} planes are etching faster than the {011} planes during the DRIE etch. To show this the variation between the maximum and minimum, the percentage deviation from a perfect circle is plotted as shown in Figure 88. This deviation increases linearly with time etched. This means the ICP etching does not improve the circularity of the opening but actually makes it worse showing that neither the wet or dry etch is isotropic.

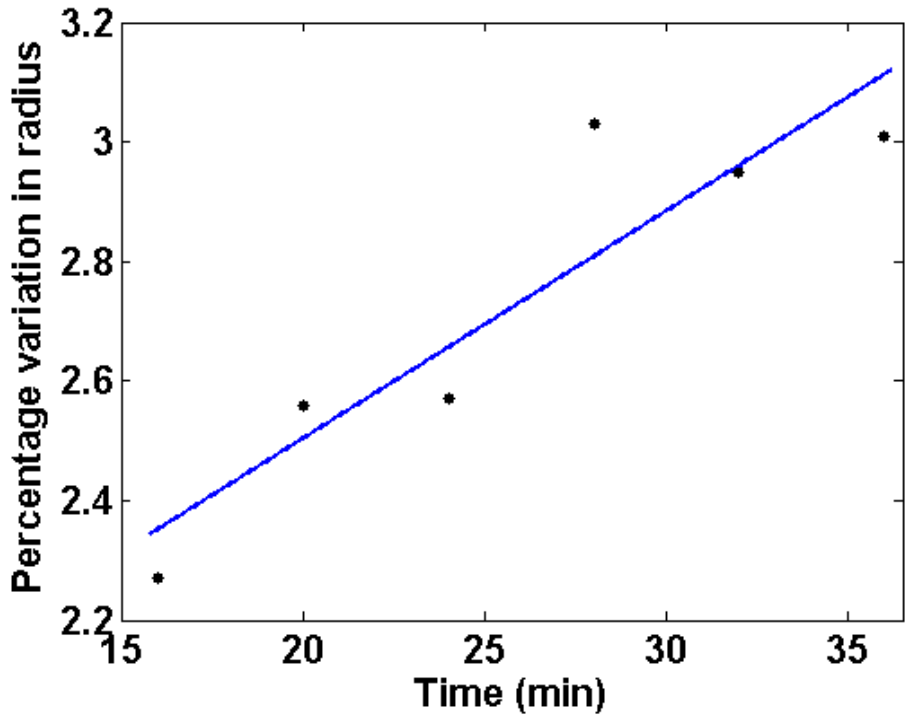


Figure 88: Graph showing the percentage variation from a perfect circle as a function of ICP etching time.

Next the harmonics R_n were analysed as a function of etching time. Figure 89 shows the variation of the first four harmonics with time for an initial opening of 20 µm. This data clearly shows an increase in the magnitude of the first harmonic as a function of etching time. This is to be expected as the etch has been shown to be creating a less isotropic shape with increasing time. It also can be noted that the second harmonic is decreasing with etch time.

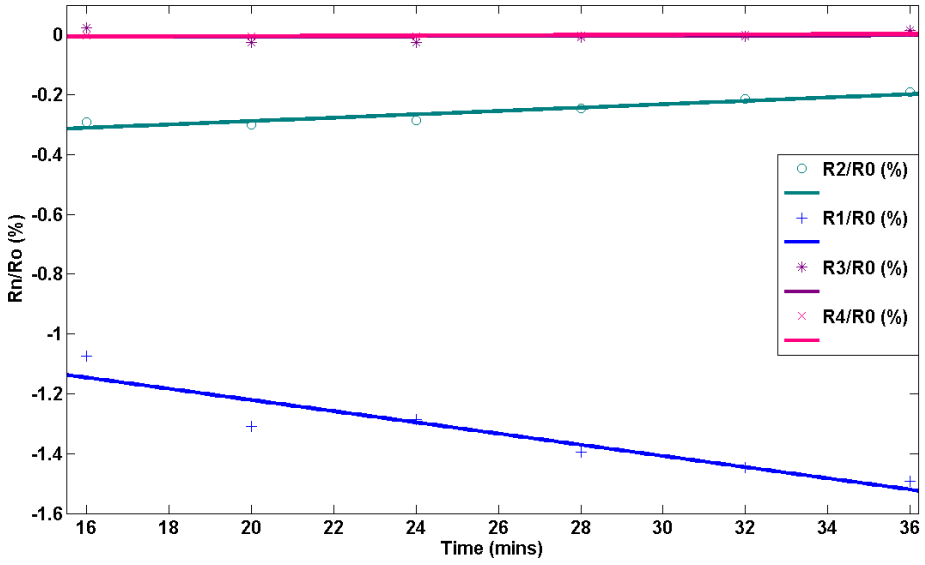


Figure 89: Variation of the anisotropy harmonics with the ICP etching time for initial opening 20 µm.

The effect of the initial opening size on the anisotropy harmonics was then investigated. Figure 90 shows the first four harmonics as a function of initial opening. The etch time selected in each case was 36 minutes. The first harmonic is seen to decrease with initial opening size while the others remain close to constant. This suggests that a bigger initial opening is desirable for creating highly uniform hemispheres.

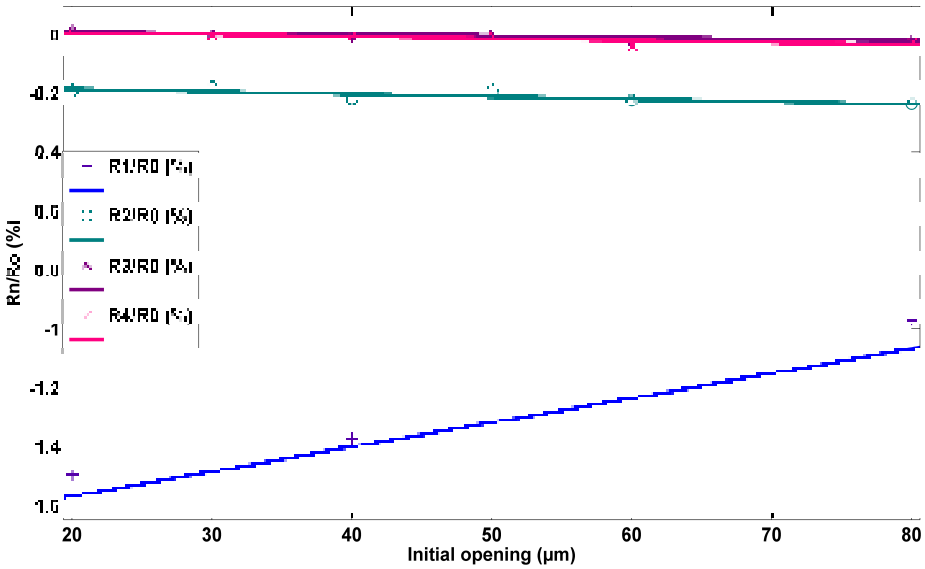


Figure 90:. Variation of the anisotropy harmonics with the initial opening size for wafers ICP etched for 36 minutes.

The etch rate as a function of angle for the circular opening was then calculated. This was done using the following equation:

$$Etchrate(\theta) = \frac{S_F(\theta) - S_I(\theta)}{t_F} \qquad (38)$$

where S_F is the final shape, S_I is the initial shape and t_F is the time etched to reach S_F. Plotting this etch rate against theta demonstrates the evolution towards a steady state etch rate as shown in Figure 91.

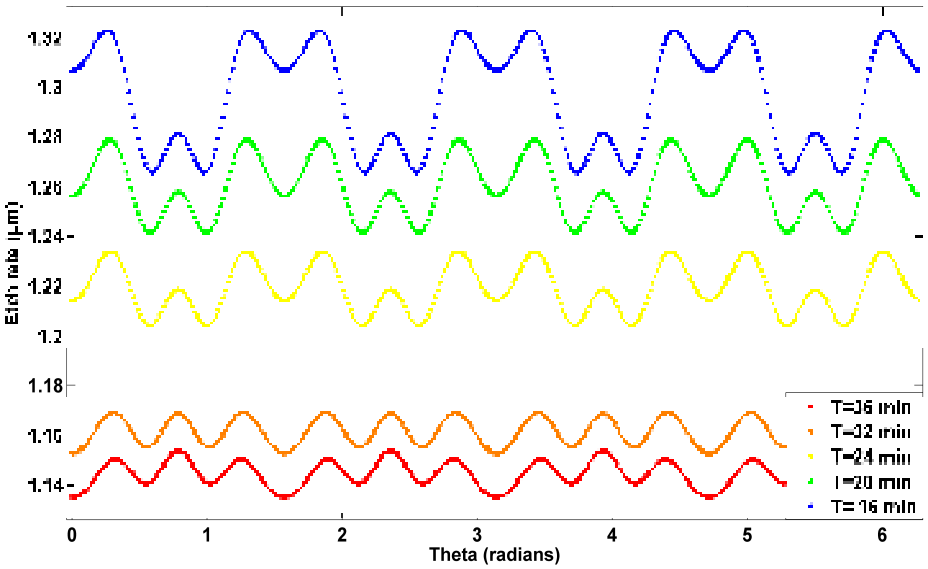


Figure 91: Graph showing the etch rate as a function of theta for the 20µm initial opening cavities as it evolves over time.

The gap in the sequence at T = 28 minutes is present due to this wafer being highly anomalous. This arises from the wafer having a slightly longer wet etch than all the other wafers. Figure 91 shows that the etch has still not reached its steady state as the rate is still decreasing and the angle dependent shape has not quite stabilised. This data is also backed up by the graph shown in Figure 89. Here the data showed that while the first harmonic was growing with time the second harmonic was decreasing. This fits with the observation that the etch shape is becoming closer to a sinusoidal function with increasing etch time.

5.3.1.2. 2D Profiles

The 2D profile of the hemispheres was investigated using a KLA tencor P-16+ stylus profiler. The lateral resolution in the plane of the wafer was 1 µm. The centre slice of this profile was taken for each etch time and is shown in Figure 92. The lower time etches are not shown as the sidewall angle was too steep for the stylus to give useful data.

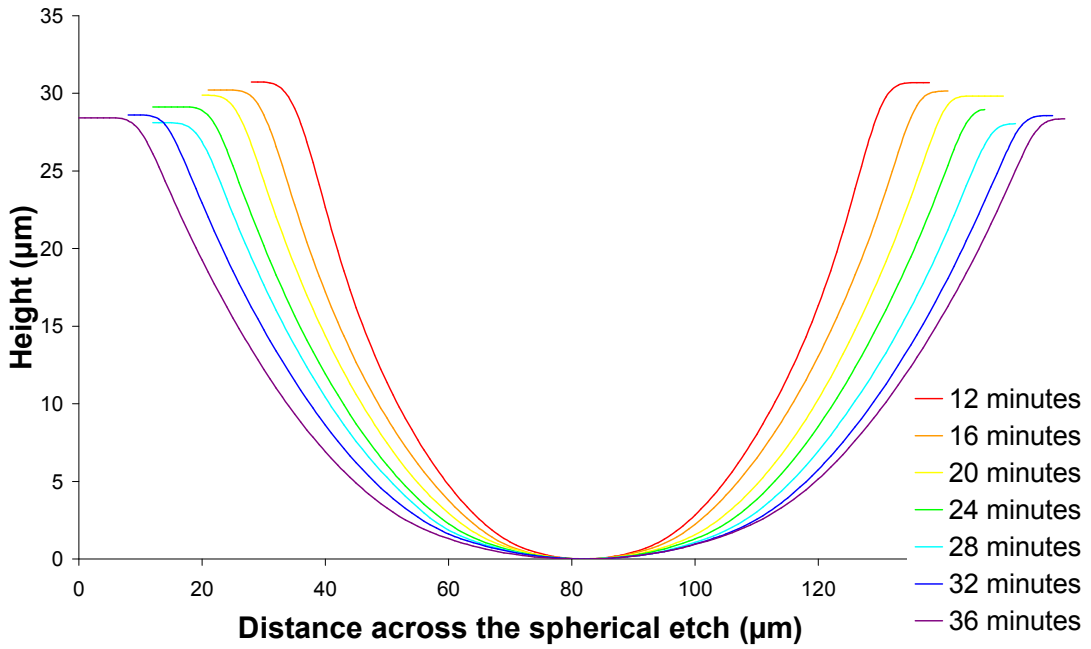


Figure 92: Graph showing a 2D slice into the plane of the wafer through the center of the hemispherical cavities.

This data shows the main effects of the ICP etch. Firstly, it is clear the radius of each cavity is gradually increasing with etch time. It is also obvious that the cavities become shallower with time. This is due to the blanket etch acting over the whole wafer so thinning the wafer itself. While the flats etch unhindered, the hemisphere surfaces present a set of all crystal planes present between the normal and the plane of the wafer and so etch slightly slower resulting in this shallowing effect.

Looking at a 2D slice of the hemispherical cavities again it is clear that the etch is not isotropic and therefore the cavity is not truly hemispherical. The variation is shown clearly when compared to the best fit circle which was achieved by first calculating the best fit circle to a 2D slice through the hemisphere using the equation of a circle:

$$z = z_0 - \sqrt{R^2 - (x - x_0)^2} \qquad (39)$$

where z and x are the coordinates of each data point, z_o and x_o are the coordinates of the origin of the circle and R is the radius. Using Matlab code (see appendix 2), the variables x, z and R were given rough bounds and the corresponding circle for each set of variable was calculated. The difference between these circles and the real data

was then calculated by squaring the difference between each set of data points and summing over the whole data range. The values were then compared to find the lowest number and therefore the best fitting circle.

The values were then applied to a slice from a micro-cavity with an initial opening 20 µm and an ICP etching time of 36 minutes. The results showed that the best fit circle to the data was of radius 109 µm centered at z = 74.3, x = 82.3. Using this calculated centre point, equation 37 could be used to reveal the anisotropy. The best fit was achieved when n = 3 was used as shown in Figure 93.

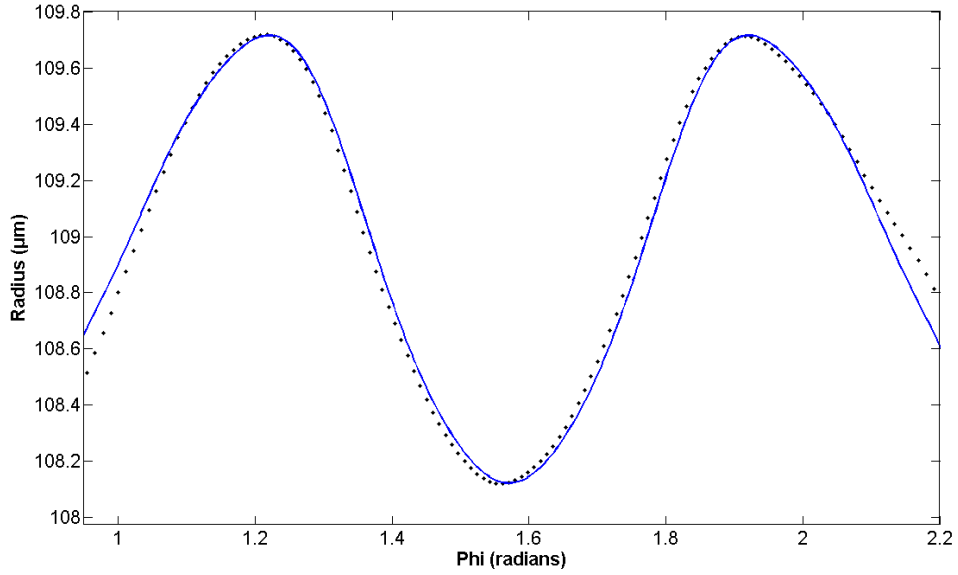


Figure 93: Graph showing a 2D slice through the centre of a hemispherical cavity along $\theta=0^{o}$ (initial opening 20 µm and ICP etching time 36 minutes). The data has been fitted to equation 37.

As the hemispherical opening was not a perfect circle due to the anisotropy in the etching process, it is not expected that the 3D line scans will be constant with respect to the angle theta they are taken. To demonstrate this, a line scan from θ = 45 degrees is presented in Figure 94. The same procedure was used to calculate the centre point of the best fit circle and equation 37 was then used to obtain the plot.

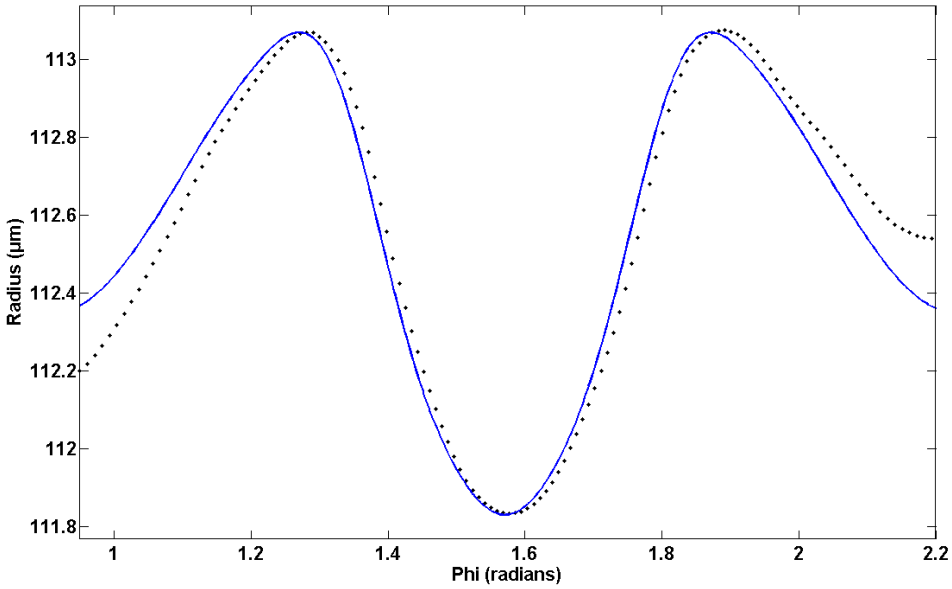


Figure 94: Graph showing a 2D slice through the centre of a hemispherical cavity along θ=45° (initial opening 20 µm and ICP etching time 36 minutes). The data has been fitted to equation 37.

This graph shows that the overall isotropy has a similar dependence on phi; however, it is not exactly the same. The R_n values from both fits are shown in Table 7 for comparison.

Theta (degrees)	0	45
R_0	108.9	112.5
R_1	-0.002338	-0.06281
R_2	-0.8646	-0.004145
R_3	-0.01621	-0.2441
R_4	-0.05588	-0.005035
R_5	0.08842	0.01208
R_6	-0.03034	0.03496
R_7	0.02551	0.009106
R_8	0.02644	-0.002676
R_9	0.006532	-0.006286

Table 7: Table showing the R_n constants used to fit the data to equation 37 for two different 2d slices through the hemisphere.

This result is not unexpected as it has already been shown that the shape of the 2D opening is dependent on the crystal orientations and so a similar effect would occur within the 3D shape. This results in a slightly different shape being formed at every value of theta due to the different crystal planes being present.

5.3.1.3. 3D shape

Finally the 3D shape of the whole hemisphere was investigated. In order to characterise this, a KLA tencor P-16+ stylus profiler was again used. In order to characterise the hemispheres the axis and angles were defined as shown in Figure 95.

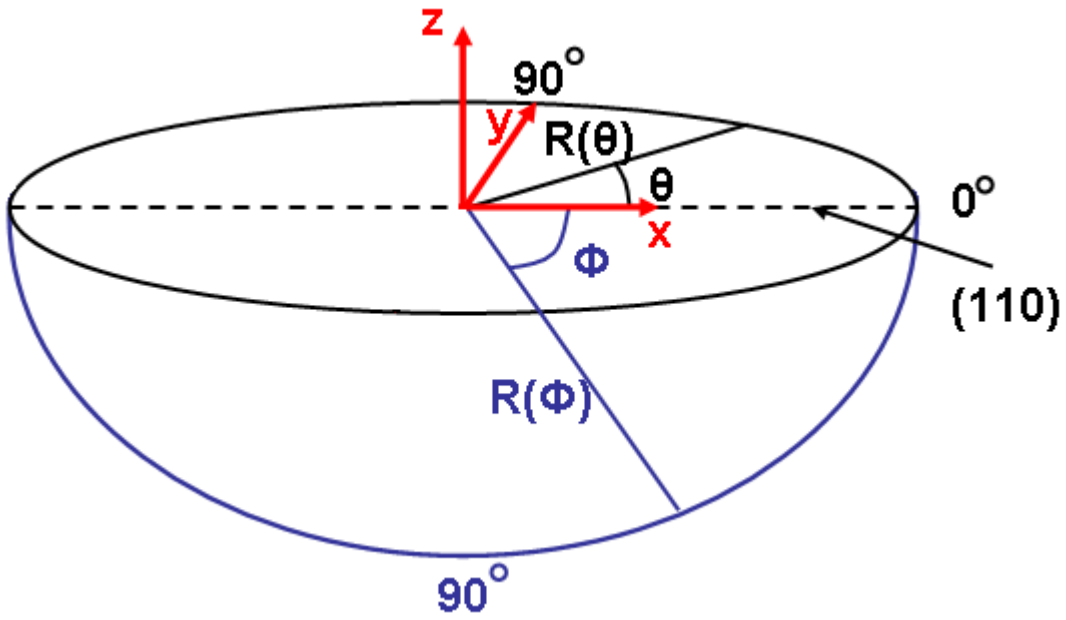


Figure 95: Representation of how the data was recorded and labelled. The zero angle was common to both theta and phi with theta varying from 0-360 degrees while phi varies between 0-180 degrees. The centre of the bowl was chosen as the origin.

A best fit sphere to the whole cavity was found. This was done in the same manner as the best fit 2D slice using Matlab but with an extra variable added. Figure 96 shows the etch shape as measured by the stylus profiler.

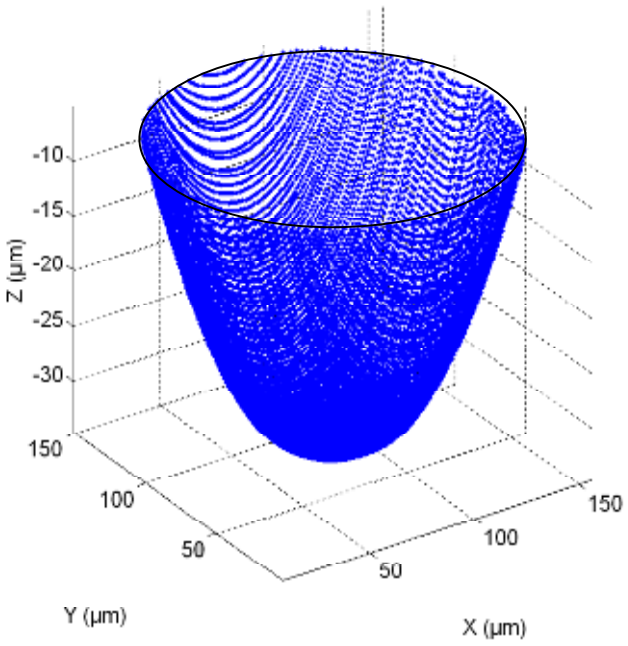


Figure 96: 3D plot of the stylus profiler data for a hemisphere produced from an initial opening of 20 µm and an ICP etching time of 36 minutes.

This data was then taken and the best fit sphere calculated. This was done in Matlab using the equation:

$$z = z_o - \sqrt{R^2 - (x - x_0)^2 - (y - y_o)^2} \qquad (40)$$

where z, y and x are the coordinates of each data point, z_o, y_o and x_o are the coordinates of the origin of the circle and R is the radius. The variables x_o, y_o, z_o and R were given rough bounds and the corresponding hemisphere for each set of variable was calculated. Figure 97 shows the best fit sphere to the data recorded from the micro-cavity.

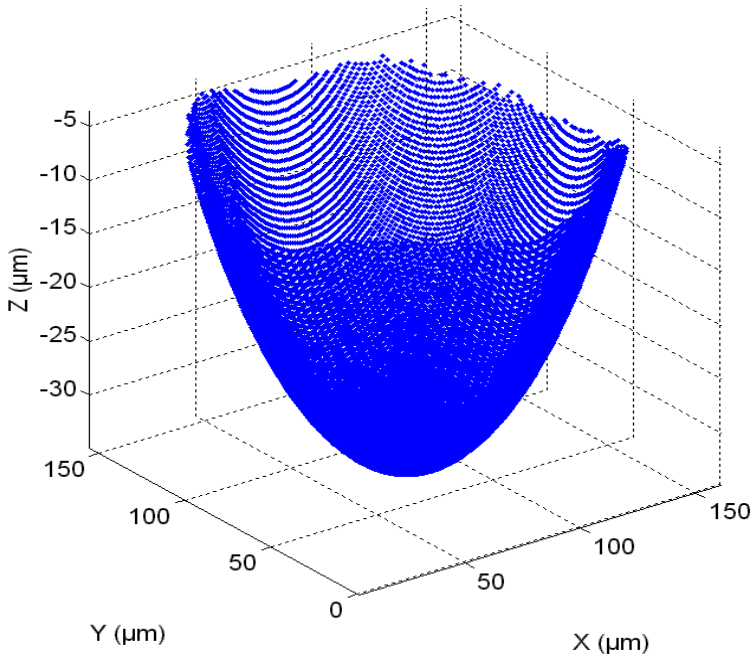


Figure 97: 3D plot of best fit hemisphere to the micro-cavity.

The difference between these hemispheres and the measured data was then calculated. This is done by squaring the difference between each set of data points and summing over the whole data range. This value was then compared in each case to find the lowest value and therefore the best fitting circle. Figure 98 shows the residual left after the subtraction of the two sets of data. An R squared test on the fitting gives a result of 99.45 %.

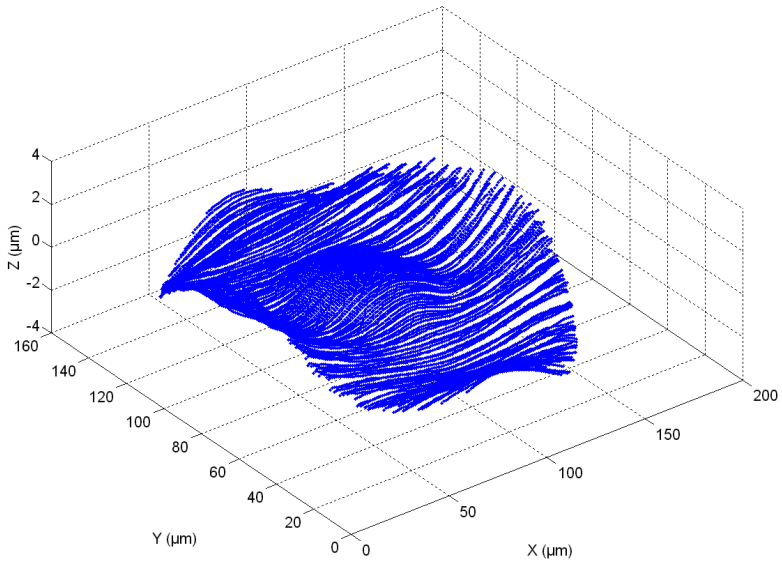


Figure 98: 3D plot of the difference between the real data and the best fit hemisphere.

The data was analysed for a variety of different micro-cavities but the results did not yield any more insights than the 2D slices discussed in the previous section. The data did however confirm the 4 fold symmetry expected from the crystal structure. This can be seen in Figure 98 where the residual pattern has 4 fold rotational symmetry.

5.3.2. Surface Roughness

Having studied the shape evolution, the roughness was then investigated. The roughness is a critical factor in the quality of the micro-cavity. While long scale aberrations of the surface shape will distort the cavity mode, it will not lead to loss of photons. It is the short scale roughness that will lead to scattering of the light leading to a reduction in the reflectivity [122, 137]. The data discussed in the following was obtained by the project collaborators at Imperial College London.

First, a Zygo optical profilometer was used to characterise the surfaces. This tool had a vertical accuracy of 1 nm, allowing much higher resolution than the stylus profiler. The lateral resolution was limited by the wavelength of the light as well as the resolution of the camera. Using this profiler, light could only be collected from a limited region at the bottom of the cavities. The data presented below is for a circular area of 11.6 μm diameter. Figure 99 shows the aberration of the profile from a perfect sphere as a function of etch time. It is clear that the aberration improves with increasing etch time.

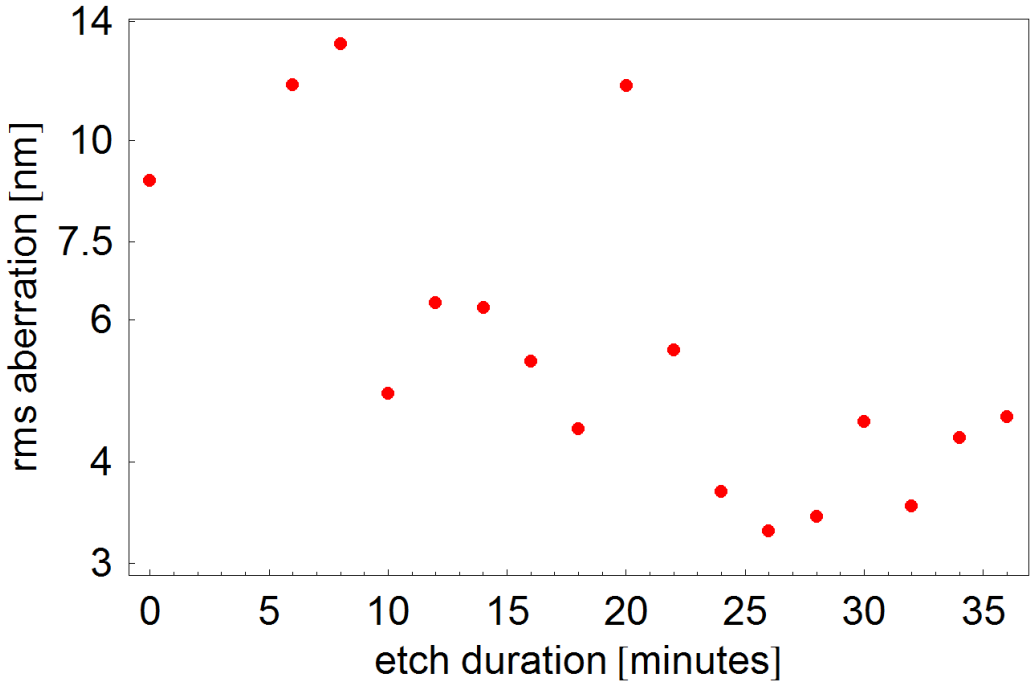


Figure 99: Aberration of the surface from a perfect sphere, versus etch duration.

This improvement is corroborated by the behaviour of the surface for shorter length scales. Figure 100 shows the RMS roughness for a length scale of 1.2 μm. This length scale is of particular interest as it determines the reflectivity of the micro-cavities for a wavelength on the order of 780 nm. It can be clearly seen that an increase in the etch time results in a smoother surface in the micro-cavities.

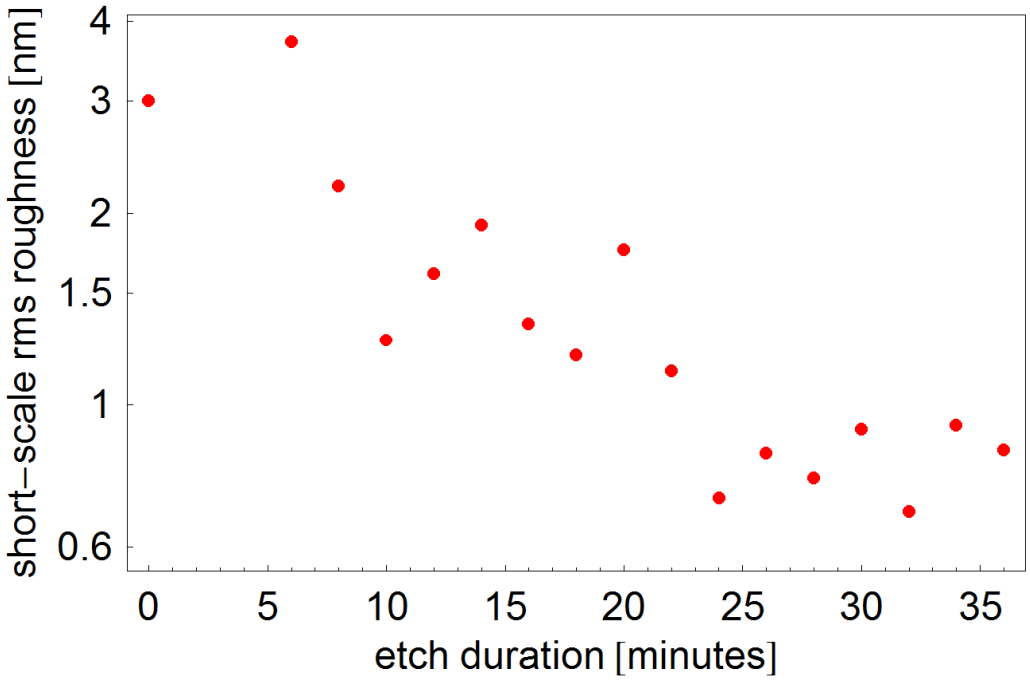


Figure 100: Short-scale (1.2μm) rms roughness of the surface from a perfect sphere, versus etch duration.

Next, AFM measurements of the micro-cavities were performed. It proved difficult to reach the cavities with the AFM cantilever due to the depth of the micro-cavities. Therefore, reliable measurements could only be taken from the shallower micro-cavities that had been etched for 14 minutes or more. In order to scan a wafer that had undergone no ICP treatment, a wafer was cleaved through the centre of a micro-cavity. This allowed easy access to the bottom of the micro-cavity via the cleaved edge. AFM scans were also taken on the flat part of the silicon wafer. This was performed to monitor the evolution of a perfectly smooth surface under ICP etching.

A virgin wafer is supplied with a Chemically Mechanically Polished (CMP) surface. This means the initial surface is extremely smooth. Measurements confirmed this showing an initial roughness of ~0.15 nm. Figure 101 shows the evolution of the flat wafer surface as a function of etching time. A tilt and a bow have been removed in order to compensate for a drift of the cantilever. As expected the ICP process initially increases the surface roughness of the surface. This increase mainly manifests itself as boulders. The boulder size and number increases until 10-14 minutes of ICP etching. It then gradually decreases leading to a smooth surface of less than 1 nm RMS roughness.

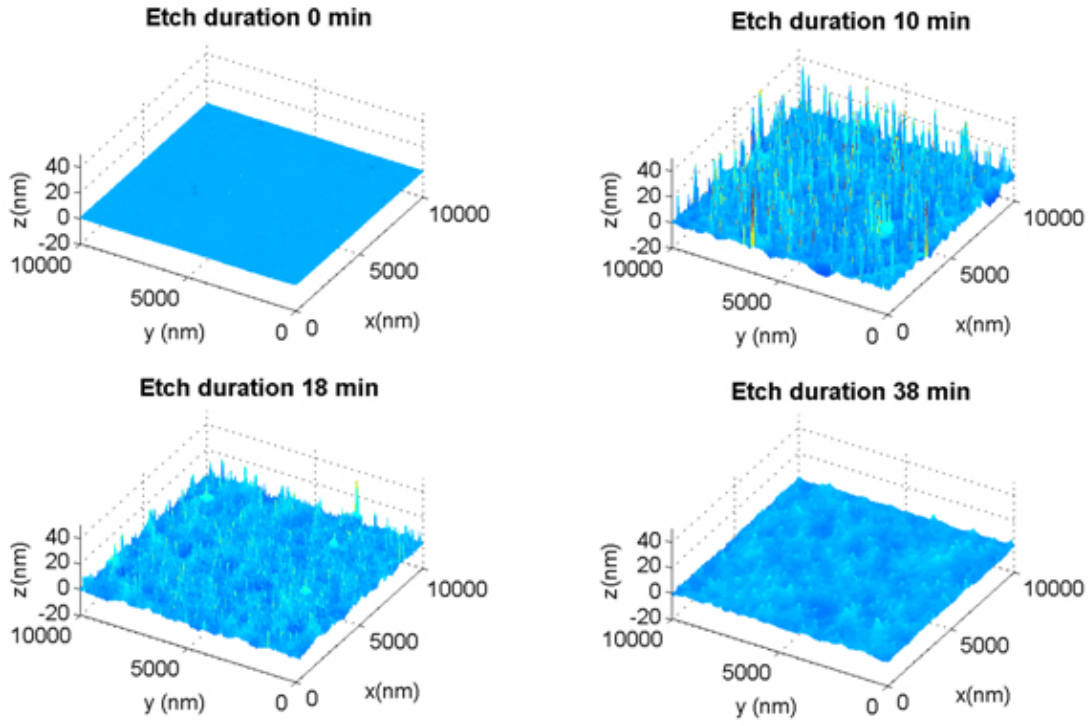


Figure 101: AFM scans depicting the evolution of the flat portion of the wafer as a function of ICP etch time.

The cavity profiles are initially significantly rougher, with approximately 5 nm RMS roughness. This gradually decreases to a smoother profile over time. The evolution of the cavity profiles as a function of etching time is shown in Figure 102.

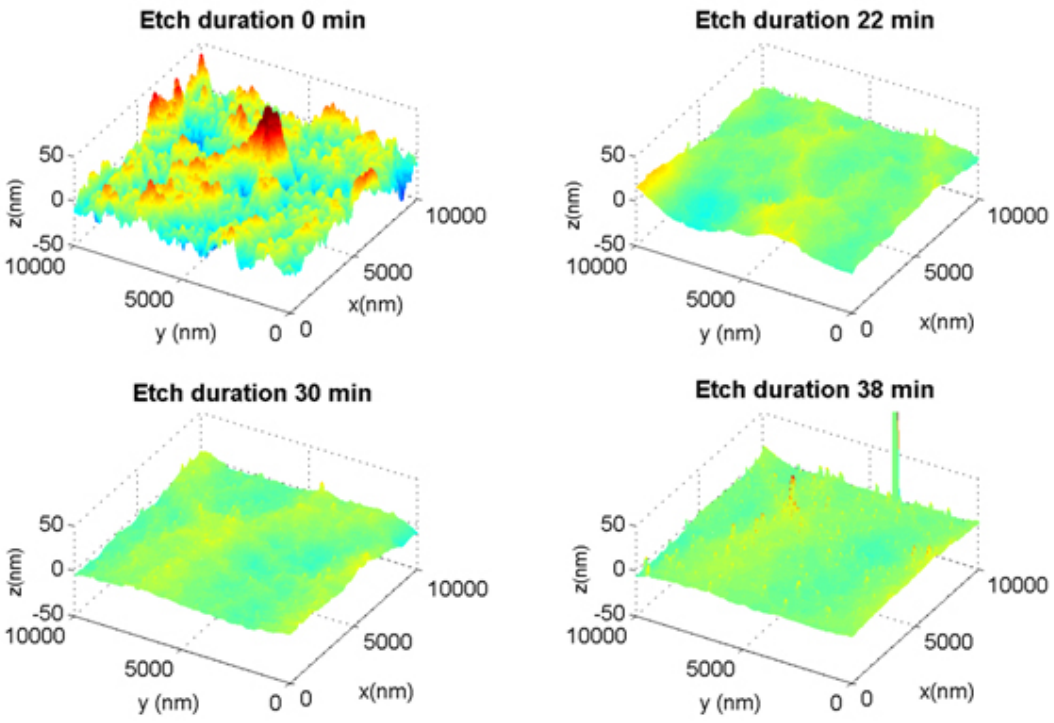


Figure 102: AFM scans depicting the evolution of the concave micro cavity surface as a function of ICP etch time.

The RMS surface roughness of the silicon surface measured by the AFM is plotted in Figure 103 as a function of ICP etching time. Both the concave micro-cavity surface (blue) and the flat wafer surface (black) are shown. The measurements for the concave surface confirms the smoothing effect of the ICP etch shown by the interferometer measurements.

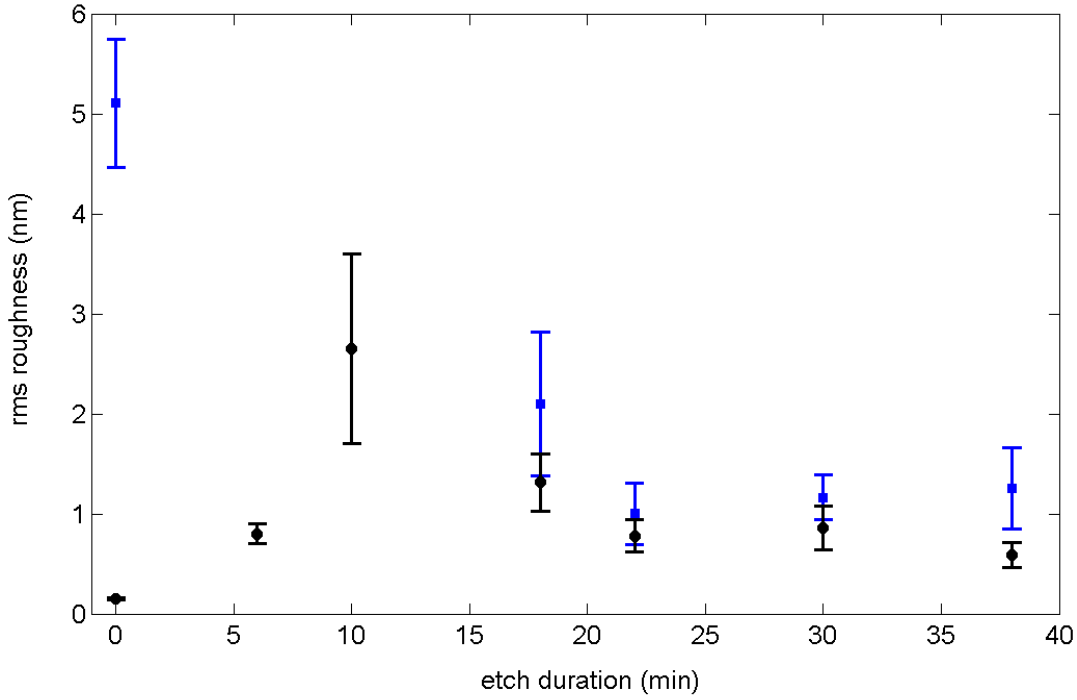


Figure 103: Graph showing the evolution of the RMS roughness of the concave micro-cavity surface (blue) and flat wafer surface (black) with respect to ICP etching time.

5.3.3. Optical properties

The determining factor in the performance of the micro-cavities will be the finesse. This depends on the losses due to the scattering properties of the surface. The long-scale aberration of the surface from a sphere will distort the mode, but will not lead to losses due to incoherently scattered light. Short-scale roughness however will lead to scattering, leading to a reduction in the reflectivity of the mirror. The boulders, which are a highly visible feature of the AFM scans, will have a negligible effect on the reflectivity. In work performed by the project collaborators at Imperial College London the effect of these boulders was estimated. They assumed that the boulders will radiate as spherical, perfectly conducting dipoles. Their combined surface area occupies less than 0.2 % of the total surface in all scans. Their radius is on the order of 20 nm, leading to an effective scattering cross-section of less than 3 nm. The loss was then calculated using the Debye – Waller formula [138]. The total scattering loss

due to these features will therefore be of less than 10 ppm in the worst-case scenario. For the longer etch times, this figure is reduced by over two orders of magnitude, and is therefore negligible compared to the losses due to the overall roughness, which exceed 100 ppm.

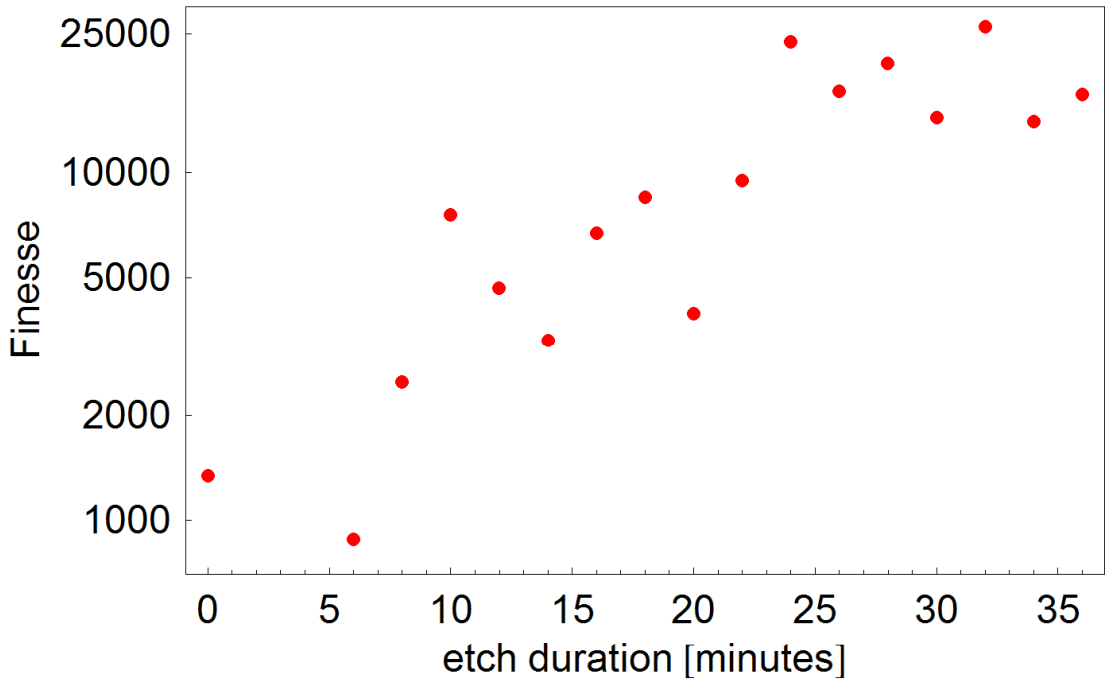


Figure 104: Maximum possible finesse, inferred from the short-scale roughness measurement assuming a perfectly reflecting mirror.

The finesse, F, of the micro-cavities is calculated by:

$$F = \frac{\pi}{(1-R)} \tag{41}$$

where R is the reflectance. The finesse is plotted against etch duration as shown in Figure 104. For this result it is assumed the etched surface is coated with a perfectly reflecting layer. It is also assumed that the second mirror of the cavity has the same reflectivity, so as to be perfectly impedance-matched. This shows that the ICP etching procedure results in an improvement from a finesse of ~1000 to maximum values exceeding 25000.

5.3.4. Atom experiments

The project collaborators at Imperial College London have created a Fabry-Perot optical resonator from the silicon micro-cavities. Using the setup shown in Figure 105 it has been proven that this resonator can be used for single atom detection and photon production [129].

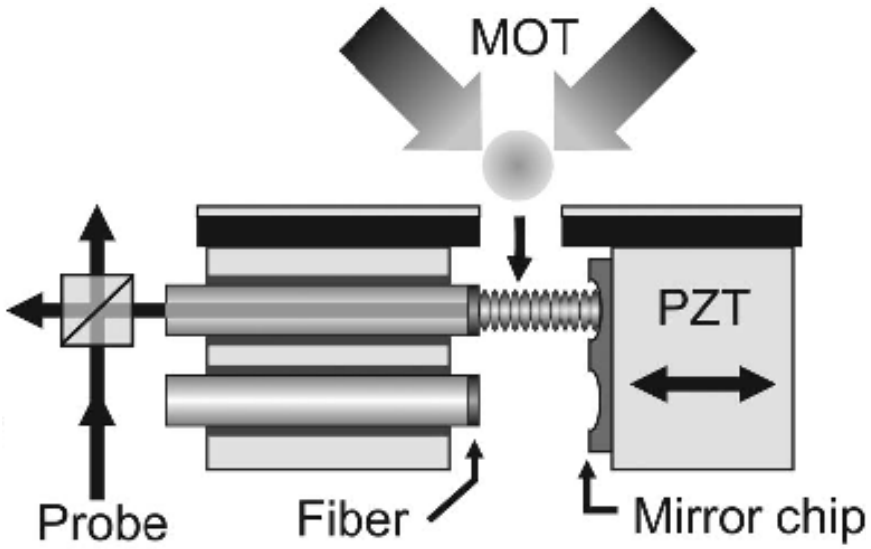


Figure 105: Picture showing the setup used to create an optical resonator from the silicon micro cavities.

The atoms are initially trapped by the MOT and then dropped into the optical cavity under the force of gravity. The laser light is guided into the cavity using an optical fibre. The presence of the atoms can be seen through changes in both the intensity and the noise characteristics of probe light reflected from the cavity input mirror. This experiment is repeated multiple times with identical drops before the results are averaged. Using this data it has therefore been shown that single atom detection is possible.

Using the same cavities it has also been shown that they can be used to produce single photons on demand. Once again atoms are trapped in a MOT and then dropped through the optical cavity. When the atoms are in the centre of the cavity an excitation laser passing transversely through the cavity is fired. This triggers photon emission into the cavity. Figure 106 shows a typical result from this experiment.

First the reflectance is shown. The rise represents the presence of atoms in the cavity. At its peak the excitation laser is turned on, this is represented by the dotted line. This causes the atoms to be kicked out of the cavity as shown by the sharp drop in signal. At the same time a spike in the fluorescence can clearly be seen. This represents the photons produced by the interaction between the atom, cavity and excitation laser.

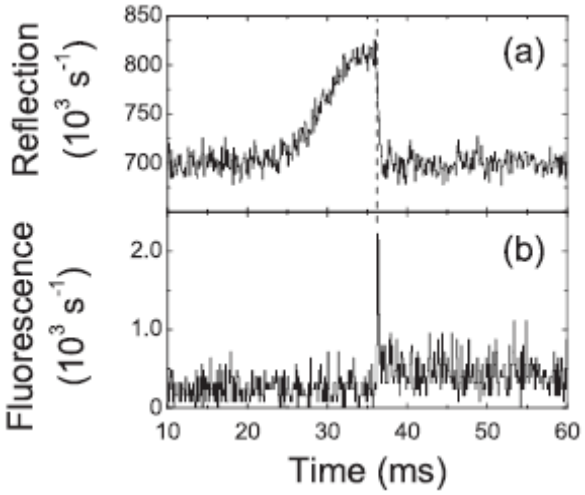


Figure 106: Graph showing the ability to produce photons on demand using the micro-cavity. a) shows the reflectance signal (photon count rate) as a cloud of atoms is dropped into the cavity, b) shows the fluorescence recorded from the cavity.

5.4. Conclusion

It has been shown that the silicon micro-cavities, fabricated using the methods presented here, are suitable for atom optics experiments. It has also been shown that it is possible to fabricate these cavities to any desired size by manipulating the initial conditions and the etch parameters. A method has been presented of integrating these mirrors into atom chips. This shows the versatility of this fabrication technique as not only an atom chip tool but also to other OMEMs devices.

The evolution of the shape and surface roughness produced by the fabrication method was investigated. The process was analyzed using a stylus profilometer, an optical interferometer and an AFM. The results showed that all the etches involved have a small anisotropic element that causes the micro-cavities to have aberrations from a

perfect hemisphere. This effect is attributed to the crystal planes present in the silicon wafer giving subtle differences in the etching process. It was however shown that ICP etching can significantly improve the roughness of wet etched surfaces. The spectral properties of the etched surfaces show that the smoothing is most effective at intermediate roughness wavelengths on the order of 100 to 1000 nm.

It has also been shown that the silicon micro-cavities can be used to form an optical resonator which has the capability of both single atom detection and producing single photons on demand. These are first steps toward building an optical micro-cavity network on an atom chip for applications in quantum information processing. To achieve this requires further improvements in the control of the atomic motion. With this in mind the next step is to trap and cool atoms directly inside the cavities.

Chapter 6

Sputtered Si/Ti Films

In this chapter a new fabrication technique is developed. This technique has a very wide scope for applications as it could be used for the integration of any MEMS/ integrated circuits (IC) device including atom chips. The technique is based on the co-sputtering of amorphous silicon/titanium composites at room temperature.

6.1. Introduction

There is an increasing demand to integrate MEMS and ICs on the same silicon wafers aiming at cost-effective devices with better performance, stability and simple packaging. However the integration of MEMS devices with ICs is often very difficult due to incompatibilities in the fabrication.

The simplest method of integration is to build the MEMS device directly on top of a CMOS wafer. This method however has the severe disadvantage of requiring strict process compatibility, the most critical of which is the low thermal tolerance of CMOS wafers. This can rule out the use of many MEMS structural materials such as polycrystalline silicon (poly-Si) which requires a high temperature deposition process (>600 ^{o}C) [139]. Recently, amorphous silicon (a-Si) has been developed as a promising alternative because it can be deposited at low temperatures (< 250 ^{o}C) [140, 141].

While passive MEMS structures may not need to be conductive; electrostatic and electrothermal devices require certain levels of conductivity to enhance their functionality. Amorphous silicon is usually dielectric and difficult to dope effectively. Metal layers can be employed as conductive claddings [142] but this can complicate the fabrication process and introduce stress, potentially causing deterioration of the device performance. It has been shown that the gradual increase

of electrical conduction over a range of several magnitudes in dielectric materials is possible by incorporating metal nanoparticles, including gold [143], cobalt [144] and chromium [145], into the insulating matrix.

In this work the effect of using titanium as the co-sputtered metal to create a novel MEMS structural material was studied. Titanium was chosen because it is a conductive metal that has properties close to that of poly-Si as shown in table 4. It can also be DRIE'ed allowing the film to be fabricated into devices easily. In this chapter, the suitability of co-sputtered silicon-titanium thin films as a MEMS material is investigated.

Material	Density ($g\ cm^{-3}$)	Young's modulus (GPa)	Poisson's ratio	Thermal expansion coefficient ($10^{-6}\ K^{-1}$)	Thermal conductivity ($Wm^{-1}K^{-1}$)
Poly-Si [146]	2.33	151±6	0.25	2.3	15
a-Si:H [147, 148]	2.30	134±5	0.22	4.4	5
Ti [149]	4.51	116	0.32	8.6	21.9

Table 8: Comparison of mechanical properties of poly silicon, a-Si:H and titanium.

6.2. Fabrication

The aim of this work was to fabricate silicon - titanium films of varying percentage content to allow the properties of the films to be characterised as a function of the composition.

Each sample was created on <100> p-type silicon wafers with a 1000 nm of thermal oxide grown on the front side. The wafers were pre-diced into 10 mm squares. The silicon squares were placed in a custom made sample holder that allowed six pieces of silicon to be placed in the sputterer at once, as shown in Figure 107. The holder was designed to mask off all the edges of the samples creating a 1 mm wide border. This

prevented the composite being sputtered on the sides of the substrate stopping the deposited film from coming into contact with the bare silicon substrate and therefore shorting the oxide layer. It also provided a step to measure the deposited film thickness.

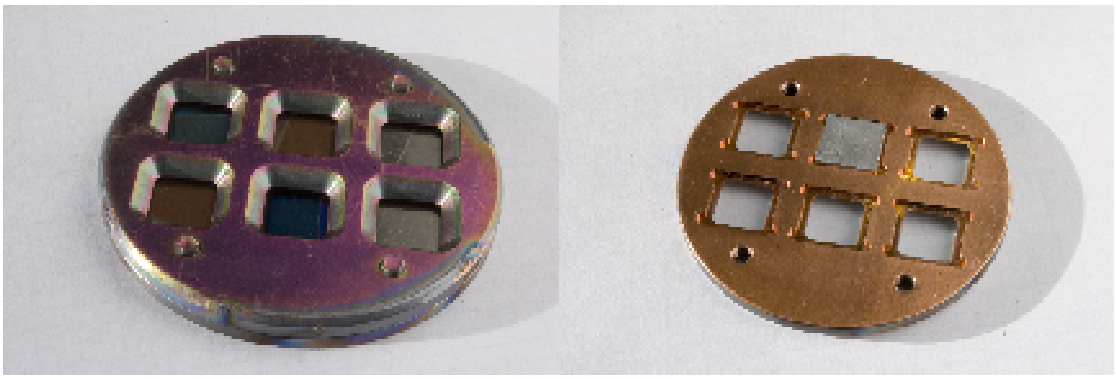


Figure 107: Photograph of the sample holder used to sputter up to six samples. Left: Front view of the complete holder. Right: Back view of the front plate, the six slots used to hold the samples in place can clearly be seen. The top middle slot is shown holding a typical sample.

Initial results were obtained by placing six silicon samples into the holder for each deposition. However it soon became apparent that the silicon substrate interfered with the Energy Dispersive X-Ray (EDX) experiments required to calculate the elemental composition of each sample. To negate this problem for each subsequent deposition five silicon substrates and one aluminium substrate were placed into the sample holder. This aluminium substrate acted as a probe sample which could be used in EDX experiments to measure the silicon content without contamination from the substrate itself.

Before samples were created a calibration run was done to find out the effect of varying the power and gas flow on the deposition rate of both materials and to calibrate the thickness monitor. It was found that both parameters have a linear relation to the sputtering rate over the ranges that would be required. Figure 108 and Figure 109 show a typical set of results.

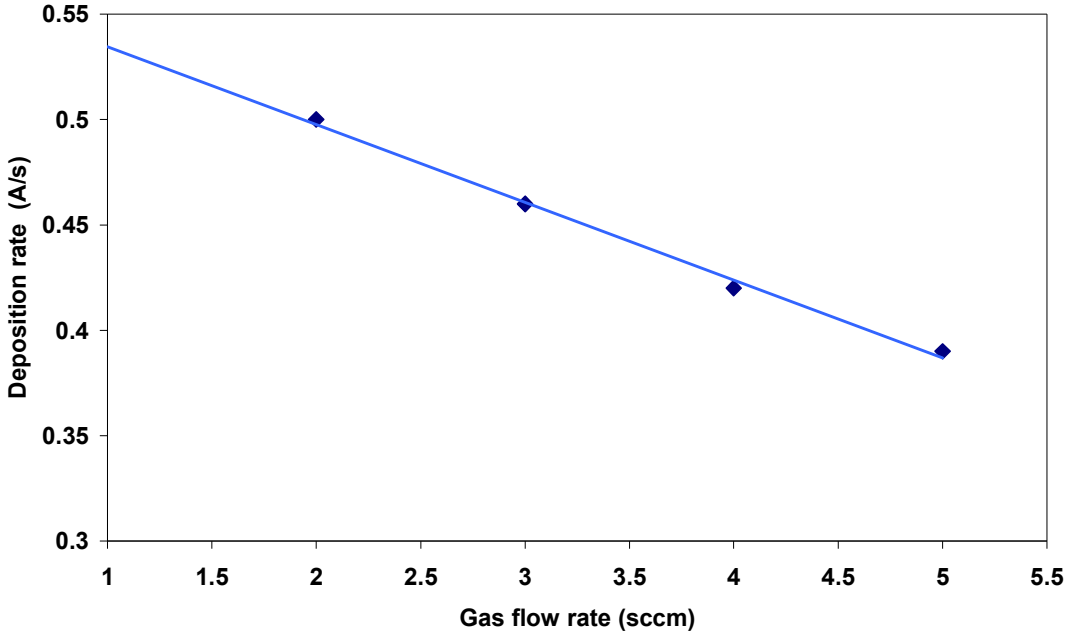


Figure 108: The effect of gas flow rate on the deposition rate of silicon.

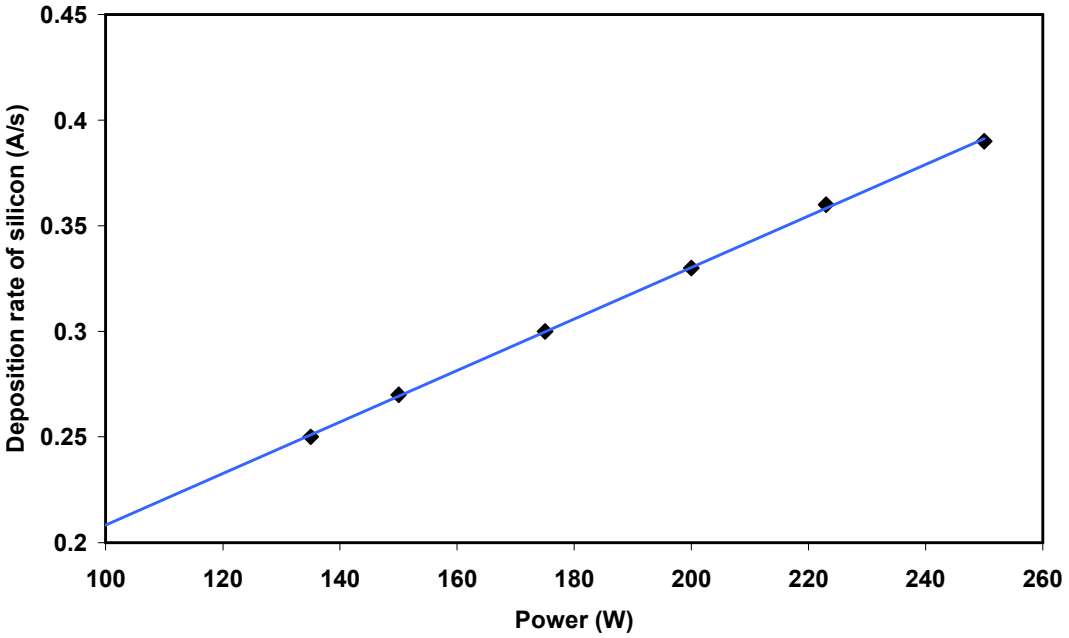


Figure 109: The effect of the power on the deposition rate of silicon.

Having checked and calibrated the system, films of varying titanium content were sputtered. The co-sputtering was performed using high purity Si (99.999 %) and Ti (99.95 %) targets on PFG 1500 DC 1.5 kW and PFG 600 RF 0.3 kW power supplies, respectively, in a Kurt J. Lester sputterer. By adjusting the power of the Ti target while keeping the power of the Si target constant, the percentage of Ti in the

deposited films was controlled. Argon was used as the sputtering gas and the chamber pressure was kept at 8 x 10^{-3} mbar. The samples were rotated during the sputtering to ensure an even coverage was obtained.

6.3. Results

Having created the samples, the film thickness was determined using a KLA Tencor P16 stylus profiler to measure the step height between the bare oxide and the sputtered layer. The sheet resistance R_s was then calculated using the following equation:

$$R_S = \rho \times \frac{V}{I} \tag{42}$$

where ρ is the geometric factor for sample being measured, V is the voltage and I is the current. The values were obtained using a 4-point probe station and an Agilent 4155C semiconductor parameter analyzer. In this case ρ is equal to 4.5324 as the sample is a thin film with a size that is more than 40 times larger than the spacing between the probes [150].

Using these two values of film thickness (T) and sheet resistance (R_S) the resistivity (R) of the film can be calculated.

$$R = T \times R_S \tag{43}$$

The titanium content by percentage of atomic weight in each sample was determined by the EDX analysis. The accelerating energy was set to 15 keV to ensure all the peaks were sufficiently excited with a large enough photon count and the scan time was set to 2 minutes. Ideally a voltage would be selected that was low enough not to penetrate the sample film and into the substrate. However, the samples created were too thin to allow the voltage to be set low enough to not penetrate the film while still exciting the titanium lines present at 4.509 keV. Therefore a higher voltage was chosen to allow a strong signal to be achieved from all the lines present.

Focusing on a 2 μm square the spectrum was recorded and analysed using INCA software from Oxford Instruments. First a scan was made of a bare aluminium sample, this acted as a base line from which the other scans could be compared. The spectrum created is shown in Figure 110. All the samples were then scanned using the same settings to obtain their spectra. A typical example is shown in Figure 111. Having created the spectra, the base scan of bare aluminium was subtracted from each sample to remove results attributable to the aluminium substrate as shown in Figure 112. Over time the samples also began to oxidise so all results were processed to remove their oxygen content.

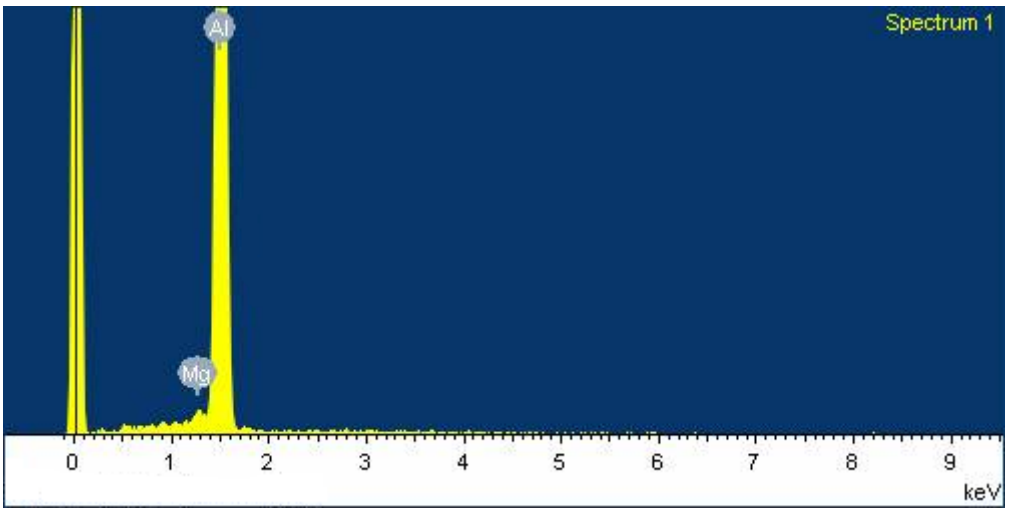


Figure 110: EDX spectrum of the aluminium substrate.

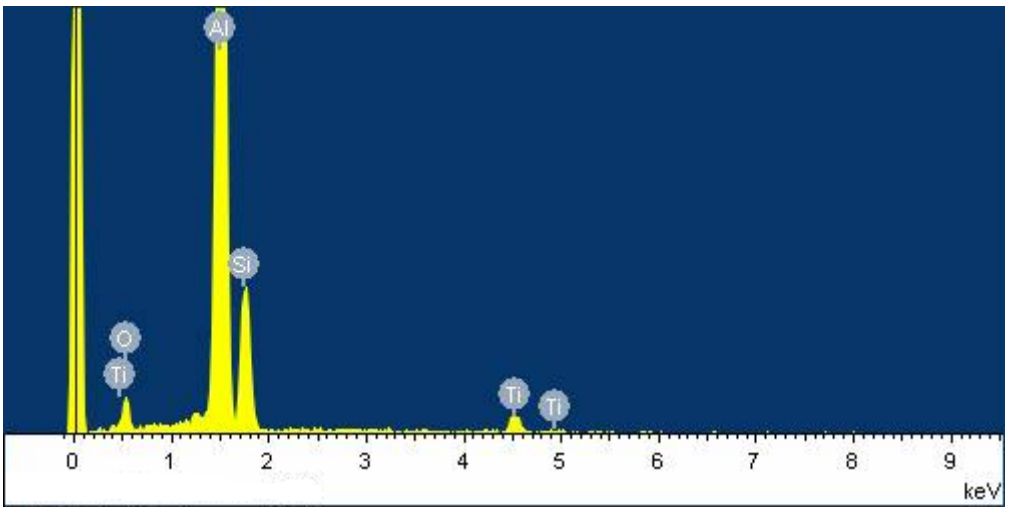


Figure 111: Typical EDX spectra obtained from the silicon titanium samples.

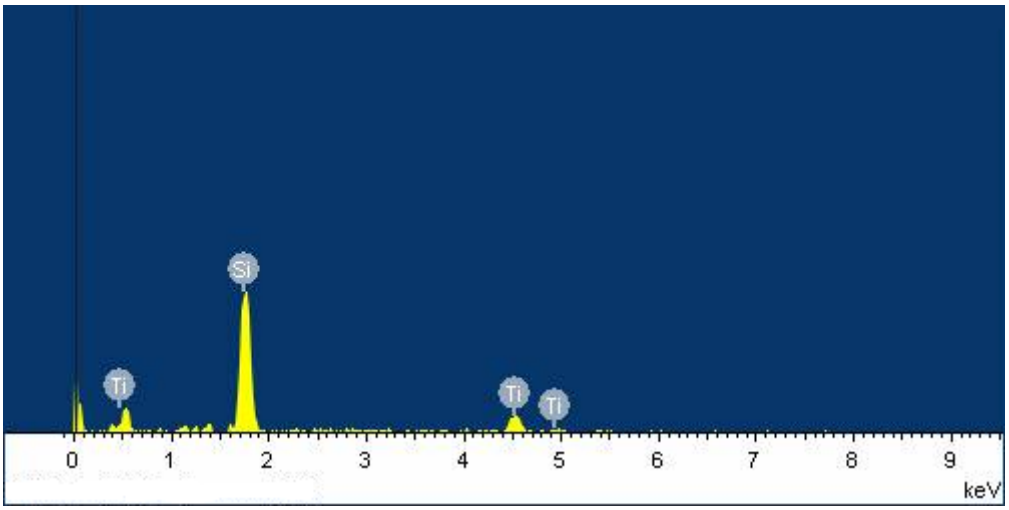


Figure 112: Typical EDX spectra obtained from the silicon titanium samples after the substrate has been subtracted from the results.

A selection of co-sputtered samples, corresponding to different titanium contents, were then annealed under normal atmosphere at T = 200 ^{o}C, 300 ^{o}C, 400 ^{o}C and 500 ^{o}C for 2 hours. This was done to investigate the stability of the electrical properties and nanostructures of the films. Figure 113 displays an AFM image of a co-sputtered silicon-titanium thin film annealed at different temperatures. The typical RMS roughness of the samples was around 0.6 – 1.5 nm for films with thickness of 290-390 nm. It is anticipated that the surface roughness could be further improved by lowering the sputtering pressure to meet the requirement of < 0.5nm RMS roughness required for the wafer bonding process [151]. The grainy structure of the film is clearly shown, corresponding to a grain size of around 20 nm. After annealing the grain size has increased; at 300 ^{o}C this grain size has reached 30 nm, while at 500 ^{o}C further increase to 40 nm is seen. However compared to pure silicon samples the annealing process did not cause an obvious increase in surface roughness.

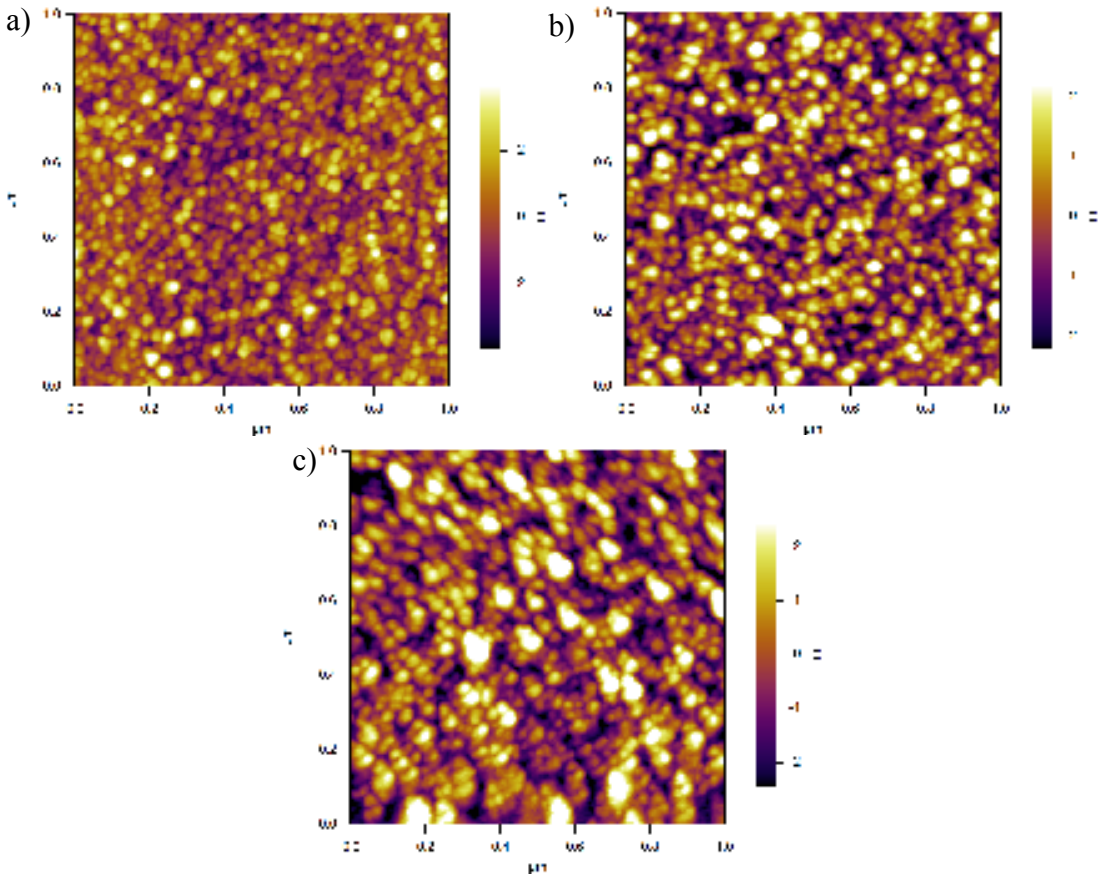


Figure 113: A 1 µm by 1 µm AFM image of co-sputtered silicon-titanium thin film a) un-annealed b) annealed at 300°C and c) annealed at 500 °C.

In Figure 114 the resistivity of the thin film as a function of the titanium content in percentage weight is shown for the four different annealing temperatures alongside the resistivity of the non-annealed film. Work done by Z. Moktadir found that the dependence of the resistivity on titanium content in the films was in good agreement with percolation theory [152] as the resistivity ρ scales as:

$$\rho = a(T)(x - x_c(T))^{-\alpha} \tag{44}$$

where a(T) is the temperature dependent pre factor, x is the percentage titanium, α is the critical exponent and $x_c(T)$ is the percolation threshold, i.e. the Ti percentage at which a continuous transport network is formed by the metallic grains. The value of the exponent α was set to 2 as this it the typical value for granular films such as co sputtered Au-SiO_2 [153]. Using this number and equation 44, the best fit was determined by the R square test for the parameters a and x_c using Matlab. The R-

square value for this fit was 99 % for all values of annealing temperature except for T_A = 500 °C where the R-square value was 96 %. These values are plotted in Figure 115

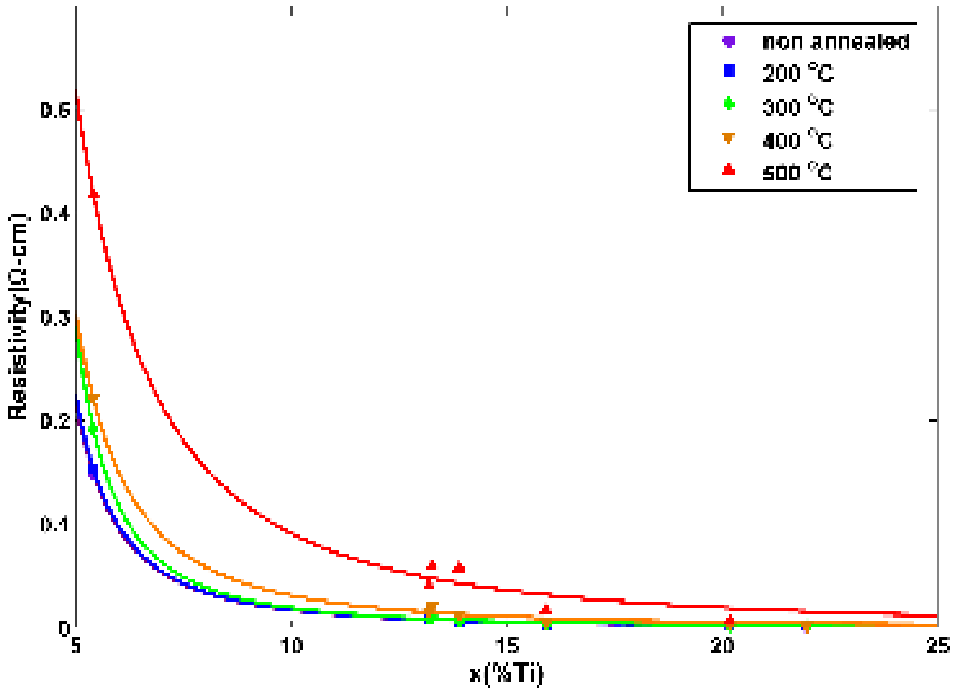


Figure 114: Plots of the resistivity as a function of the titanium content in % weight at 5 different annealing temperatures: non annealed (purple circles), 200°C (blue squares) 300°C (green diamonds) 400°C (orange triangles) and 500°C (red triangles). The solid lines are the nonlinear regression fits of the formula $\rho = a(T)(x - x_c(T))^{-\alpha}$ to the data.

To confirm this scaling behaviour, x/x_c versus $\rho x_c^{\alpha}/a$ at different temperatures was plotted which shows a good data collapse into a single curve $y = (x-1)^{-2}$. The result is shown in Figure 115. The excellent data collapse justifies the value of 2 for the critical exponent.

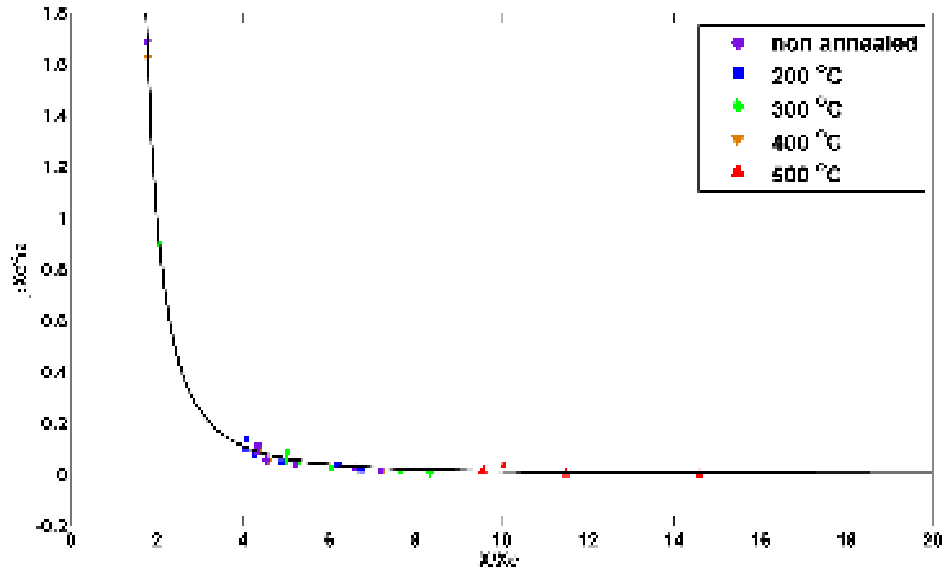


Figure 115: Data collapse at different annealing temperatures in the rescaled variables $x=x_c$ versus $\rho x_c^{\alpha}/a$. The value of the exponent is $\alpha = 2$.

The etch rate of the films was then investigated. Using one sample of each composition, half the sample was masked off using tape and then placed into an OPT RIE80+ etcher. The samples were then etched using 20 sccm SF_6, 10 sccm O_2 at a temperature of 20 ^{o}C, pressure of 15 mTorr and a power of 20 W for 5 minutes. Using the step created by the masked off area the etch rate could be calculated as shown in Figure 116.

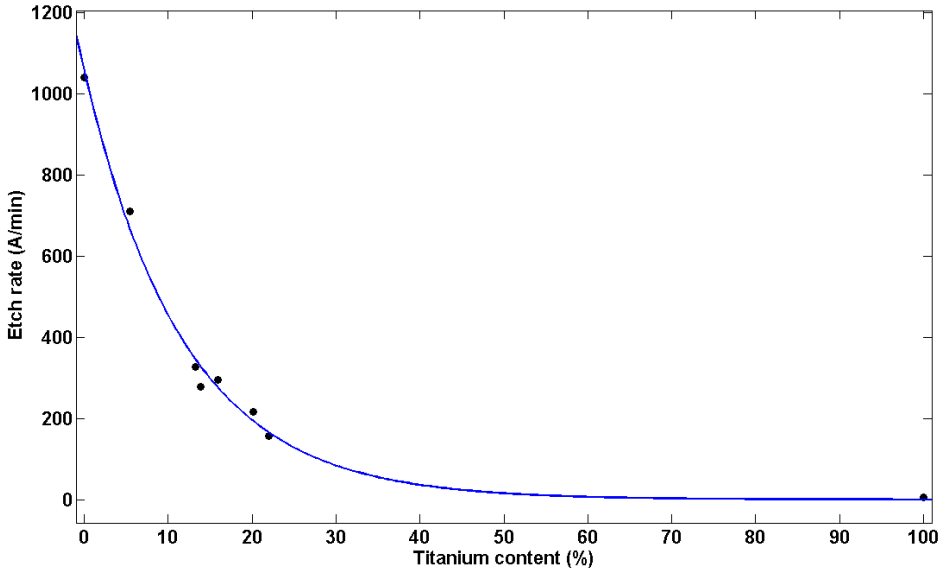


Figure 116: Graph showing the etch rate of the silicon titanium films as a function of the percentage titanium.

6.4. Discussion

The value of the exponent α is close to the value found for co-sputtered gold and silicon oxide (Au-SiO), which was 2.16 in films for which the grain size is much smaller than the film thickness (three dimensional film matrix) [153]. These observations are reminiscent of a percolation process in three dimensional composite materials.

The thin films investigated here have a grainy structure as shown in Figure 113, with the grain size smaller than the thickness of the film by at least a factor of 10 at all annealing temperatures. These films can be viewed as a random resistor network where grains are either conductive or nonconductive, depending whether they are titanium grains or silicon grains. Indeed, the universality of α was confirmed by several numerical computations of random resistor network models which have confirmed that $\alpha \sim 2$ for three dimensional lattices [154, 155]. A similar investigation of co-sputtered silicon-titanium films was carried out by Murarka and Fraser[156]. Their films were grown on poly-Si and silicon oxide substrates. They found evidence of silicides of titanium (TiO_2) component after annealing of the films in temperatures ranging from room temperature to 1000 ^{o}C. No silicides of titanium were found below 500 ^{o}C. More importantly, the presence of silicides induces a decrease of the films' resistivity. This is in contrast to the result shown here where the resistivity of the films increased with increasing annealing temperature as shown in Figure 114. These observations along side the percolative behaviour in the resistivity of films, is strong evidence that in the films no or negligible silicides are present and that the films can be viewed like a three dimensional random network of metallic and semiconducting grains.

The universality of α is not altered by the annealing process, since the grain size remained smaller compared to the films thickness after annealing. This means the value of the critical exponent is independent on the microstructure of the film. On the other hand, the threshold value of the titanium contents decreased with the annealing temperature, while the pre factor *a* increased. These two parameters are determined by the film's microstructure and the mean inter-grain junction conductance. During

annealing the grains undergo coalescence and as a consequence their average size increases. The parameter x_c is the minimum fraction of titanium for which at least one group of grains expands from one side to the opposite one of the area in consideration i.e. a percolation path.

The decrease in threshold x_c is attributed to the coarsening of the grains which induces the formation of percolation paths. Notice that the decrease of the threshold, shown in Figure 114, occurs only at annealing temperatures higher than 300 ^{o}C, where one expects the coarsening process to be significant.

6.5. Conclusion

The main purpose of this study was to provide a material that can be processed at low temperatures opening the possibility of compatibility with IC technology. Amorphous silicon alone has limited functionalities as it is difficult to dope effectively, which means it is not suitable for many modern MEMs applications. Metal layers normally have to be employed as conductive cladding [157] for a-Si to enable the device functionalities, which complicates the microfabrication processes, as well as introducing residual stress, which is one of the key factors causing deterioration in MEMS performance.

This work provides a low temperature method to form a-Si/Ti layers with tailored conductivities that are suitable for MEMS and IC monolithic integration. This study provided an understanding of electrical properties of such material and gives an insight into the physical mechanism behind those properties. The a-Si/Ti layers are also compatible with common microfabrication processes such as effective dry etching using SF6 plasma as has been shown. Thus significantly reducing the potential fabrication cost usually associated with any other new MEMS structural materials developed thus far. Furthermore the a-Si/Ti films possess smooth surfaces. This combination of factors suggests this material has the potential to be a structural material for future IC MEMS devices.

These films could be used in MEMS devices requiring a structural layer that is also conductive. One such application would be an electrostatic actuator or cantilever system. Currently such devices are often fabricated in poly silicon and a conductive metal is deposited on top to allow voltages to be applied. This extra layer can involve multiple new process steps and can also lead to extra fabrication problems such as with the bonding process. The ability to have a structural layer which also has a tuneable conductivity would greatly simplify the fabrication processes

Chapter 7

Conclusion

For a truly integrated atom chip device to be created many elements must be integrated onto a single device. To date most atom chips merely perform one function, usually guiding, with other functions either performed off chip or using macro scale components. Working towards a truly integrated portable device this thesis aimed to replicate these macroscopic capabilities on the micro scale of the atom chips.

The aim of this research was first to develop fabrication processes suitable for the unique requirements of atom chip manufacture. Secondly using these techniques to design and fabricate novel atom chips by integrating magnetic and optical elements onto a single device that can be used to trap and manipulate ultra cold atoms and Bose Einstein condensates.

A ‘tool box’ of techniques was developed to help in these aims. This included developing existing fabrication techniques to meet the unique needs of atom chip devices as well as creating new recipes and techniques where existing ones were not available. Using these techniques a number of devices were fabricated which not only demonstrated that integration of these elements is possible but also created useful devices in their own right.

Wire fabrication was the key component to all atom chips as it is these that act to help trap the initial atoms as well as guide them into the desired position on the devices. A study into the suitability of different fabrication methods was therefore undertaken. For integration purposes electroplated wires are the most suitable as they can be easily added to existing fabrication processes without large modifications. For this reason a detailed study into the production of wires by electroplating was performed and the process was characterised for optimisation with regard to cold atom trapping.

A new approach was then developed which allows microscopic MOTs to be integrated into a silicon chip to collect small atom clouds that are automatically well positioned with respect to the traps on the chip removing the complicated loading and dispensing techniques previously needed.

The MOTs' automatically prepare all the required light beams from a single circularly polarised input beam by reflecting the light in a concave square pyramid of mirrors. This greatly reduces both the number of expensive optical components needed to prepare the light beams and the amount of laser power needed. Integrated wires encircling the base of the pyramid produce the required magnetic field with modest electrical power consumption and accurate positioning. The fabrication of an atom chip with integrated micro MOTs was achieved and using these devices atom clouds have been created. The fabrication of an integrated MOT array on a chip represents an important step towards a truly integrated atom chip for portable applications.

Having developed methods integrating the initial trapping and the guiding onto a micro scale atom chip, a method for detecting and addressing the atoms was created. Towards this aim, a micro cavity was fabricated. An in depth study of its formation has led to a fabrication process that can produce hemispherical cavities with only small aberrations. An ICP polishing recipe was then developed capable of smoothing the silicon surface to an RMS of ~0.5 nm. Using this cavity it has been shown that an optical resonator could be constructed capable of single atom detection and single photon production.

Finally a study into the effect of using titanium as the co-sputtered metal to create a novel MEMS structural material was undertaken. Titanium was chosen because it is a conductive metal that has close properties to that of poly-Si, it can also be DRIE etched allowing the film to be fabricated into devices easily. The main purpose of this study was to provide a material that can be processed at low temperatures opening the possibility of compatibility with IC technology. Amorphous silicon alone has limited functionalities as it is difficult to dope effectively, which means it is not suitable for many modern MEMS applications.

This work produced a low temperature method to form a-Si/Ti layers with tailored conductivities that are suitable for MEMS and IC monolithic integration. The a-Si/Ti layers are also compatible with common microfabrication processes, such as effective dry etching using SF6 plasma. This significantly reduces the potential fabrication cost usually associated with any other new MEMS structural materials developed thus far.

In conclusion the main aims of this thesis have been achieved. Multiple fabrication techniques have been developed and then successfully implemented in the fabrication of atom chips. The first step towards integrated atom chips has been achieved. The next step would be to use the foundations built in this thesis to create a multi function device for real world applications.

7.1. Future work

The initial characterisation of the hemispherical micro-cavities showed some interesting properties. Further study into the cavity fabrication would be very useful for further understanding the shape evolution which should in turn lead to better control of the shape produced. Two main avenues of investigation arose from the results obtained. First the ICP etching recipe itself might be further improved as currently it has the effect of decreasing the sphericality of the cavities due to its slight anisotropy. Improving the isotropy of the etch itself would be a big step towards fabrication of better cavities. The effect of the substrate wafers crystal orientation is also of interest, as it is this that causes the inherent anisotropy. It may be possible to improve the shape by better selection of base substrate.

The creation of a single atom chip that allowed on chip trapping via micro MOTs, guiding via the wires, and single atom detection via the hemispherical micro-cavities, would allow some very interesting devices to be constructed. Using such parts it can be easily envisioned that a single device would allow the creation and reading of single atoms for quantum information exchange.

Currently the optical detection of atoms relies on the presence of an optical fibre. A solution to allow easy alignment and tuning of the cavity has been demonstrated within the research project with the creation of a 1D actuator. The design and fabrication of a 2D and 3D actuator has also almost been completed. Integrating this into a chip containing all the structures developed in this thesis could lead to a single device able to trap, guide, count and even address single atoms.

Appendix 1

In this appendix, the Matlab code used to find the edge of the spherical microcavities from an optical microscope image.

```
% Clear Workspace & Command Window
clear all;
clc;

% Read image and turn into edge diagram

im=imread('w10_20BAWresized.png');
J=rgb2gray(im);
BW2=edge(J,'roberts');

% Create matrix of position
num_i=782;
num_j=779;

Ycd=zeros(num_i,num_j);
Xcd=zeros(num_i,num_j);

for j=1:1:num_j;

     Ycd(:,j)=782:-1:1;

end

for i=1:1:num_i;

     Xcd(i,:)=1:779;

end

 Xcd=Xcd-386.0;
 Ycd=Ycd-396.0;

%  Make matrix real dimensions
Xcd=Xcd*0.16;
Ycd=Ycd*0.16;

% Turn X,Y into polar
Radiusmatrix=(sqrt((Xcd.^2)+(Ycd.^2)));
theta = atan(Ycd./Xcd);
%
% Find edge positions in image
[r,c] = find (BW2==1)
edgepos(:,1)=r(:,1);
edgepos(:,2)=c(:,1);
%
% Convert edge positions into polar and rad positions
thetapos=zeros(length(edgepos),1);
Radiusmatrixpos=zeros(length(edgepos),1);
```

```
for i = 1:length(edgepos)

    thetapos(i) =theta (edgepos(i,1),edgepos(i,2));

     Radiusmatrixpos(i) = Radiusmatrix (edgepos(i,1),edgepos(i,2));
 end

thetaposdeg=thetapos*(180/pi)
Radiusmatrixpos= sqrt (Radiusmatrixpos.^2)

fig2=polar(thetaposdeg, abs(Radiusmatrixpos)-
mean(Radiusmatrixpos),'o');
fig2=plot(thetaposdeg, (Radiusmatrixpos),'o');
```

Appendix 2

In this appendix, the Matlab code used to find the best fix sphere to the spherical microcavities is presented.

```
% Clear Workspace & Command Window
clear all;
clc;

% Set Start, Final and interval values
initial_z =76;
z_inc = .1;
final_z = 79;

initial_r = 111;
r_inc = .1;
final_r = 114;

initial_x = 81;
x_inc = .1;
final_x = 83;

% Calculate number of values for y, r & x.
num_z = ceil(((final_z - initial_z)/z_inc) + 1);
num_r = ceil(((final_r - initial_r)/r_inc) + 1);
num_x = ceil(((final_x - initial_x)/x_inc) + 1);

% Read data from data file
w18 = dlmread('w18-3d.txt');
x18=(w18(:,1));
y18=(w18(:,2));
z18=(w18(:,3));

x182=(w18(:,1));
y182=(w18(:,2));
z182=(w18(:,3));

% i=find(sqrt(((x18-75.2).^2)+((y18-72.1).^2))>10);
% x18(i)=[];
% y18(i)=[];
```

```
% z18(i)=[];
i=find(z18>-6);
z18(i)=[];
x18(i)=[];
y18(i)=[];

yo=76.3

% init 3D array
yressqsum = zeros(num_z,num_r,num_x);
%
%
for z = 1:1:num_z
     for r=1:1:num_r
         for x=1:1:num_x

%
%              yfit(y,r,x)=;
%              yresidual=y18-yfit;
%             yresidualsquared=yresidual.^2;
%             yressqsum=sum(yresidualsquared)
            zo  = ((z - 1)*z_inc) + initial_z;
            rad = ((r - 1)*r_inc) + initial_r;
             xo  = ((x - 1)*x_inc) + initial_x;

            step0 = (y18-yo).^2;
            step1 = (x18-xo).^2;
            step2 = rad^2;
            step3 = step2 - step1 - step0;
            step4 = sqrt(step3);
            step5 = (zo - step4);
            step6 = (z18-(step5)).^2;
            zressqsum(z,r,x) = sum(step6);
          %  yressqsum(y,r,x) = sum((y18-(yo-sqrt(rad^2-(x18-
xo).^2))).^2);

         end
     end
 end

%
% % % Find minimum value in row and returns row number
  [intvalue,zvalue] = min(zressqsum);
% % % Find minimum value in column and returns column number
  [intvalue,rvalue] = min(intvalue);
% % % Find minimum value in z-plane and returns z-index number
  [minvalue,xvalue] = min(intvalue);

 %yvalue = yvalue(1);
 %rvalue = rvalue(1);

  rvalue = rvalue(xvalue);
  zvalue = zvalue(rvalue);

  minzo  = (zvalue - 1)*z_inc + initial_z;
  minrad = (rvalue - 1)*r_inc + initial_r;
  minxo =  (xvalue - 1)*x_inc + initial_x;
%
minzo
```

```
minrad
minxo
minvalue
 zfit=minzo-sqrt(minrad^2 - (x18-minxo).^2 - (y18-yo).^2);
%  i=find(zfit>28.5);
%  zfit(i)=28.5;
 zresidual=(z18-zfit);
 zressq= (zresidual).^2;
 zressqsum = sum(zressq)

 rsquare= 1 - (zressqsum/sum((z18-mean(z18)).^2))

 figure (1)
 scatter3 (x18,y18,z18 )
 figure (2)
 scatter3 (x18, y18, zfit)
 figure (3)
 scatter3 (x18,y18,zresidual)

%plot (x18, ymanualfit , x18 , y18, x18, yplot)

zfit2=minzo-sqrt(minrad^2 - (x182-minxo).^2 - (y182-yo).^2);
zresidual2=(z182-zfit2);
 zressq2= (zresidual2).^2;
 zressqsum2 = sum(zressq2)
```

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