UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING, SCIENCE AND MATHEMATICS
SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

Electrodeposited Ni/Ge and Germanide Schottky Barriers for Nanoelectronic Applications

by

Muhammad Khaled Husain

A thesis submitted in partial fulfilment of the requirements for the award of Doctor of Philosophy at the University of Southampton

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ABSTRACT

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In recent years metal/semiconductor Schottky barriers have found numerous applications in nanoelectronics. The work presented in this thesis focuses on the improvement of a few of the relevant devices using electrodeposition of metal on Ge for Schottky barrier fabrication. This low energy metallisation technique offers numerous advantages over the physical vapour deposition techniques. Electrical characteristics of the grown diodes show a high quality rectifying behaviour with extremely low leakage currents even on highly doped Ge. A non-Arrhenius behaviour of the temperature dependence is observed for the grown Ni/Ge diodes on lowly doped Ge that is explained by a spatial variation of the barrier heights. The inhomogeneity of the barrier hights is explained in line with an intrinsic surface states model for Ge. The understanding of the intrinsic surface states will help to create ohmic contacts for doped n-MOSFETs. NiGe were formed single phase by annealing. Results reveal that by using these high-quality germanide Schottky barriers as the source/drain, the subthreshold leakage currents of a Schottky barrier MOSFET could be minimised, in particular, due to the very low drain/body junction leakage current exhibited by the electrodeposited diodes. The Ni/Ge diodes on highly doped Ge show negative differential conductance at low temperature. This effect is attributed to the intervalley electron transfer in Ge conduction band to a low mobility valley. The results show experimentally that Schottky junctions could be used for hot electron injection in transferred-electron devices. A vertical Co/Ni/Si structure has been fabricated for spin injection and detection in Si. It is shown that the system functions electrically well although no magnetoresistance indicative of spin injection was observed.

Declaration of authorship

I, Muhammad Khaled Husain, declare that the thesis entitled:

"Electrodeposited Ni/Ge and Germanide Schottky Barriers for Nanoelectronic Applications"

and the work presented in it are my own. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what I have contributed by myself and for the integrality of projects, I have made clear what was done by others.
- parts of this work have been published in research journals. A list of publications is provided with this manuscript.

Signed:

Date:

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List of Publications

Articles

Inhomogeneous Ni/Ge Schottky barriers due to variation in Fermi-level pinning

X. V. Li, **M. K. Husain**, M. Kiziroglou and C. H. de Groot, Microelectronic Engineering, Vol. 86 (7-9), pp. 1599-1602,2009.

High-quality Schottky contacts for limiting leakage currents in Ge-based Schottky barrier MOSFETs

M.K. Husain, X. V. Li, and C.H. de Groot, IEEE Transactions on Electron Devices, Vol. 56, No. 3, pp.499-504, 2009.

High-quality NiGe/Ge diodes for Schottky barrier MOSFETs

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Observation of negative differential conductance in a reverse-biased Ni/Ge Schottky diode

M.K. Husain, X. V. Li, and C.H. de Groot, IEEE Electron Device Letters, Vol. 30, No. 9, pp.966-968, 2009 .

A vertical transport geometry for electrical spin injection and extraction in Si

M.K. Husain, X. V. Li, and C.H. de Groot, Solid State Communications, Vol. 149, pp.1565-1568, 2009.

Conference Presentations

Electrical spin injection and extraction in Si in a vertical transport geometry

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High-quality Schottky contacts for limiting leakage currents in Ge based Schottky barrier MOSFETs

M.K. Husain, X. V. Li, and C.H. de Groot, UK Semiconductors conference 2008, Sheffield, UK.

High-quality NiGe/Ge contacts for Schottky barrier MOSFETs

M.K. Husain, X. V. Li, and C.H. de Groot, E-MRS Spring Meeting, 2008, Strasbourg, France.

A study on Ge based spin-LED for spintronic applications

M.K. Husain, X. V. Li, and C.H. de Groot, Condensed Matter and Materials Physics, 12-13 April 2007, University of Leicester , UK

List of symbols

a, b, c	Lattice constants
d	Broadening of an XRD peak
d_{Res}	Resolution of XRD
$d_{Observed}$	Observed broadening of an XRD peak
$e-$	Electron
$h+$	Hole
k	Boltzmann constant
k_l	A fitting parameter of Lombardi model
i_o	Exchange current density
i_L	Mass transport limited current
$m*$	Effective mass
m_j	Nondegenerate quantum states
n_t	Number of different mobility mechanisms
q	Electron charge
t	Time
t_{ox}	Gate oxide thickness of a MOSFET
v_{sat}	Saturation velocity of electrons
v_1, v_2, v_3, v_4	Electron drift velocities
z	Valency
A^*	Richardson constant
A^r	A fitting parameter of Arora mobility model
B_l	A fitting parameter of Lombardi mobility model
C_l	A fitting parameter of Lombardi mobility model
C	Capacitance
C_{ox}	Gate oxide capacitance
C_b	Bulk concentrations of metal ion in a solution
D_p	Hole diffusion constant
D_n	Electron diffusion constant
D_M	Density of metal M
E_{bgn}	A material parameter for Slotboom model

E_C	Conduction band energy level
E_V	Valence band energy level
E_o	Vacuum energy level
E_F	Fermi energy level
E_m	Most probable energy of tunneling electrons
E_{CNL}	Charge neutrality energy level in a semiconductor
E_g	Semiconductor bandgap energy
E_{eq}	Equilibrium potential of an electrode
G_{CC}	Generation rate in the conduction band
I	Current
I_S	Saturation current
I_{sub}	Subthreshold current
I_{DS}	Drain to source current in a MOSFET
I_{GIDL}	Gate induced drain leakage current
I_{SD}	Source to drain current
J	Current density
J_p	Hole current density
J_n	Electron current density
$J+$	Current density from semiconductor to metal
J-	Current density from metal to semiconductor
J_S	Saturation current density
J_{CC}	Current density of electrons tunneling from bulk to interface conduction bands
L_g	Gate length of a MOSFET
M	A metal
M_w	Atomic weight of metal M
N_A	Avogadro's number
N_d	Donor doping density
N_a	Acceptor doping density
N_i	Total concentration of ionised impurity
N_0	A reference impurity concentration of Arora mobility model
N_{ref}	A reference impurity concentration for Slotboom model

Q	Cathodic charge in electrodeposition
Q_T	Total charge of all reactions during electrodeposition
R_S	Series resistance of a Schottky diode
R_{sh}	Sheet resistance
R_r	Recombination rate
R_g	Gas constant
R_{CC}	Recombination rate in the conduction band
S	Fermi-level pinning factor
T	Temperature
T_{film}	Deposited metal film thickness
T_n	Electron temperature
Vol_M	Volume of metal M
V	Voltage
V_g	Gate voltage of a MOSFET
V_{gsub}	Subgate voltage
V_d	Drain voltage of a MOSFET
V_{DS}	Drain to source voltage in a MOSFET
V_{GS}	Gate to source voltage in a MOSFET
V_T	Threshold voltage
V_n	Depth of Fermi-level below the conduction band
V_i	Intercept of the C^{-2}-V curve with voltage axis
W/L	Aspect ratio of the gate in a MOSFET
X_d	Offset between drain and gate edge
α	Current efficiency of electrodeposition
β_c	A temperature dependent parameter in Canali Mobility model
δ	Thickness of diffusion layer
δ_l	A fitting parameter of Lombardi model
Φ_m	Metal work function
Φ_{CNL}	Energy difference between charge neutrality level and vacuum
Φ_s	Semiconductor work function
ϕ_n	Electron Schottky barrier height
ϕ_p	Hole Schottky barrier height

$\overline{\phi_n}$	Mean electron Schottky barrier height
η	Ideality factor
η_l	A fitting parameter of Lombardi model
Θ	The unit step function
χ	Semiconductor electron affinity
ψ_i	Built-in potential
ψ_s	Surface potential
ρ	Resistivity
$\mathscr{E}$	Electric field
$\mathscr{E}_{eq}$	Equilibrium electric field
$\mathscr{E}_t$	Transverse electric field
$\mathscr{E}_{ref}$	A reference electric field of Lombardi model
$\mathscr{E}_d$	A component of electric field paraller to current flow
$\mathscr{E}_0$	An electric field constant
ϵ_s	Dielectric constant
ϵ_∞	Electronic component of dielectric constant
μ_n	Electron mobility
μ_p	Hole mobility
μ_{dop}	Doping dependent mobility
μ_{min}	A reference mobility of Arora mobility model
μ_d	A reference mobility of Arora mobility model
μ_{ac}	Mobility due to acoustic surface phonons
μ_{sr}	Mobility due to surface roughness
μ_{low}	Low field mobility
Γ_{CC}	Probability of tunneling to conduction band
σ_s	Standard deviation of barrier height
σ^+	Left circularly polarised electroluminescence
σ^-	Right circularly polarised electroluminescence
λ_l	Transverse electric field
λ	Wavelength
ζ	Overpotential of an electrode

List of acronyms

2DEG	2-dimensional electron gas
CMOS	Complementary metal-oxide-semiconductor
FE	Field emission
GIDL	Gate-induced drain lekage
LED	Light emitting diode
MIGS	Metal-induced gap states
nMOSFET	n channel MOSFET
pMOSFET	p channel MOSFET
MOSFET	Metal-oxide-semiconductor field effect transistor
NDC	Negative differential conductance
SB-MOSFET	Schottky barrier MOSFET
SB-nMOSFET	Schottky barrier n-channel MOSFET
SB-pMOSFET	Schottky barrier p-channel MOSFET
SEM	Scanning electron microscope
TE	Thermionic emission
TFE	Thermionic field emission
WKB	Wentzel-Kramers-Brillouin
XRD	X-ray diffraction

Contents

Chapter 1

Introduction

1.1 General

Semiconductor devices have been studied for over 125 years [1]. A metal / semiconductor interface was the first semiconductor device ever studied. This interface can be used as a rectifying contact, that is the device allows electrical current to flow easily only in one direction, or as an ohmic contact, which can pass current in either direction with only a negligible voltage drop. This device is much easier to fabricate than a p-n junction rectifier, which is formed at the interface of a p-type and an n-type semiconductor. During the past forty years components based on metal/semiconductor rectifying junctions have been increasingly used in microelectronics, and research activity has continued with the aim of obtaining a full understanding of the physics of the rectifying barrier formation and the current transport across metal/semiconductor interfaces. Modern surface science analytical methods have been applied to probe the detailed microscopic interactions at interfaces between metals and semiconductors. However, as the transistors sizes are going down to allow higher density of information processing and storage, a flexible and commercially viable technique of fabrication on the nanometre-scale will be required. This imposes a challenge to the growth of electronics industry in future. The conventional metallisation in microelectronics is performed by physical vapour deposition methods like evaporation and sputtering. In contrast, electrodeposition is adopted for metallisation on semiconductors in this project for metal/semiconductor rectifying contact

fabrication. It is shown that this technique gives higher rectification both for Si and in particular for Ge. The fabricated contacts could offer significant improvement of semiconductor device performance for the devices discussed in the next sections.

1.2 A Schottky barrier

A Schottky barrier is the rectifying junction formed by the intimate contact of a metal and a semiconductor having nonequal work functions or electronegativities. The devices is dominated by a majority carrier current flow, i.e., electrons for n-type and holes for p-type semiconductors. Because of the metal on one side of the junction, a Schottky barrier has less depletion layer than a conventional p-n junction diode. This results in less stored charge and faster switching of the device. Design considerations with Schottky barriers are limited in some applications compared to p-n junction rectifiers because their reverse leakage currents are many times higher. Still the physical and transport properties of the Schottky barrier contacts are of huge interest because of their much easier fabrication and potential applications in nanoelectronics as well as spintronics.

1.3 Schottky barriers in conventional MOSFETs

Metal-oxide-semiconductor field effect transistors (MOSFETs) have demonstrated a continuous pace in performance improvement over the past thirty years due to aggressive device scaling at the cost of more and more complex process engineering. As the scaling of the modern complementary MOSFETs continue, Si is approaching its fundamental scaling limits. To overcome this, Ge is proposed as an alternative channel material. This new material offers higher bulk carrier mobilities for both electron and hole than Si at low electric fields. Currently, one of the big challenges imposed by ultra-scaled Ge based devices is the formation of ultra shallow, highly doped source/drain regions, keeping the parasitic series resistances as low as possible. The Fermi-levels at any metal/Ge interfaces are pinned near the valence band edge of Ge. So, ohmic characteristics for p-Ge and Schottky characteristics for n-Ge are observed irrespective of metal work functions. This results in high parasitic resistance

in the source/drain of n-channel Ge MOSFETs. In order to reduce this parasitic resistance a mechanism of Fermi-level de-pinning at the metal/nGe interface would be required. Hence, an investigation and clear understanding of the Fermi-level pinning mechanism in metal/Ge Schottky barriers is of great importance.

1.4 Schottky barriers as source/drain in MOSFETs

As discussed in the previous section, the continuing drive towards high integration is causing the semiconductor industry to consider significant scaling by device modifications and incorporation of new materials in order to improve transistor performance. New device structures are also being considered to replace the MOSFETs when conventional scaling fails. One such structure is the Schottky barrier MOSFET [2, 3] (SB-MOSFET). In this device, the problems associated with doping are completely eliminated by forming metallic silicide source and drain contacts. Unlike a doped source-drain architecture, the metallic silicide junctions form an atomically abrupt interface to the substrate and channel region, making the device scalable to the sub-10 nm regime with relative ease. The silicided junctions result in a low series resistance, provide an easy method to produce ultra-shallow junctions and overcome the solid solubility limitation associated with doping. The SB-MOSFET can realise complimentary operation by choosing a low work function metal for nMOSFET (electrons as majority carriers) and a high work function metal for pMOSFET (holes as majority carriers).

A SB-MOSFET imposes several challenges for obtaining high drive current and at the same time low off state leakage current for a given channel doping density. For a SB-MOSFET, it may be difficult to achieve high drive current due to the relatively high potential barrier between the source and the channel [4]. This problem may be overcome, or at least alleviated, by using a Ge substrate as opposed to Si because of the low Schottky barrier height of germanide/Ge contact and the higher carrier mobility of Ge. High drive current could also be achieved by reducing the doping density in the channel region increasing the channel mobility for a long channel MOSFET. Another challenge is to obtain high or nearly ideal electron barrier heights on nGe for the source drain of a pMOSFET by metal deposition and keeping the Fermi-

level pinning intact up to the annealing temperatures where germanidation results in the lowest specific resistance of the metal germanides. As Ge is a narrow band-gap semiconductor, Ge-based SB-MOSFET is badly affected by off-state leakage currents which result from tunnelling current through the Schottky barrier at the drain end, which is sensitive to barrier heights. To overcome this problem, electrodeposition of metals on semiconductor could be performed in order to obtain high Schottky barrier heights [5, 6] at the drain contact as opposed to those formed by physical vapour deposition. By using this technique, the junction leakage currents in an SB-MOSFET could be minimised.

1.5 Schottky barriers in Gunn diodes

A Gunn diode, also known as a transferred-electron device, is a form of diode used in high-frequency electronics. The active area of a Gunn diode consists only of n-doped semiconductor material (e.g. GaAs, Ge, GaN and InP) with two electrical contacts on opposite ends. These semiconductors are characterised by having two valleys in their conduction bands with different mobility. When a proper bias is applied, inter valley electron transfer occurs and the diode exhibits negative differntial resistance. Gunn diodes made of conventional III-V compound semiconductors (e.g. GaAs) have been successfully applied for generation of high-power millimeter-wave signals using oscillators based on the negative resistance effect. Injection limited cathode contacts of linearly-graded $Al_xGa_{1-x}As$ have been used to increase the efficiency of the Gunn devices. However, a simpler Schottky barrier contact has not been explored as a means of hot electron injection over the barrier, particularly because of the high barrier heights of most metals with GaAs. As an alternative, hot carrier injection by tunneling mechanism through the Schottky barriers could be explored. Electrodeposition method could be adopted to form a sharp metal/semiconductor interface on a highly doped semiconductor to enable hot electron tunneling. This may result in hot electron injection in a Gunn diode, which would benefit from a simpler fabrication of Schottky barrier contacts.

1.6 Schottky barriers in Spin transistors

The operation of a conventional MOSFET is dependent on the charge of electrons or holes. A spin transistor uses the angular momentum of an electron, called spin, apart from its charge. In the corresponding research area, Spintronics, a two-channel model is assumed for the possible states of spin-up and spin-down electrons, between which rarely occurs any interchange of states. Albert Fert and Peter Grunberg independently discovered the giant magnetoresistance (GMR) effect in 1988 [7, 8] and won the 2007 Nobel Prize in physics for their work. GMR is the first effect directly related to spin dependent transport. The commercial success of the two-terminal all-metal GMR device as magnetic read heads and magnetic random access memory, resulted in an enormous interest in three terminal semiconductor based hybrid spin transistors [9–12].

The first prototypical spin transistor scheme presented in Fig. 1.1 was proposed by S. Datta and B. Das [13] in 1990. A current passes through a ferromagnetic source and becomes spin polarised. This current is then injected into a semiconductor through a tunneling or a Schottky barrier contact. The current flow through the semiconductor is modulated using an external modulation bias. Finally the spin polarised current is collected at a second ferromagnetic drain contact.

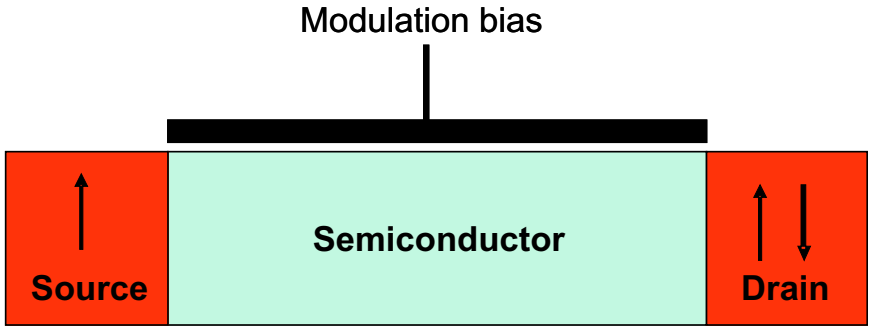

Figure 1.1: An example of a spin transistor structure. The source and the drain are ferromagnets while the channel is a semiconductor. A spin-dependent modulation mechanism controls the spin current flow through the semiconductor.

The semiconductor based spin transistor is a very promising alternative to conventional transistors. The relative advantages of a spin transistor over a conventional transistor could be its operation at terahertz frequency, lower power, smaller size, larger scale of integration and lower cost. However, current gain is the property lack-

ing in the spin transistors developed so far and this has become the main obstacle for its integration with conventional electronic circuits. Semiconductor materials offer the possibility of new device functionalities, which are not realisable in metallic systems. For example, equilibrium carrier densities in semiconductors can be varied through a wide range by doping. Moreover, as the typical carrier densities in semiconductors are low compared to metals, electronic properties are easily tunable by gate potentials. A vast body of knowledge concerning semiconductor materials and processing already exists. Many of these processes have already been scaled up to commercial production lines. All these factors make semiconductors the natural choice for hybrid spintronics specifically for realising spin transistors.

For successful fabrication of a semiconductor spin transistor, the major challenge is the transfer of spin polarised carriers into a semiconductor such as Si or Ge. The main obstruction in this process is the conductivity mismatch problem which could be overcome by using a Schottky barrier contact of a ferromagnet with a semiconductor. Electrodeposition of a metal could be very useful as opposed to other deposition techniques since it produces very sharp interface with the semiconductor without intermixing. The second challenge followed by spin injection is obviously to detect the injected carriers in the semiconductor. A Schottky contact at the drain could be used for this detection. The spin polarised electrons results in a high magnetoresistance signal in the detection electrode when its magnetisation direction is opposite to that of the injection electrode. In this work, spin injection in Si will be electrically investigated using Schottky barriers at the injection and detection contacts.

1.7 Outline of this thesis

The thesis is organised as follows:

Chapter 2 discusses in detail the physics of Schottky barrier contacts and their characterisation techniques. An introduction to the metal electrodeposition technique is presented. Moreover, an introduction to the numerical simulation tool Sentaurus Device that has been used to simulate Schottky barriers and MOSFETs in this project is given.

Chapter 3 presents an investigation on the barrier inhomogeneity in Ni/Ge Schot-

tky barriers. The spatial variation of a Schottky barrier height is explained in light of modern theoretical models. The results help us understand the mechanism of Fermi-level pinning and its dominance in the source/drain formation and the solution to mitigate the effect in doped source/drain MOSFETs.

In Chapter 4, the theory of SB-MOSFETs is presented, emphasising the difference with the scaling limitations of the conventional MOSFETs. The experimental results of high-quality Ni/Ge Schottky barriers grown by electrodeposition is presented. The fabricated Schottky barriers show excellent rectification with very low leakage current. By numerical simlation it is shown that such high quality contacts could be used in SB-MOSFETs to suppress subthreshold leakage currents.

In Chapter 5, the experimental observation of negative differential conductance in a Ni/Ge Schottky barrier is reported. With the aid of theoretical models and numerical simulation it is shown that, at reverse bias, electons tunnel into the high electric field of the depletion region of the Ni/Ge Schottky barrier. This scatters the electrons into the upper valley of the Ge conduction band, which has a lower mobility. The observed effect is hence attributed to the transferred electron effect, typical in a semiconductors with two-valley conduction bands, eg. in GaAs and InP.

In Chapter 6 an overview of various fundamental principles underpinning electrical spin injection to semiconductors is presented. Electrical spin polarised carrier injection and extraction in Si has been investigated using a Co/Si/Ni vertical structure built on Si membrane. Electrical characteristic measurements performed on the devices at low temperatures show evidence of the conduction being dominated by tunneling. The devices, however, did not show any magnetoresistance signal even at low temperatures. Numercial simulations are performed to identify the possible reason hampering the spin injection. Investigation shows that the resistance-area product at the spin injection contacts hampers spin polarised carrier injection. This could be overcome by growing a thin highly doped Ge layer at the Schottky junctions, which tunes the resistance-area products to obtain spin injection in Si.

Chapter 2

Schottky barriers

In this chapter the background on a metal/semiconductor Shottky barrier contact, its formation, current transport mechanisms are presented. A brief introduction to the Fermi-level pinning mechanism is given. Various experimental methods for extracting Shottky barrier parameters are discussed. As a fabrication technique of metal/semiconductor Shottky barrier, electrochemical deposition technique is briefly introduced. An introduction to the numerical simulation tool Sentaurus Device that has been used to simulate the Ni/Ge Shottky barriers in this project is given.

2.1 Introduction

Metal/semiconductor contacts are of great importance since they are present almost in every semiconductor device. They can behave either as an Shottky barrier or as an ohmic contact dependending on the characteristics of the interface. The difficulties associated with the scaling of conventional doped source/drain MOSFETs could be overcome by using a Schottky source/drain. In the following sections the background on the metal/semiconductor Shottky barrier is presented.

2.2 Formation and operational principles of a Schottky barrier

The energy band diagram of a metal and an n-type semiconductor aligned using the same vacuum level (E_o) is shown in Fig. 2.1a. As the metal and semiconductor are brought together, the Fermi energies of the metal and the semiconductor do not change immediately. This yields the flat-band diagram of Fig. 2.1b, which is not at thermal equilibrium, since the Fermi energy in the metal is lower than that in the semiconductor. The energy of the electrons in the semiconductor is lowered by diffusion of electrons into the metal.

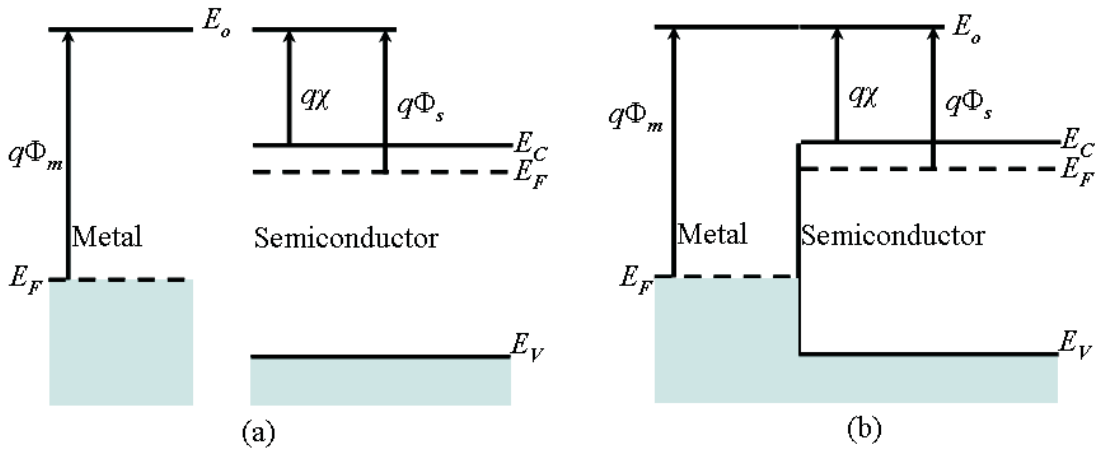

Figure 2.1: Energy band diagram of a metal and a semiconductor (a)before and (b)immediately after a contact is made. Here q, Φ_m, Φ_s and χ, E_o, E_C, E_V, E_F are the electronic charge, the metal work function, the semiconductor work function, the semiconductor electron affinity, the vacuum energy level, the conduction band energy, the valence band energy, and the Fermi-level, respectively.

As the electrons leave the semiconductor, a positive charge, due to the ionised donor atoms, stays behind forming the depletion region. This charge creates a negative field and lowers the band edges of the semiconductor. Electrons flow into the metal until equilibrium is reached between the diffusion of electrons from the semiconductor into the metal and the drift of electrons caused by the field created by the ionised impurity atoms. The corresponding band diagram is shown in Fig. 2.2. This equilibrium is characterised by a constant Fermi energy throughout the structure.

The margin of the metal work function Φ_m and semiconductor electron affinity χ

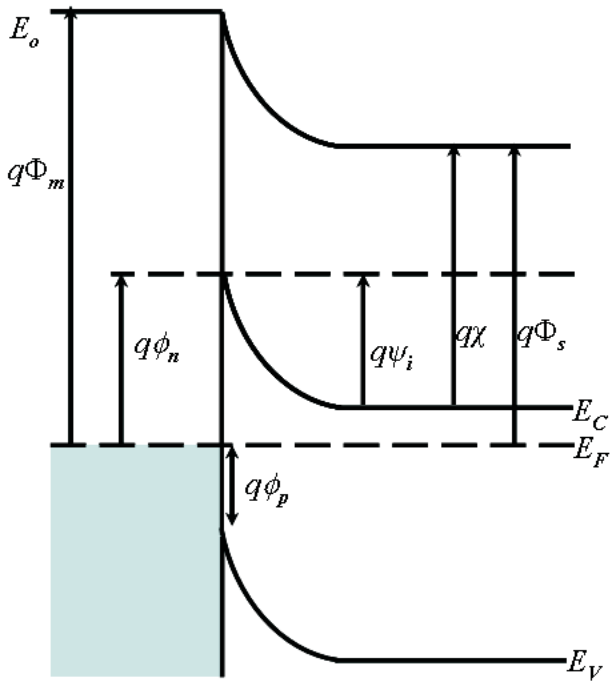

Figure 2.2: Energy band diagram of a metal-semiconductor contact in thermal equilibrium. Here, ϕ_n, ϕ_p and ψ_i are the electron barrier height, the hole barrier height and the built-in potential, respectively.

is defined as the electron barrier height ϕ_n given by:

$$\phi_n = \Phi_m - \chi \tag{2.1}$$

If E_g is the bandgap of the semiconductor then the hole barrier height ϕ_p is given by:

$$\phi_p = \frac{E_g}{q} + \chi - \Phi_m \tag{2.2}$$

where q is the electronic charge and E_g is given by

$$E_g = q(\phi_p + \phi_n) \tag{2.3}$$

The built-in potential ψ_i is defined as the difference between the Fermi energy of the metal and that of the semiconductor:

$$\psi_i = \Phi_m - \chi - \frac{E_C - E_F}{q} \tag{2.4}$$

Experimentally it has been found that equation 2.1 does not correctly predict the barrier height. ϕ_n is strongly influenced by the Fermi-level pinning effect, which is

mainly caused by intrinsic interface states at the semiconductor boundary. Dangling bonds and the species of chemicals adsorbed on the surface of semiconductors give rise to surface states modelled by Bardeen [14]. These states introduce energy levels that are within the energy gap of the host crystal, creating acceptor or donor type surface traps. These states can have a very high density and a narrow distribution of energies within the band-gap. Electrons from the conduction band may be trapped in these surface states. These states typically are sufficiently dense that in equilibrium the Fermi-level falls within them at the surface. As a result, the barrier height is determined by the property of the semiconductor surface and is independent of the metal work function. Moreover, Heine [15] pointed out that localised surface states cannot exist in the semiconductor when it is contacting the metal, but resonance surface states, which are tails of the metal wave functions can exist. The length of this tail can be about a few lattice constant. The gap states tend to lead towards a matching of some neutrality level lying in the gap in each semiconductor. The mechanism of the Fermi-level pinning by this model will be presented in Chapter 3.

The current transport in a Schottky barrier under various bias conditions could be due to the carrier transport over the barrier and through the barrier. In addition there are two more mechanisms such as recombination in the space-charge region and recombination in the neutral region. The overall current can be approximately modelled by a combination of the thermionic emission current and the tunnelling current for semiconductors with a high mobility and low density of defect states because in this case the current from electron-hole recombination and hole injection can be neglected.

2.2.1 Thermionic emission for Schottky characterisation

Ideal Schottky barriers exhibit rectifying behaviour due to carrier emission over the top of the barrier at room temperature. This is known as the thermionic emission (TE) mechanism, which is presented schematically in Fig. 2.3. Only the carriers with energies larger than $q\phi_n$ can overcome the Schottky barrier presented in Fig. 2.3a and contribute to the transport from the metal to the semiconductor or vice versa. Under forward bias condition as shown in Fig. 2.3b, a positive bias is applied to the metal. The semiconductor remains at the same potential but the metal Fermi-level is

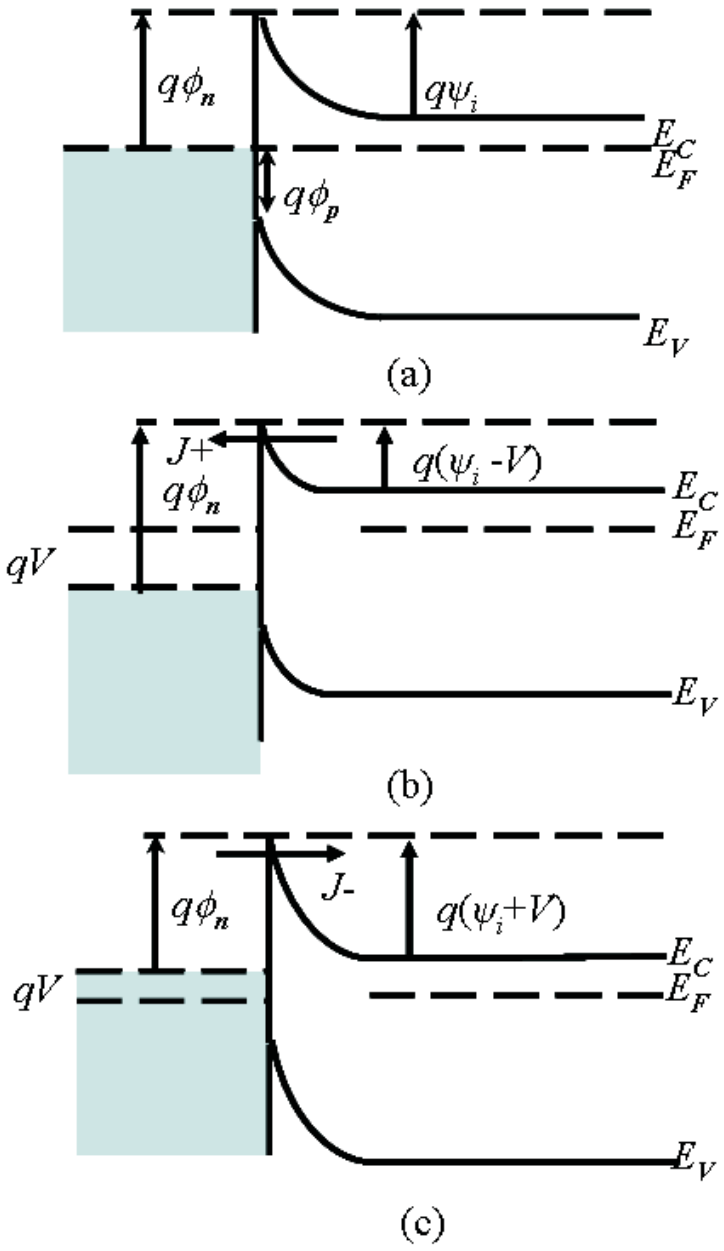

Figure 2.3: A schematic representation of thermionic emission current transport in a Schottky barrier: (a)Equilibrium band diagram without a bias. (b) Band diagram of a forward-biased Schottky barrier when a positive bias V is applied to the metal. Here $J+$ is the current density from the semiconductor to the metal. (c) Band diagram of a reverse-biased Schottky barrier when a negative bias V is applied to the metal. J- is the current density from the metal to the semiconductor.

shifted to lower energies due to the applied voltage and this in turn leads to a lowering of the barrier potential. Hence, the current density $J+$ from the semiconductor to the metal increases significantly. At the same time, the electron current density J- from the metal to the semiconductor remains very small because of a high and almost constant barrier between the metal and the semiconductor. Similarly, under reverse bias condition as shown in Fig. 2.3c, a negative bias is applied to the metal. $J+$ is significantly decreased because the barrier potential is increased. Since J- is almost voltage independent, therefore, the total current for forward and reverse bias is different. The current density (J) of a homogeneous Schottky barrier is given by [1]:

$$J(V) = J_S(e^{\frac{qV}{\eta kT}} - 1) \tag{2.5}$$

where the saturation current density, J_S is defined as

$$J_S = A^*T^2(e^{-\frac{q\phi_n}{kT}}) \tag{2.6}$$

where V is the applied voltage, q is the electron charge, k is the Boltzmann constant, T is the absolute temperature, A^* is the Richardson constant, η is the ideality factor and ϕ_n is the electron Schottky barrier height.

Assuming the TE mechanism as the current transport mechanism across a homogeneous Schottky barrier, current I can be expressed as a function of the applied bias V by

$$I = I_S(e^{\frac{qV}{\eta kT}} - 1) \tag{2.7}$$

where the saturation current I_S, according to equation 2.6, is given by

$$I_S = AA^*T^2(e^{-\frac{q\phi_n}{kT}}) \tag{2.8}$$

where A is the active contact area in cm^2. If the applied bias V is much greater than $3kT/q$ then the exponential part of equation 2.7 dominates and the equation reduces to

$$I = I_S e^{\frac{qV}{\eta kT}} \tag{2.9}$$

$$lnI = lnI_S + \frac{q}{\eta kT}V \tag{2.10}$$

The intercept of the straight line equation gives the value of lnI_S when lnI is plotted in log axis as a function of V for the values of $V \gg \frac{3kT}{q}$. The ideality factor η can be

calculated from the slope of the equation as

$$\eta = \frac{q}{kT}\frac{dV}{d(lnI)}V \tag{2.11}$$

Then the barrier height of the Schottky diode can be worked out by

$$\phi_n = -\frac{ln(I_S/AA^*T^2)kT}{q} \tag{2.12}$$

Moreover the slope of the linear part of the forward I-V characteristics of the Schottky barrier gives the series resistance of the diode.

The height of a Schottky barrier can also be determined by the capacitance (C) measurement. When a small AC voltage is superimposed upon a DC bias, charges of one sign are induced on the metal surface and charges of the opposite sign in the semiconductor. The relation between capacitance C and voltage V for a Schottky barrier formed by a metal and n-type semiconductor is given by [1]:

$$C = \sqrt{\frac{q\epsilon_s N_d}{2(\psi_i - V - \frac{kT}{q})}} \tag{2.13}$$

where ϵ_s and N_d are the permittivity and the doping density of the semiconductor, respectively. From equation 2.13 the doping concentration as a function of the gradient of the inverse square capacitance per unit area can be worked out as:

$$N_d = \frac{2}{q\epsilon_s}(-\frac{dC^{-2}}{dV})^{-1} \tag{2.14}$$

If N_d is constant the plot of C^{-2} gives a straight line and from the gradient of this line the doping density of the semiconductor is obtained. The height of the Schottky barrier is given from the intercept V_i of the extension of the straight line with the voltage axis as [1]:

$$\phi_n = V_i + V_n + \frac{kT}{q} \tag{2.15}$$

where V_n is the depth of the Fermi-level below the conduction band.

The third technique of a Schottky barrier height determination is the activation energy measurement that requires no assumption of electrically active area. By multiplying equation 2.5 by A, the electrically active area, we get

$$ln(\frac{I}{T^2}) = ln(AA^*) - \frac{q(\phi_n - V)}{kT} \tag{2.16}$$

where $q(\phi_n - V)$ is the activation energy. Over a limited range of temperature, the value of A^* and ϕ_n are temperature independent [1]. Therefore, for a given forward bias V, the slope of a plot of $ln(\frac{I}{T^2})$ versus $1/T$ yields the barrier height ϕ_n, and the ordinate intercept at $1/T$=0 yields the product of A and A^*.

The application of an electric field in a Schottky barrier causes the image force lowering of the potential energy for charge carrier emission. Consider an electron in vacuum, at a distance x from a metal surface. A positive charge will be induced on the metal surface and will give rise to an attractive force between the two, known as the image force. The force of attraction between the electron and the induced positive charge is equivalent to the force that would exist between the electron and an equal positive charge located at -x. This positive charge is referred to as an image charge. When an external field is applied these two energy components together have the effect of lowering the barrier height. At high fields, the height of a Schottky barrier is considerably lowered by an amount given by:

$$\Delta\phi = \sqrt{\frac{q\mathscr{E}}{4\pi\epsilon_s}} \tag{2.17}$$

where $\mathscr{E}$ is the applied electric field.

2.2.2 Field emission and thermionic field emission

Under certain circumstances it may be possible for electrons with energies below the top of the barrier to penetrate the barrier by quantum mechanical tunneling. In the case of a very heavily doped (degenerate) semiconductor at low temperature, the current in the forward bias (same for reverse bias) arises from the tunneling of electrons with energies close to the Fermi energy in the semiconductor. This is known as field emission (FE) and is schematically shown in Fig. 2.4. If the temperature is raised, electrons are excited to higher energies and the tunneling probability increases very rapidly as the barrier to them gets thinner and lower. On the other hand, the number of excited electrons decreases very rapidly with increasing energy, and there will be a maximum contribution to the current from electrons which have an energy E_m above the bottom of the conduction band. This is known as thermionic field emission (TFE) and is presented schematically in a forward biased Schottky barrier in Fig. 2.4.

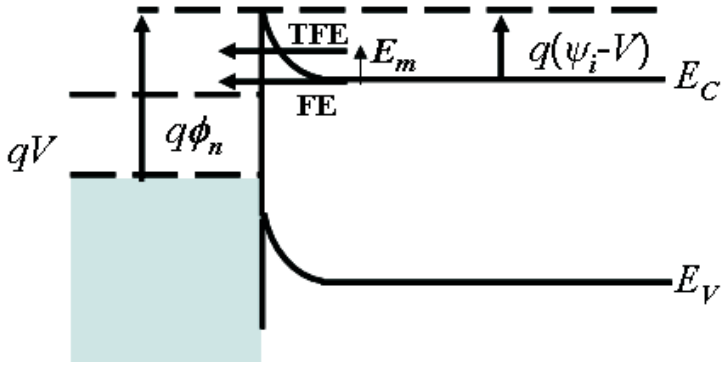

Figure 2.4: A schematic representation of a Schottky barrier energy band diagram indicating the different energies for FE and TFE under forward bias. Here TFE occurs at an energy E_m above the bottom of the conduction band.

2.3 Schottky barrier fabrication by electrodeposition

Electrodeposition is the material deposition technique used in this project to deposit Ni on Ge. Kiziroglou *et al.* [6] compared the transport characteristics of evaporated Ni/Si Schottky barriers with that of the electrodeposited Ni/Si Schottky barriers of the same structure and observed that the latter exhibits higher quality rectifying behaviour than the former. The poor quality rectifying of the evaporated Schottky barrier was attributed to the formation of an interfacial layer at the Ni/Si interface due to the intermixing of the high energy Ni atoms with Si during evaporation. This interfacial layer lowers the Schottky barrier height resulting in the increase of the reverse current density. Therefore, in order to obtain high quality Schottky barrier on Ge, Ni was electrodeposited. This method is attractive since it is very simple, quick and cost effective and does not require any vacuum chamber unlike the conventional material deposition techniques, eg. evaporation and sputtering. However, the method requires a conductive substrate and the lack of it results in poor nucleation, adhesion of the metal film on semiconductor. However, in this work it was found that even low doping in Ge is sufficiently conductive to allow electrodeposition.

2.3.1 Electrodeposition principle

Electrodeposition, also known as electroplating, occurs in an electrochemical cell containing metal ions in a solution, a cathode or substrate upon which the metal is deposited, a reference electrode and an anode or counter electrode as shown schematically in Fig. 2.5. An electric field applied across the two electrodes provides a driving force for the ions to move. The positive metal ions move to the electrode called the cathode, where they gain electrons thereby undergoing reduction to atoms which deposit onto the cathode. A typical electrodeposition reaction for a metal M having a valency z, is given by [16]:

$$M^{z+} + ze^{-} \rightarrow M(solid) \tag{2.18}$$

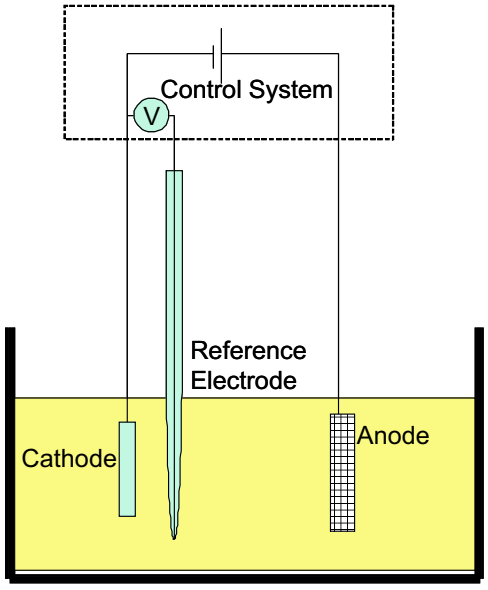

Figure 2.5: A schematic representation of a three electrode electrodeposition setup consisting of the cathode, the anode, and the reference electrode immersed in a solution containing metal ions.

The nature of the deposit is determined by many factors including the electrolyte composition, its pH, the substrate, the potential applied between electrodes and the current density. When an electrode is immersed in an electrochemical solution and no current is flowing through it the surface charges which build up at equilibrium lead to the formation of a potential difference between the metal electrode and the solution. This potential is called the equilibrium potential E_{eq}, which depends on

the material of the electrode and the activity of the metal salt in the electrolyte solution. If an external voltage is applied to the system, a current will flow and the voltage drop *E(I)* across the electrochemical system will in general be different from the equilibrium potential E_{eq}. The difference in these potentials is known as the overpotential ζ given by:

$$\zeta = E(I) - E_{eq} \tag{2.19}$$

If the overpotential is negative and large, then the current-potential relationship during electrodeposition is given by the Butler-Volmer equation:

$$i = i_o exp\frac{-\alpha z N_A q \zeta}{R_g T} \tag{2.20}$$

where i_o is termed as the exchange current density (i_o =i when ζ =0), α the transfer coefficient, N_A Avogadro's Number and R_g the Gas Constant. In reality, this exponential current variation cannot hold for high values of overpotential as the current density is limited by the mass transport of metal ions from the solution to the electrode. The value of the limited current is given by:

$$i_L = \frac{n_e N_A q D}{\delta} C_b \tag{2.21}$$

where D is the diffusion constant for the particular metal ions, C_b is the bulk concentrations of the metal ion in the solution, δ is the thickness of the diffusion layer and n_e is the number of electrons involved in the reaction. Therefore, the current varies exponentially for a certain range of overpotential, but it saturates at the mass transport limit at high overpotential as shown in Fig. 2.6. With increasing potential the current increases linearly until the equilibrium potential of the metal is reached. Then the current increases exponentially while metal deposition is taking place. Finally the current saturates when it is limited by the total mass transport ability of the solution and the electrode. The rate of the metal deposited will vary with the current density due to the difference in the number of available electrons.

In a three electrode electrodeposition setup, the purpose of the anode/counter electrode is to supply the current required by the working electrode without limiting the measured response of the cell. The role of the reference electrode is to provide a fixed potential which does not vary during the experiments. During the deposition

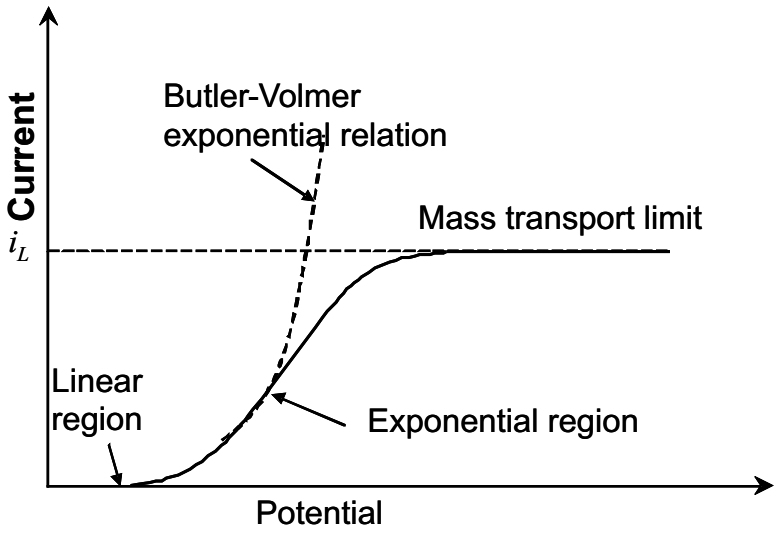

Figure 2.6: Current voltage variation during electrodeposition.

process a potential difference arises at the metal and the solution interface as a result of charging. This potential of the cathode is measured against the reference electrode potential. The potential between the cathode and the reference electrode is controlled by a potentiostat, and as the reference cell is maintained at a fixed potential, any change in applied potential to the cell appears directly across the interface between the cathode and solution. The reference electrode serves dual purposes of providing a thermodynamic reference and also isolating the cathode from the system. In practice, however, any measuring device must draw a current to perform the measurement. Thus, a good reference electrode should be able to maintain a constant potential even if a few microamperes are passed through its surface. In this work, a saturated calomel electrode, consisting of mercury, calomel and KCl has been used as a reference electrode.

There are two different methods of electrodeposition depending on how the current or voltage is applied: the constant voltage method (current is measured during the deposition); and the constant current method (voltage is measured during the deposition). In addition, cyclic voltametry is used in order to optimise the various electrodeposition methods by investigating the nucleation of the deposited films. In this technique an applied voltage is ramped from low to high and then back to low when the current is being measured. The optimum deposition potential is then de-

termined from the cyclic voltametry characteristic. Finally a constant deposition potential is maintained, during the metal deposition process, in which the actual film is deposited.

2.3.2 Film thickness control

The reduction of the metal has been generalised as Equation 2.18 for a single metallic ion. Therefore, to reduce one mole of a given metal z moles of electrons are required. The total cathodic charge used in the deposition Q, is the product of the gram-moles M of the metal deposited, the valency z, Avogadro's Number N_A, and the electronic charge q. Thus, the following equation gives the charge required to reduce M mole of metal:

$$Q = MzN_Aq \tag{2.22}$$

The number of moles of metal reduced by charge Q is:

$$M = \frac{Q}{zN_Aq} \tag{2.23}$$

In the electrodepositon process, two or more reactions may occur simultaneously at an electrode and the amount of total charge passed corresponds to the sum of the charges of all reactions. The current efficiency (α) for one of the simultaneous reaction (metal reduction in our case) is defined as the charge required for that reaction Q_M divided by the total amount of charge Q_T for all reactions. Therefore equation 2.23 can be written as:

$$M = \frac{\alpha Q_T}{zN_Aq} \tag{2.24}$$

The total charge used in the metal deposition can be obtained as the product of the current I and the time of deposition t. The weight of the deposit w can be obtained by multiplying equation 2.24 with the atomic weight M_w of the deposited metal. Finally, to obtain the thickness T_{film} of the deposited metal film, the density of the metal D_M is used as:

$$D_M = \frac{w}{Vol_M} = \frac{w}{AT_{film}} \tag{2.25}$$

where Vol_M is the volume of the deposited metal, A is the area of the deposit. Using Equations 2.24 and 2.25 the general equation of the required charge for the deposition of a film with thickness T_{film} is found to be:

$$Q_T = \frac{zN_A q D_M A T_{film}}{\alpha M_w} \tag{2.26}$$

This charge can be monitored during electrodeposition by observing the current passed in a given time. The current efficiency α could be estimated by measuring the film thickness by scanning electron microscope (SEM) after electrodeposition.

2.4 Device simulation framework

Device modeling of Ge-based Schottky barriers were performed for investigation of Ge channel SB-MOSFETs with dimensions in the sub-100 nm regime, i.e., channel lengths less than 100 nm and gate oxide layers as thin as 1 nm. Investigation of devices with various structures and materials, such as back-to-back Schottky barriers for electrical spin-injection experiment will be shown in Chapter 6. Fabrication of such devices would require complex lithographic techniques and sophisticated material growth processes resulting in very high cost. As a result of this high cost and the fabrication challenges, measurements on fabricated devices are not readily available for comparison with simulation results for this research study. However, this modeling study will provide useful insight into the factors limiting device performance and predict trends in device performance due to variations in device structure and design.

2.4.1 An introduction to the simulation tool

Numerical simulations of Ni/Ge Schottky barriers have been performed by a numerical simulator Sentaurus Device from SYNOPSYS Ltd. This tool is primarily designed for simulating the thermal, electrical, and optical characteristics of silicon devices, and is also capable of simulating other semiconductor materials such as Ge. A set of physical device equations that describe the carrier distribution and conduction mechanisms are used to compute terminal currents, voltages, and charges.

In the simulator, a real semiconductor device is represented as a virtual device whose properties are discretised onto a non-uniform grid or mesh. This is done by

the Sentaurus structure editor tool. A virtual device structure is then defined by two files. One is a grid file containing a description of the various regions within the device, i.e., boundaries, types of materials, location of electrical contacts, as well as the location of all the discrete nodes and their connectivity (the device mesh). The second is a data file containing the doping profiles of the device. Sentaurus device uses these files along with various transport equations and built-in physical models to describe the devices electrical characteristics, as well as the devices internal parameter variations and distributions, such as electrostatic potential, carrier concentrations, carrier mobilities, and carrier velocities.

The electrical terminal characteristics of the device are predicted by solving key semiconductor equations, including Poissons Equation and the electron and hole continuity equations, at the nodes within the device mesh. These equations are given below:

$$Poisson's\ equation : \nabla(\epsilon\nabla\psi) = -q(p - n + N_d^+ - N_a^-) \tag{2.27}$$

$$Electron\ continuity\ equation : \nabla J_n = qR_r + q\frac{\partial n}{\partial t} \tag{2.28}$$

$$Hole\ continuity\ equation : -\nabla J_p = -qR_r + q\frac{\partial p}{\partial t} \tag{2.29}$$

where ψ is the electrostatic potential, p and n are the hole and electron density, N_d^+ and N_a^- are the ionised donor and acceptor concentrations, R_r is the recombination rate. J_n and J_p consists of the drift and the diffusion terms as given by:

$$Electron\ drift - diffusion\ current : J_n = q\mu_n n\nabla\psi\ +\ qD_n\nabla n \tag{2.30}$$

$$Hole\ drift - diffusion\ current : J_p = q\mu_p p\nabla\psi\ -\ qD_p\nabla p \tag{2.31}$$

where D_n and D_p are the diffusion constants, μ_n and μ_p are the electron and hole mobility respectively. The system unknowns are ψ, n and p. The Sentaurus device tool integrates the equations over a test volume, applying the Gaussian theorem, and discretising the resulting terms to a first-order approximation to obtain a solution.

The accuracy of the simulation arises from its accurate description of the physics of device operation. Numerical simulations utilising the many tools provided by the Sentaurus software were performed in order to obtain a realistic description of the Schottky diodes behaviour. Therefore, the device characteristics presented in this thesis are reasonable predictions of what can be expected in fabricated structures.

2.4.2 Simulation models

One of the major advantages of Sentaurus Device is the ability to selectively include specific numerical model functions such as mobility, tunneling effects, bandgap narrowing, etc. In order to obtain an accurate description of the carrier mobilities in the MOSFETs modeled in the simulation study, a physical model is used to describe their affect on the carrier mobilities.

A large variety of models have been developed, which describe mobility dependency on material properties and operating conditions. The mobility models that were used in the simulations of MOSFETs are discussed. Different mobility contributions can be combined according to Mathiessen's rule:

$$\frac{1}{\mu} = \sum_{n_t} \frac{1}{\mu_{n_t}} \tag{2.32}$$

where μ is the carrier mobility, n_t is the number of different mobility mechanisms. In this section the mobility models are reported that have been used in device simulations in this thesis. The reader is referred to Ref. [17] for a detailed explanation of model parameters.

In doped semiconductors, a degradation of the carrier mobility is experienced due to scattering of the carriers by charged impurity ions. The Arora [18] model is used to describe the mobility dependence on the impurity concentrations in MOSFETs built on silicon and germanium. The Arora model reads:

$$\mu_{dop} = \mu_{min} + \frac{\mu_d}{1 + \left(\frac{N_i}{N_0}\right)^{A^r}} \tag{2.33}$$

where μ_{min}, μ_d, N_0 and A^r are the temperature dependent fitting parameters used in the Arora model and N_i denotes the total concentration of ionised impurities.

Large transverse electric fields in the channel region of MOSFETs forces carriers to interact strongly with the semiconductor-insulator interface. As a result, carriers in the channel are subjected to scattering by acoustic surface phonons (μ_{ac}) and surface roughness (μ_{sr}). Sentaurus Device generally uses the Lombardi [19] model to describe the mobility degradation caused by these effects given by:

$$\mu_{ac} = \frac{B_l}{\mathscr{E}_t} + \frac{C_l \left(\frac{N_i}{N_0}\right)^{\lambda_l}}{\mathscr{E}_t^{1/3} \left(\frac{T}{T_0}\right)^{k_l}} \tag{2.34}$$

$$\mu_{sr} = \left(\frac{\left(\frac{\mathscr{E}_t}{\mathscr{E}_{ref}}\right)^{A^*}}{\delta_l} + \frac{\mathscr{E}_t^3}{\eta_l} \right)^{-1} \tag{2.35}$$

where $\mathscr{E}_t$ and $\mathscr{E}_{ref}$ are the transverse electric field and a reference electric field, respectively, B_l,C_l, N_0, λ_l, k_l, η_l, δ_l are fitting parameters. These contributions are combined with the bulk mobility according to the Mathiessens's rule.

In strong electric fields, the carrier drift velocity is no longer proportional to the electric field strength, rather, the velocity saturates to a finite speed. For Ge based devices simulation the Canali model [20] is used to model this effect:

$$\mu(\mathscr{E}_d) = \frac{\mu_{low}}{\left[1 + \left(\frac{\mu_{low}\mathscr{E}_d}{v_{sat}}\right)^{\beta_c}\right]^{\frac{1}{\beta_c}}} \tag{2.36}$$

where the exponent β_c and the saturation velocity v_{sat} are temperature dependent parameters. μ_{low} is the low field mobility, influenced by previously described contributions. the driving force $\mathscr{E}_d$ can be taken as the component of the electric field parallel to the current flow.

At large impurity concentrations the density of energy states no longer possesses a parabolic energy distribution, instead it becomes dependent on the impurity concentration. This results in a reduction of the bandgap due to the broadening of the impurity band along with the formation of bandtails on the conduction and valence band edges. This phenomenon strongly influences the electrical behaviour of the device, in particular, the minority carrier charge storage and the minority carrier current flow in heavily doped regions. Sentaurus device simulates the bandgap narrowing effect using the Slotboom model [21]:

$$\Delta E_g(N_i) = E_{bgn}\left[\ln\left(\frac{N_i}{N_{ref}}\right) + \sqrt{\left(\ln\left(\frac{N_i}{N_{ref}}\right)\right)^2 + 0.5}\right] \tag{2.37}$$

where E_{bgn} and N_{ref} are material parameters.

Sentaurus Device offers three tunneling models namely 1. FowlerNordheim model 2. the direct tunneling model and 3. the non-local tunneling model. The FowlerNordheim tunneling and the direct tunneling model are restricted to trapezoidal tunneling barriers of metal/oxide/semiconductor interface. The magnitude of the tunneling current depends on the band-edge profile along the entire path between the points connected by tunneling. Therefore, computation of tunneling current at a certain point depends on quantities at other points in the structure. This makes tunneling in a Schottky barrier a nonlocal process. Therefore tunneling current at Schottky barriers, heterostructures, and gate leakage through thin, stacked insulators are best approximated by the nonlocal tunneling model.

The non-local tunneling model utilises either the Schrodinger equation or the WentzelKramersBrillouin (WKB) approximation models to obtain the tunneling probability Γ_{CC} for carriers tunneling to the conduction band at the Schottky contact. For an interface located at 0 and a point at $r > 0$, the expression for the net conduction band electron recombination rate due to tunneling to and from the conduction band at point 0^- immediately to the left of the interface is:

$$\begin{aligned} R_{CC}(r) - G_{CC}(r) = \Theta\left[\epsilon - E_C(0^-)\right]\frac{A^*}{qk}\left|\frac{dE_C}{dr}(r)\right|\Theta\left[-\frac{dE_C}{dr}(r)\right]\Gamma_{CC}(r,\epsilon)\times \\ \left[T_n(r)log\left(1 + exp\left[\frac{E_F(r)-\epsilon}{kT_n(r)}\right]\right) - T_n(0^-)log\left(1 + exp\left[\frac{E_F(0^-)-\epsilon}{kT_n(0^-)}\right]\right)\right] \end{aligned} \tag{2.38}$$

where R_{CC} is the recombination rate, G_{CC} is the generation rate, E_C and E_F are the (position-dependent) conduction band edge and electron Fermi energy, $\epsilon = E_C(r)$, Θ is the unit step function, A^* is the effective Richardson constant and T_n is the electron temperature. The current density of electrons that tunnel from the conduction band in the bulk to the conduction band at an interface or a contact is the integral over the recombination rate:

$$J_{CC} = -q\int_{0^+}^{\infty}[R_{CC}(r) - G_{CC}(r)]dr \tag{2.39}$$

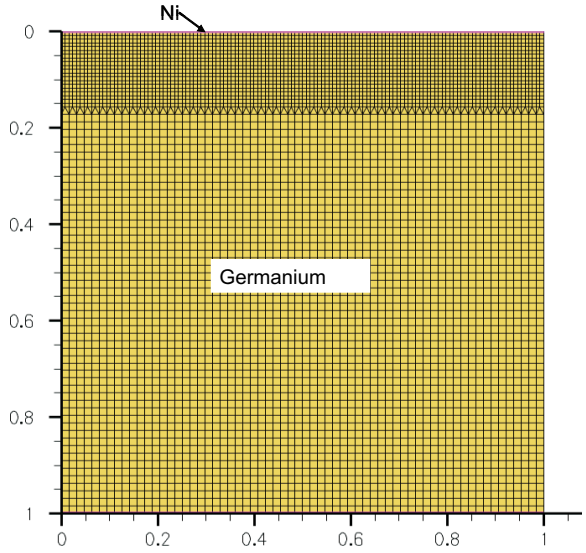

Figure 2.7: An image of the Ni/Ge Schottky barrier mesh.

where 0^+ denotes a position infinitesimally to the right of the interface.

The barrier lowering model due to image force can be applied to a Schottky barrier.The following expression is used to compute the value of the barrier lowering:

$$\Delta\Phi(\mathscr{E}) = a_1[(\frac{\mathscr{E}}{\mathscr{E}_0})^{p_1} - (\frac{\mathscr{E}-\mathscr{E}_{eq}}{\mathscr{E}_0})^{p_1}] + a_2[(\frac{\mathscr{E}}{\mathscr{E}_0})^{p_2} - (\frac{\mathscr{E}-\mathscr{E}_{eq}}{\mathscr{E}_0})^{p_2}] \tag{2.40}$$

where $\mathscr{E}$ is the absolute value of the electric field, $\mathscr{E}_{eq}$ is the equilibrium electric field for zero barrier lowering and $\mathscr{E}_0$ is equal to 1 V/cm, a_1, a_2, p_1 and p_2 are constants.

2.4.3 Schottky barrier simulation

A typical mesh created by using Sentaurus Structure Editor for the Schottky diode simulation is presented in Fig. 2.7. The contact area was 1 μm^2. For accurate calculation of the diode current a very fine mesh of 1 nm^2 was used from the contact to the depletion region edges.

There is no graphical user interface for Sentaurus device for device simulation. For the definition of the transport model, physics model, the file names, the solve procedure, and so on, a script has to be written with a text editor. A typical input file for the Ni/Ge Schottky diode simulation is given below. The file section contains the filenames of the input and the output files. The Anode contact is regarded as the

Ni Schottky contact. In order to account for the Fermi-level pinning effect in Ge the work function of the metal at the contact description was tuned so that a net electron barrier height is obtained by using equation 2.1. A lumped resistance of 10 ohm is added in the cathode elctrode contact to account for any series resistance.

In order to enable the tunneling and the image force lowering effect the options 'eBarrierTunneling' and 'Barrierlowering' were used in the 'Physics' section. Furthermore, in the 'Math' section the 'NonLocal tunneling length' is used to specify the tunneling distance. The parameter 'Digits(Nonlocal)' determines the relative accuracy (the number of valid decimal digits) to which Sentaurus Device computes the tunneling currents.

The 'coupled' command contains the equations to be solved. This command is based on a Newton solver, which is an iterative algorithm in which a linear system is solved at each step simulation. The 'quasistationary' command is used to ramp a device from one solution to another through the modification of its boundary conditions (for example, ramping the voltage at a contact) or parameter values.. The coupled device equations are solved for each new voltage of the sweep. In order to control the ramp, statements for step sizes, initial and the final voltages are given as arguments.

```
File{
   Grid    = "Nige1a_msh.grd"
   Doping  = "Nige1a_msh.dat"
   #This is for the DEVICE with ND=2.9E17 CM-3 AND 1 um square area.
   Plot    = "Nige1a_des4.tdr"
   Current = "Nige1a_des4.plt"
   Param   = "bar.par"
}

Electrode{
   { Name="Anode"    Voltage= 0.0 Schottky Workfunction=4.59 }
   { Name="Cathode"  Voltage= 0.0 Resist=1000 }

}

Physics( Electrode="Anode") {
 Recombination (eBarrierTunneling)
  BarrierLowering
}
```

```
Plot{eCurrent
    ConductionBand ValenceBand
}

Math (Electrode="Anode"){
 Nonlocal(Length=20e-7)
# nonlocal length tunneling length of 20 nm was used.
 Digits(Nonlocal)=3
 EnergyResolution(Nonlocal)=0.001
}

Math {Iterations=30}
Solve {
   NewCurrentFile="init"
   Coupled(Iterations=100){ Poisson }
   Coupled{ Poisson Electron Hole}
   Quasistationary(
      InitialStep=0.01 Increment=1.35
      Minstep=1e-6 MaxStep=0.1
      Goal{ Name="Anode" Voltage=-1 }
   ){ Coupled{ Poisson Electron Hole} }

   NewCurrentFile=""
   Quasistationary(
      InitialStep=0.01 Increment=1.35
      Minstep=1e-6 MaxStep=0.002
      Goal{ Name="Anode" Voltage=1 }
   ){ Coupled{ Poisson Electron Hole}}
}
```

Typical $I - V$ characteristics obtained by numerical simulations of a Ni/Ge Schottky barrier with 1 μm square area are presented in Fig. 2.8 for various Ge doping densities. It is observed that at reverse biases the current increases with increasing voltage for the highly doped Ge. This indicates to the tunneling through the Schottky barrier. This tunneling is relatively low for the medium doped Ge case, and disappears for the lowly doped Ge as expected from the TE and TFE theories. Therefore, Sentaurus Device simulator can successfully and accurately simulate the Schottky behaviour of metal/semiconductor contacts under varying substrate doping densities.

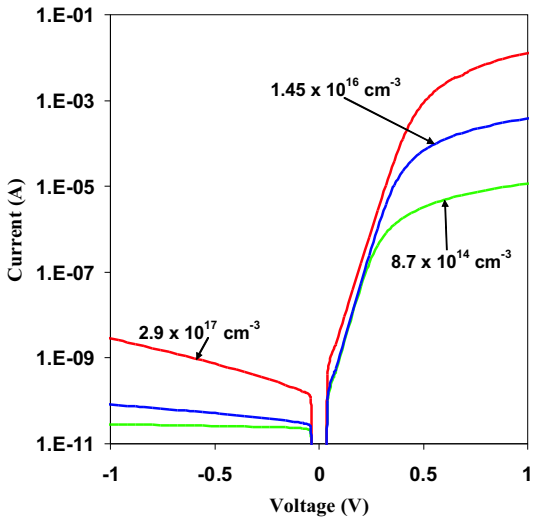

Figure 2.8: Typical $I - V$ curves obtained by numerical simulation of Ni/Ge Schottky barriers for various Ge n-type doping densities.

Chapter 3

Inhomogeneous Ni/Ge Schottky barriers

To achieve high performance Ge nMOSFETs it is necessary to reduce the metal/semiconductor Schottky barrier heights at the source and drain. Ni/Ge and NiGe/Ge Schottky barriers are fabricated by electrodeposition using n-type Ge substrates. I-V and C-V and low temperature I-V measurements are presented. A high-quality Schottky barrier with extremely low reverse leakage current is revealed. The I-V characteristics are shown to fit the thermionic emission model in which Schottky barrier height is described by a Gaussian distribution function. A likely explanation for the distribution of the Schottky barrier height is the spatial variation of the intrinsic states at the Ge surface due to a variation in interfacial oxide thickness, which de-pins the Fermi-level.

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3.1 Introduction

Ge, as a channel material, is one of the key technology boosters to enhance device performance. Ge-based pMOSFETs with doped source/drain show better performance over the Si based devices due to the relatively higher carrier mobility in Ge [22, 23]. However, Ge-based nMOSFETs are lagging behind the Si MOSFETs.

A major obstacle for the Ge based nMOSFETs is the strong Fermi-level pinning of Ge resulting in high Schottky barrier heights for electrons with typical germanides, such as NiGe, TiGe, CoGe. Therefore, to achieve high performance Ge nMOSFETs it is necessary to reduce the Schottky barrier height to the metal or germanide source and drain as much as possible. This reduction of barrier height is hampered by the extreme degree of Fermi-level pinning that takes place at the metal/Ge interface with the Schottky pinning parameter being virtually zero [24]. It has been recently shown that this pinning can be partly prevented by inserting an oxide layer of several nm thickness at the interface between the metal and the semiconductor [25, 26]. Discussion of the barrier height in Si and Ge metal/semiconductor contacts has usually been made assuming spatial uniformity of the barrier height. However, it has been shown experimentally [6, 27] that in case of Si any physical interpretation of the discrepancy of the barrier height as derived from $I - V$ and $C - V$ characteristics as well as the non-Arrhenius behaviour of the temperature dependence can only be explained by assuming a spatially inhomogeneous barrier height. Here, the same analysis is validated in Ni/Ge and by extension NiGe/Ge Schottky barrier contacts and the results are discussed in the light of the potential mechanisms responsible for Fermi-level pinning [28, 29]. This information can be used to purposely adjust the Schottky barrier height at source/drains of nMOSFETs by inserting an ultrathin insulator between the metal and the semiconductor.

3.2 A conventional doped source/drain MOSFET

A basic MOSFET is schematically presented in Fig. 3.1 for a n-type channel formed on p-type semiconductor. The n+ source and drain regions are diffused or implanted into the relatively lightly doped substrate, and a thin oxide layer separates the gate from the substrate. No current flows from drain to source without a conducting channel between them as the drain-substrate-source combination forms oppositely directed p-n junctions in series. When a positive voltage is applied to the gate relative to the substrate(connected to the source for instance), positive charges appear on the gate material whereas negative charges are induced in the underlying semiconductor, forming a depletion region and a thin surface region comprising of

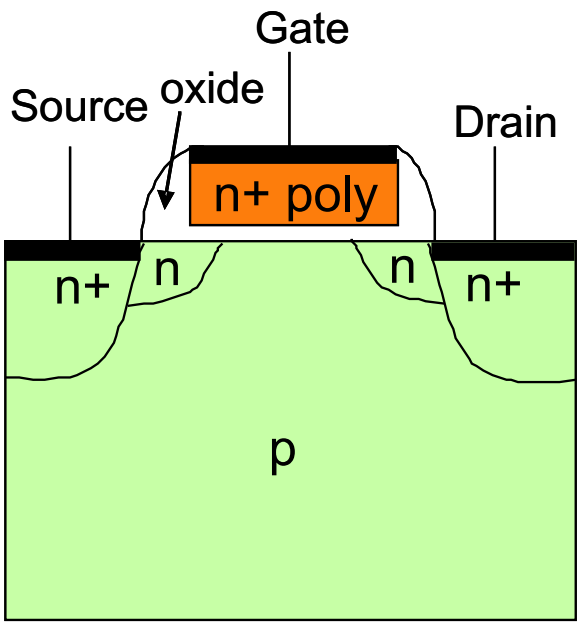

Figure 3.1: A schematic representation of an enhancement type n-channel MOSFET showing the n+ doped drain/source regions with lightly doped n extentions and n+ polysilicon gate.

mobile electrons. These induced electrons form the channel of the device allowing current to flow from drain to source when appropriate bias is applied. The effect of the gate voltage is to vary the conductance of the induced channel. The lightly doped n-type regions decreases the field between the drain and the channel regions thereby reducing injection into the oxide.

The transport equation for a basic MOSFET characteristics is based on the assumptions: 1) an ideal metal-oxide-semiconductor capacitor, 2) current transport is dominated by the drift of carriers, 3) constant mobility in the inversion layer, 4) uniform channel doping, 5) the transverse field is much smaller than the longitudinal field. These assumptions all-together are known as the gradual channel approximation. As shown in textbooks [1] in the ON state the transport equation yields:

$$I_{DS} = \frac{W}{L}\mu_n C_{ox}[(V_{GS} - V_T)V_{DS} - {V_{DS}}^2] \tag{3.1}$$

at $|V_{DS}| < |V_{GS}| - |V_T|$, where, W/L is the aspect ratio of the device, C_{ox} is the oxide capacitance, V_{GS} is the gate voltage with respect to source, V_{DS} is the drain voltage with respect to source and V_T is the threshold voltage. Pinch-off and saturation occurs when $|V_{DS}| = |V_{GS}| - |V_T|$ and $|V_{DS}| > |V_{GS}| - |V_T|$ respectively and the drain

current reduces to

$$I_{DS} = \frac{W}{L}\mu C_{ox}(V_{GS} - V_T)^2 \tag{3.2}$$

These equations predict zero current when $|V_{GS}| < |V_T|$. In the off-state, however, diffusion is the dominant transport mechanism in the channel. The sub-threshold current can be shown to be [1]:

$$I_{sub} \propto [1 - exp[\frac{-qV_{DS}}{kT}]]exp(\frac{q\psi_s}{kT}) \tag{3.3}$$

where ψ_s is the surface potential and is approximately $V_{GS} - V_T$. I_{sub} is independent of V_{DS} for $V_{DS} > 3kT/q$. Ideally, the sub-threshold current is very small and then increases rapidly at turn on. One measure of this is the sub-threshold swing. The ideal sub-threshold swing at room temperature is 60 meV/decade.

The goal of MOSFET scaling is to obtain faster devices with higher drive currents, while still maintaining the ideal device characteristics mentioned above. There are various sets of scaling rules [1] that can be applied to MOSFET design parameters when reducing the dimensions of an established process. Such rules can approach fundamental limits, for example, the gate oxide cannot be made much thinner than $\sim 15\mathring{A}$ because of substantial gate leakage into the channel. The source/drain technology is an important concern of scaled MOSFETs. For ultra-scaled MOSFETs, metal source/drain junction will be required for reducing parasitic resistances. Thus, the Schottky barrier height control at the metal/semiconductor interface is indispensable for achieving high performance MOSFETs. In order to achieve high performance i.e. high drive current and high speed from MOSFETs a silicide layer is usually formed at the gate, source and drain electrode terminals. Silicidation is usually done by annealing a metal/silicon junction at high temperatures in an inert atmosphere. The choice of metal silicides in Si technology meets the basic requirements: low specific resistivity, low contact resistivity to both types of Si, high thermal stability, good processibility, and excellent process compatibility with standard Si technology.

3.3 Fermi-level pinning by metal-induced gap states

According to the model of Heine [15], when a metal/semiconductor contact is made, the wave functions of the electrons in the metal decay into the semiconductor

in the energy range where the conduction band of the metal overlaps the semiconductor band gap. This results in states in the forbidden gap, which are known as metal-induced gap states (MIGS). The formation of MIGS in the band gap of the semiconductor means that a metallic phase appears in the semiconductor. Therefore, when a metal and a semiconductor contact, the chemical potential of this metallic phase in the semiconductor would agree with that of the metal. In other words, MIGS determine the band alignment at the semiconductor/metal interface and Schottky barrier height [30]. The mechanism of band alignment is shown in Fig. 3.2.

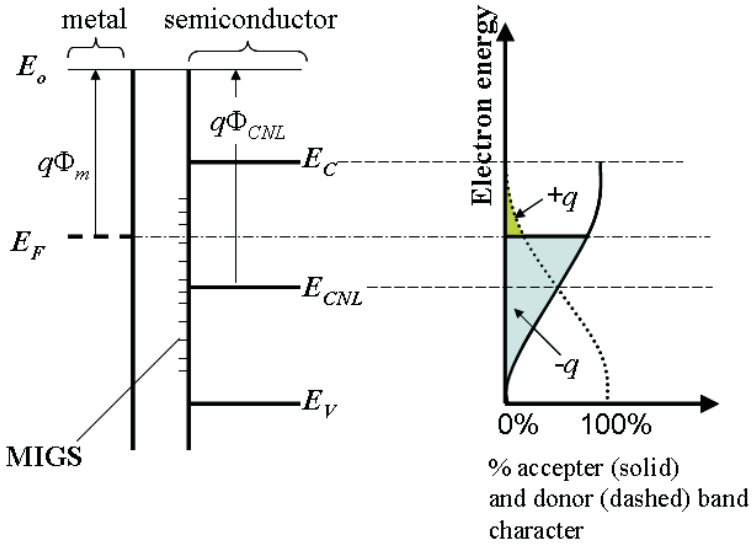

Figure 3.2: Energy band diagram (left) of a metal/semiconductor contact showing MIGS and the charge neutrality level E_{CNL} schematically. $q\Phi_{CNL}$ is the energy difference between E_{CNL} and E_o. The charging characteristics (right) of the MIGS are also presented (redrawn from Ref. [31]).

MIGS are donor-like close to the valence band and acceptor-like near the conduction band. The energy level in the band gap at which the dominant character of the interface charges changes from donor-like to acceptor-like is called the charge neutrality level (E_{CNL}). Charge transfer generally occurs across the interface due to the presence of intrinsic interface states. Filling an acceptor-like interface state results in a negative charge, while leaving a donor-like interface state empty results in a positive charge. Therefore, charging of these states creates a dipole that tends to drive the band line-up toward a position that would give zero dipole charge. Fig. 3.2 shows the case where the metal Fermi-level E_F is above E_{CNL} in the semiconductor,

creating a dipole that is negatively charged on the semiconductor side. This interface dipole drives the band alignment so that E_F goes toward E_{CNL}.

A parameter that determines the the Fermi-level pinning at various semiconductors is known as the pinning factor S, given by:

$$S = \frac{\delta\phi_n}{\delta\Phi_m} \tag{3.4}$$

This factor determines how much ϕ_n can be modulated by changing the metal workfunction. The various S factors for a variety of materials [31] are presented in Fig. 3.3a. This pinning factor is found to follow the emipirical model developed by Monch [32] and is given by:

$$S^{-1} - 1 = 0.1\,(\epsilon_\infty - 1)^2 \tag{3.5}$$

where ϵ_∞ is the electronic component of dielectric constant. Materials with a smaller S tend to pin the Fermi-level more effectively to E_{CNL}, as presented in Fig. 3.3b.

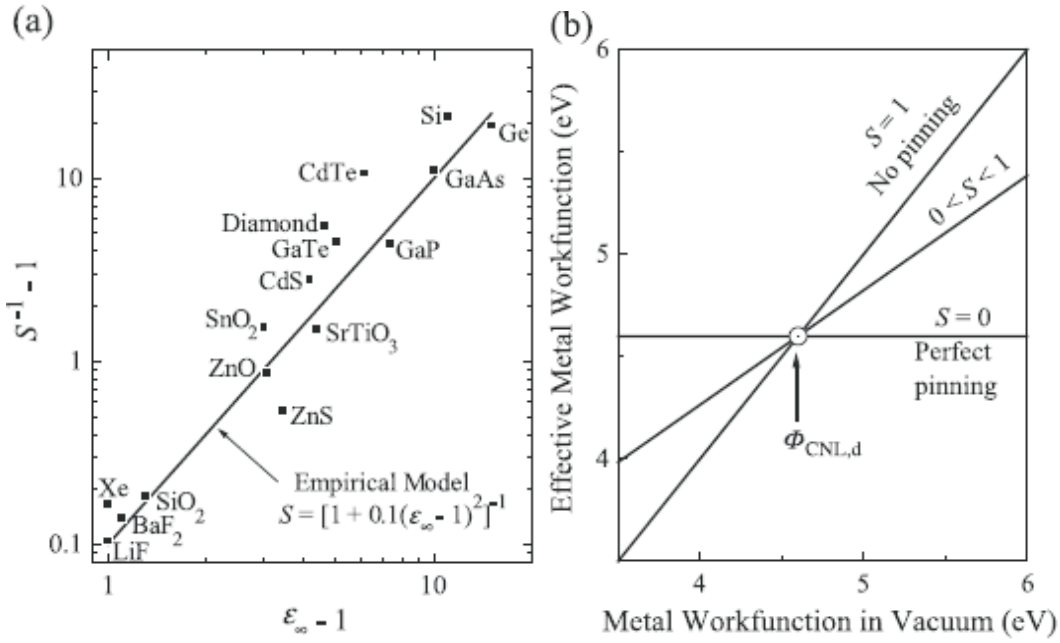

Figure 3.3: (a) Variation of the slope parameter S with electronic dielectric constant ϵ_∞ of the semiconductor. The empirical model is also shown. Materials with large ϵ_∞ have small S. (b) A smaller S leads to a higher degree of pinning of the metal Fermi-level to the charge neutrality level E_{CNL} (reproduced from Ref. [31]).

The maximum value of S is unity that corresponds to no pinning of the metal Fermi-level. Experimentally the value of S was found to be 0.02 and 0.27 for Ge and

Si, respectively. This resulted in observations [33] that Schottky barriers formed on Ge are very little dependent on Φ_m of the electrode metal while those formed on Si vary in proportion to the metal work function as presented in Fig. 3.4.

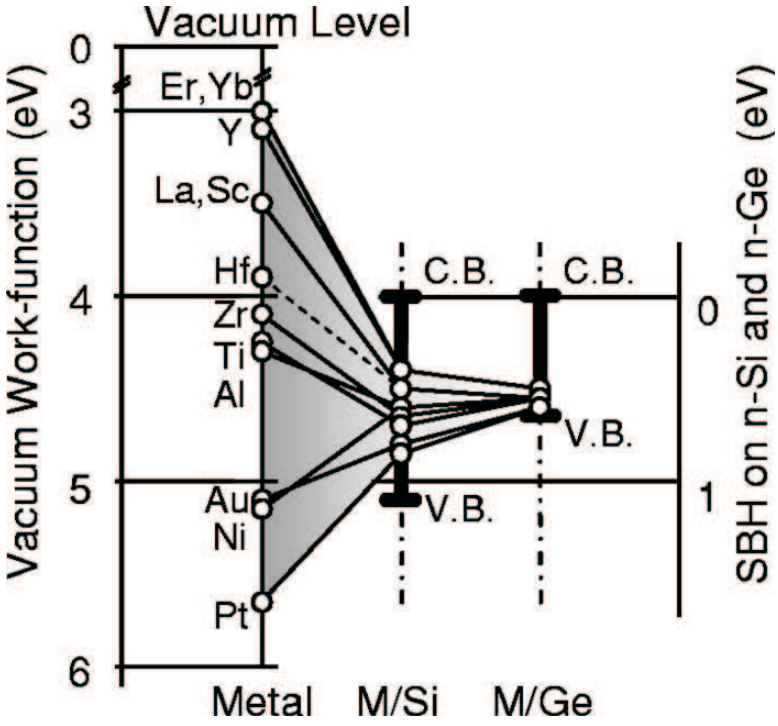

Figure 3.4: Experimentally obtained Schottky barrier heights on nSi and nGe and reported metal work functions showing the effect of Fermi-level pinning on Si and Ge (reproduced from Ref. [33]).

The technology for mitigating Fermi-level pinning by MIGS was proposed by Kobayashi *et al.* [24]. The main concept is illustrated in Fig. 3.5. The free-electron wavefunction penetrates into the semiconductor, which generates MIGS and pins the Fermi-level. Since Ge has smaller bandgap and higher dielectric constant than Si, the strong Fermi-level pinning occurs near E_{CNL} which is close to the valence band. An ultrathin insulator inserted between metal/Ge interface blocks the free state penetration into Ge and equivalently reduces MIGS density. As a result, Fermi-level pinning is released and effective barrier height becomes low.

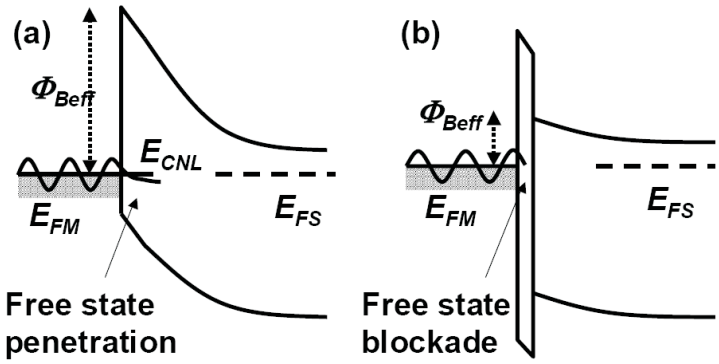

Figure 3.5: Schematic band diagram of (a) metal/Ge junction, where free electron wavefunction penetrates into Ge and (b) metal/insulator/Ge junction, where free electron wavefunction penetration is blocked (reproduced from Ref. [24]).

3.4 Experimental procedure

For the fabrication of Ni/Ge Schottky barriers, Sb-doped Ge (100) wafers were taken as the starting wafers. Square patterns of sizes from 20 to 400 μm square were transferred to the photoresist-coated substrates by conventional lithography. The back ohmic contacts were defined by Au-Sb evaporation and annealing the samples in an $H_2(2\%)/N_2$ inert atmosphere.

Buffered Hydrofluoric acid (HF) pretreatment on Ge immediately before electrodeposition is a very critical step of the fabrication method presented here. This is because the native oxide on the Ge surface disturbs the Ni nucleation on Ge and should be removed before electrodeposition. In this experiment a 20:1 buffered HF dip for 30 seconds was performed to remove any native oxide from Ge. This was followed by de-ionised water wash to remove the HF from the samples. The HF treatment was done several times immediately prior to electrodeposition of Ni.

For electrodeposition, a Ni-sulphate bath and an Autolab AUT72032 potentiostat three electrode system with a Pt counter electrode and a saturated calomel reference electrode were used. A Ni-sulphate aqueous solution was prepared using a recipe presented in Table 3.1. Among the constituents, Ni-sulphate provides the Ni-ions for deposition, whereas, boric acid controls the pH value and acts as a weak buffer for the solution. Sodium dodecyl sulphate improves the wettability of the electrolyte to the semiconductor surface.

Ingredient	Quantity (mol dm^{-3})
Ni-sulphate	0.1
Boric Acid	0.1
Sodium dodecyl sulphate	0.005

Table 3.1: Composition of the solution used for Ni electrodeposition [34].

In order to determine an optimum deposition potential for Ni deposition on Ge, a cyclic voltammogram was initially obtained for the Ge substrates. Typical cyclic voltammograms of Ni electrodeposition on Ge having nominal resistivities of 2-2.4 Ω-cm, 0.13-0.15 Ω-cm and 0.005-0.02 Ω-cm are presented in Fig. 3.6.

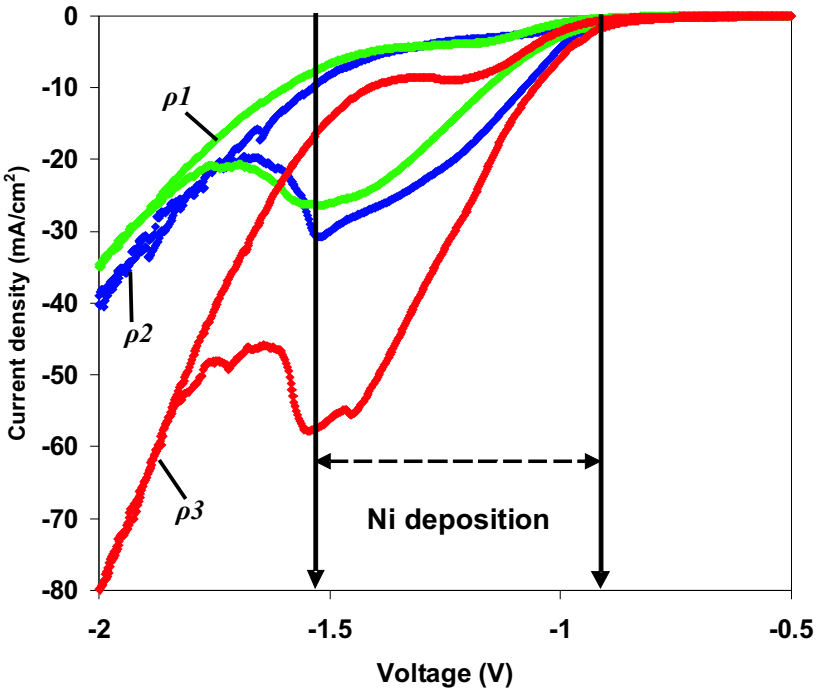

Figure 3.6: Cyclic voltammogram of Ni electrodeposition on Ge with resistivity of ρ1=2-2.4 Ω-cm, ρ2=0.13-0.15 Ω-cm and ρ3=0.005-0.02 Ω-cm. Ni deposition takes place at voltage ranges from -0.9 to -1.55 Volts. (This experiment was partly done by Xiaoli V. Li).

As the applied potential is increased, there is no electrodeposition current until a certain threshold potential near -0.9 Volts. Beyond that threshold the potential is high enough to cause Ni nucleation and electrodeposition on Ge. This threshold potential

for Ni deposition does not depend on the substrate resistivity as observed in Fig. 3.6. This is because at lower voltages, before nucleation begins there is practically no current flowing and hence, there is no voltage drop along the electrode. As nucleation continues, more and more sites of the substrate become active with increasing bias and the current increases. The increased substrate resistivity reduces the electrodeposition current. Thus, electrodeposition is taking place at a lower rate on high resistivity substrates. For the various substrates, the cathodic current was dominated by Ni deposition between -0.9 and -1.55 Volts, (between the arrows in Fig. 3.6). Therefore, the deposition potential could be within this region. For Ni electrodeposition on the photoresist patterned Ge substrates, the deposition potential ranged between -1.10 to -1.15 Volts was chosen that resulted in a smooth, continuous Ni film. An SEM image of a typical Ni film grown by electrodeposition on Ge (0.005-0.02 Ω-cm) substrate is shown in Fig. 3.7.

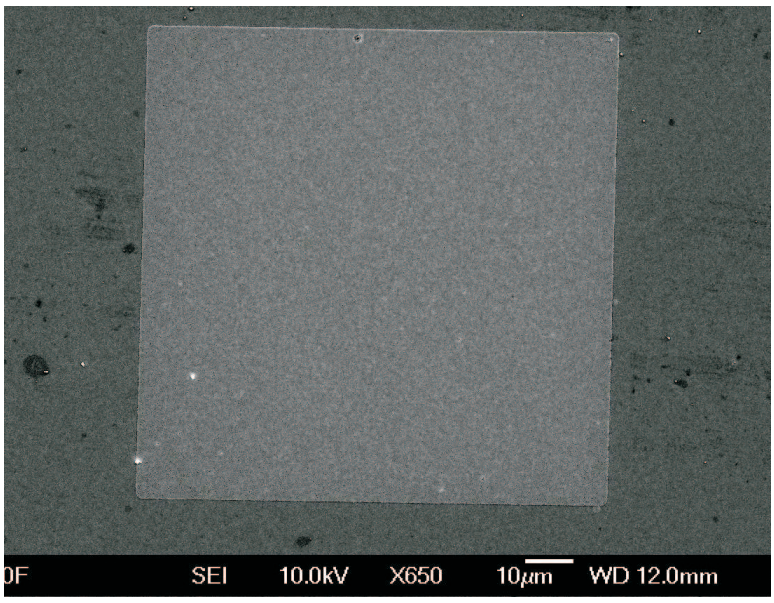

Figure 3.7: An SEM image of a typical electrodeposited Ni film.

The Ni film thickness was controlled by measuring the charge accumulating at the cathode during electrodeposition and using the equation presented in section 2.3.2. Schottky barriers with Ni layer thicknesses from 70 nm to 200 nm were fabricated. $I-V$ and $C-V$ characteristics measurements were performed using a Hewlett Packard 4155C semiconductor parameter analyzer and a Hewlett Packard

4280A, 1 MHz, capacitance Meter/$(C - V)$ plotter, respectively. The low temperature measurements were performed using a Bio-Rad DL 4960 cryostat temperature controller that enables a temperature variation from 1.5 K to room temperature. Germanidation of the Ni films was performed for 20 min in the anneal chamber at temperatures ranging from 300 to 500 °C. X-ray diffraction (XRD) and SEM scanning were performed using a Siemens D5000 X-ray Diffractometer and a LEO 1455VP SEM, respectively. More details on the experimental processes including SEM images and X-ray graphs, and metal sheet resistance can be found in Chapter 4.

3.5 Results and discussions

3.5.1 Electrical characteristics

In Fig. 3.8, $J - V$ characteristics of Ni/nGe (lowly doped, 2-2.4 Ω-cm), Ni/n+Ge (highly doped, 0.005-0.02 Ω-cm), and Nige/n+Ge (highly doped) Schottky barriers are shown. Ni film thicknesses were 70 nm where as the NiGe film thickness was 185 nm. The contact areas of the Schottky barriers on the lowly doped and highly doped Ge are 400μm and 20 μm square, respectively. The reverse leakage matches the saturation current density and has a low field dependence. Breakdown of the diodes was not observed up to -3 Volts bias, indicating that edge effects are suppressed as explained in Ref. [35].

Using the Richardson constant value for free electrons ($A^* = 50$ A cm^{-2} K^{-2} [36, 37]), electron Schottky barrier heights ϕ_n in the range of 0.52-0.55 eV were obtained for all three devices by fitting the TE model in the low forward bias region (0.08-0.2 Volts). The ideality factor η and the series resistances R_S are also extracted. These are summarised in Table 3.2. For varying metal film thicknesses, no variation in the Schottky barrier parameters was observed. The standard deviation of ϕ_n and η are obtained from extracted values of different devices grown under the same electrodeposition potential (-1.10 Volts against the reference electrode potential).

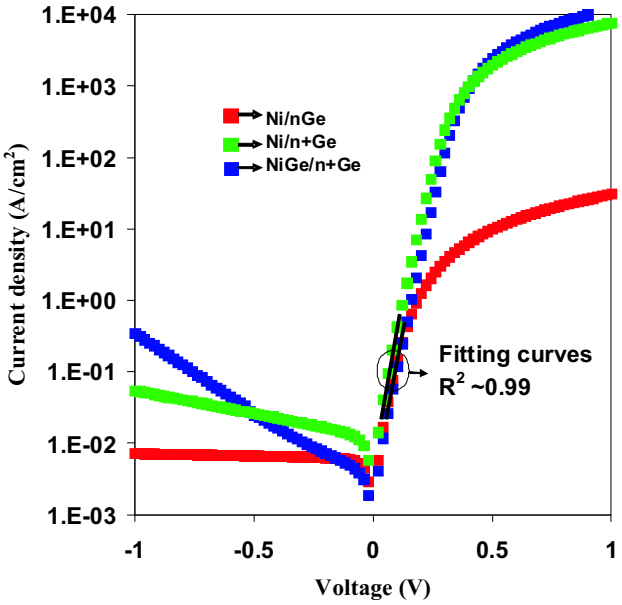

Figure 3.8: $J-V$ characteristics of electrodeposited Ni/Ge and NiGe/Ge Schottky barriers for different Ge doping concentrations clearly demonstrating the effect of Fermi-level pinning. nGe and n+Ge has resistivities of 2-2.4 Ω-cm and 0.005-0.02 Ω-cm, respectively. The TE model was fitted in the voltage range of 0.08-0.2 Volts to extract Schottky barrier parameters.

Device	ϕ_n (eV)	η	$R_S(\Omega)$
Ni/nGe (8 devices)	0.53 ± 0.01	1.18 ± 0.01	12.40
Ni/n$^+$Ge (8 devices)	0.52 ± 0.01	1.10 ± 0.02	21.32
NiGe/n$^+$Ge (6 devices)	0.55 ± 0.01	1.08 ± 0.03	10.85

Table 3.2: Extracted parameters of the Ni/nGe, Ni/n+Ge and NiGe/n+Ge Schottky barriers showing the variation of ϕ_n and η of different devices grown by using the same electrodeposition potential and annealing conditions.

It can be inferred that the Fermi-level pinning is as strong in an electrodeposited Ni/Ge Schottky barriers as it is in an annealed NiGe/Ge Schottky barriers suggesting that intrinsic effects are responsible for the Fermi-level pinning. The reliability of the results obtained here are verified in Fig. 3.9 and Fig. 3.10 where $J - V$ characteristics of Schottky barriers of different square-contact areas are shown for Ge resistivities of 2-2.4 Ω-cm and 0.005-0.02 Ω-cm, respectively. In low forward bias region, the overlap of the $J - V$ curves in both Fig. 3.9 and Fig. 3.10 indicates to the Fermi-pinning of the various Schottky barriers.

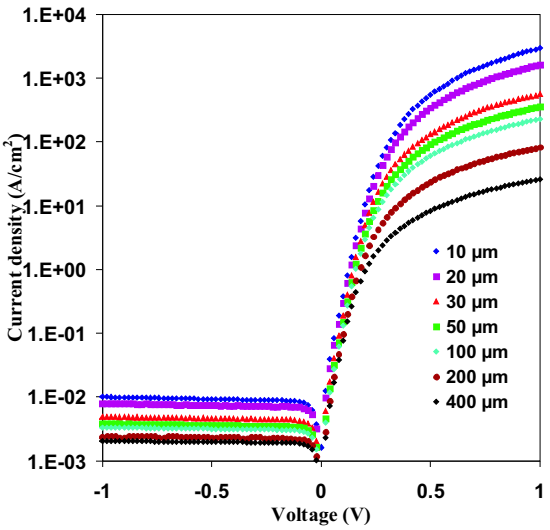

Figure 3.9: $J - V$ characteristics of electrodeposited Ni/Ge Schottky barriers having square contacts of various sizes showing the overlap of J in the low forward bias region indicating Fermi-level pinning. The substrate resistivity was 2-2.4 Ω-cm.

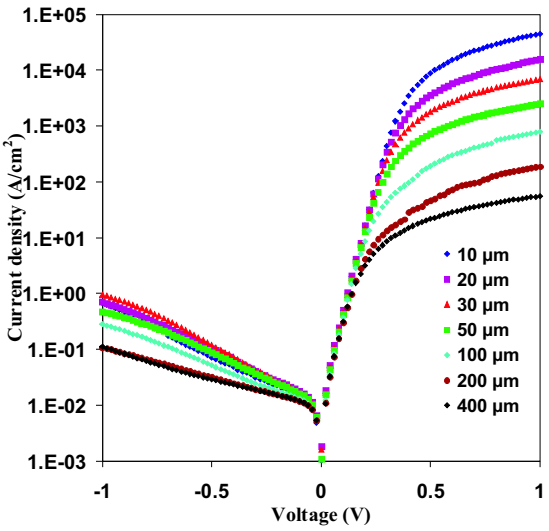

Figure 3.10: $J - V$ characteristics of electrodeposited Ni/Ge Schottky barriers having square contacts of various sizes showing the overlap of J in the low forward bias region indicating Fermi-level pinning. The substrate resistivity was 0.005-0.02 Ω-cm.

A detailed characterisation of the electrodeposited Ni/Ge Schottky barrier was performed. Low doped nGe substrates were used in the following analysis to eliminate tunneling effects and allow for a description of the Schottky barriers by TE theory only. Low temperature $I - V$ measurements were performed for the Ni/nGe devices. The range was from 50 K to 300 K, with steps of 10 K. For reproducibility of measured characteristics, investigations were performed on sample #1 and sample #2, where Ni/Ge Schottky barriers were fabricated using the same electrodeposition potential (-1.10 Volts against the reference electrode). The forward bias characteristics of a Ni/nGe device in sample #1 are shown in Fig. 3.11. For clarity, $I - V$ curves of only 9 different temperatures are plotted in this diagram. As expected from the TE theory, the saturation current I_S is reduced drastically with temperature. The reverse leakage current is also reduced following I_S (shown in Fig. 3.12). Below 120 K, the reverse leakage is lower than 100 pA, which is the lower current limit of the measurement setup that has been used.

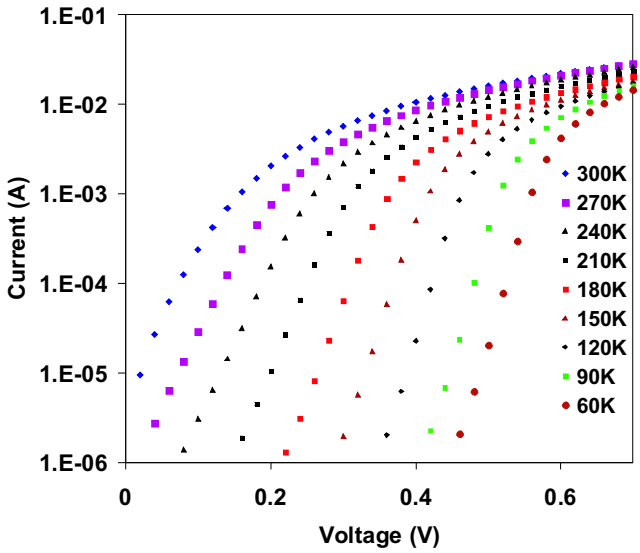

Figure 3.11: Low temperature, forward bias $I - V$ characteristics of a Ni/Ge Schottky barrier with a contact area of 400 μm square fabricated on sample #1. The substrate resistivity was 2-2.4 Ω-cm.

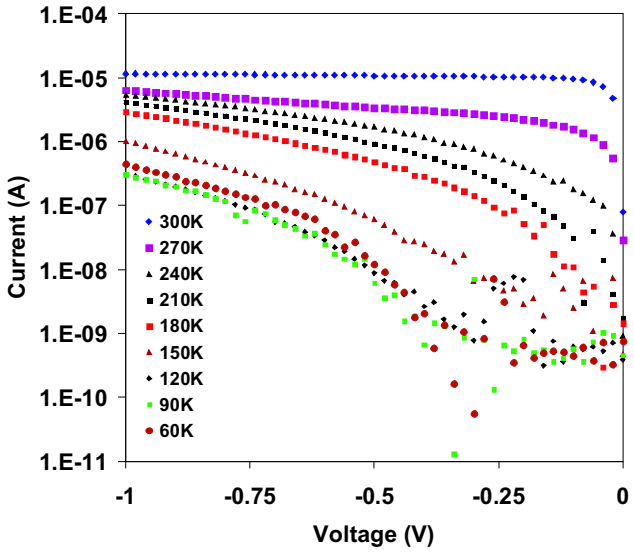

Figure 3.12: Low temperature, reverse bias $I - V$ characteristics of a Ni/Ge Schottky barrier with a contact area of 400 μm square fabricated on sample #1. The substrate resistivity was 2-2.4 Ω-cm.

The forward bias characteristics of a Ni/nGe device in sample #2 are shown in Fig. 3.13. The saturation current I_S is reduced drastically with temperature similar to what happened for the Schottky barrier in sample #1. The reverse leakage current also reduced with temperature following I_S (shown in Fig. 3.14).

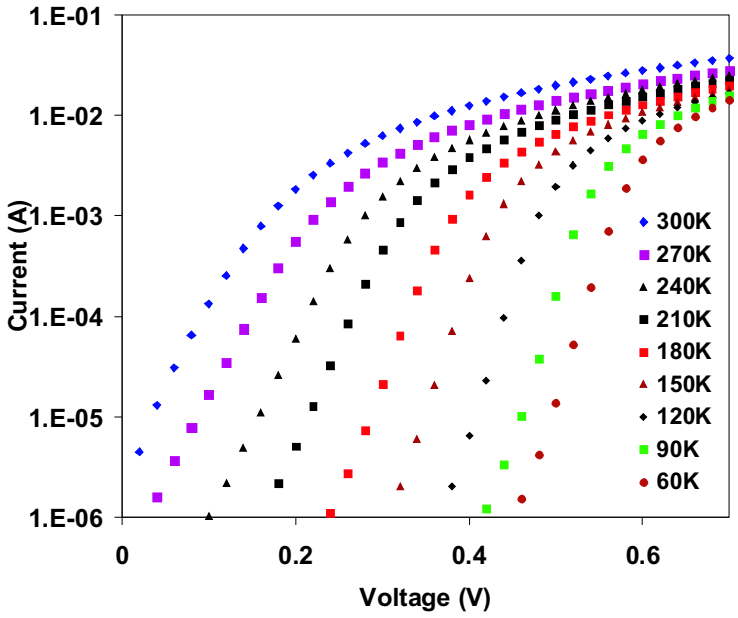

Figure 3.13: Low temperature, forward bias $I - V$ characteristics of a Ni/Ge Schottky barrier with a contact area of 400 μm square fabricated on sample #2. The substrate resistivity was 2-2.4 Ω-cm.

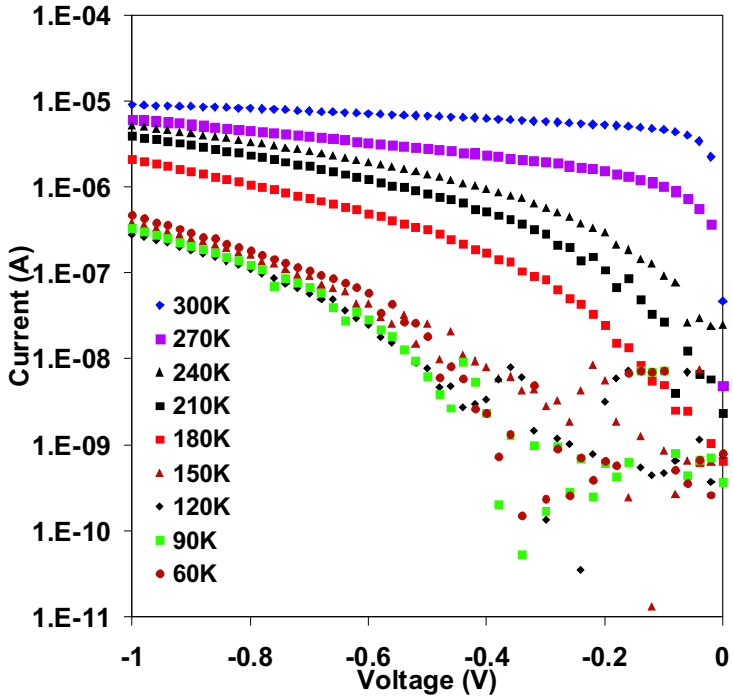

Figure 3.14: Low temperature, reverse bias $I - V$ characteristics of a Ni/Ge Schottky barrier with a contact area of 400 μm square fabricated on sample #2. The substrate resistivity was 2-2.4 Ω-cm.

The saturation current density the Ni/Ge Schottky barrier in sample #1 were extrapolated from the $I - V$ measurements for different temperatures by fitting the TE model in the low forward bias region in the current range of 1×10^{-4} - 1×10^{-5} A, and the data were plotted in an activation energy diagram as shown in Fig. 3.15. A temperature independent Schottky barrier height would result in a straight line on the activation energy diagram. A fit with $\phi_n = 0.53$ eV is shown as a solid line in Fig. 3.15. This line fits only the high temperature experimental results. For lower temperatures, a deviation from a straight line is observed, indicating a temperature dependent Schottky barrier height.

3.5.2 Inhomogeneity of Schottky barrier

Several models have been proposed to explain the low temperature behaviour of Schottky barriers [38]. In order to model the temperature dependence of Schottky barrier heights, the so-called T_0 effect is often used [39]. However, it lacks a direct

physical explanation [6]. A model that physically justifies the temperature dependence of Schottky barriers is that proposed by Werner and Guttler [40]. This model assumes a spatial distributions of the barrier height expressed by a Gaussian function. The barrier height influences capacitance and DC measurements differently. The capacitance stems from the displacement current, which depends on the mean electric field at the metal/semiconductor interface. Short-wavelength potential fluctuations at the metal/semiconductor interface are screened out at the edge of the space-charge region. Consequently, capacitance measurements reflect the mean value of the barrier height. On the other hand, the current across the interface depends exponentially on the barrier height and thus sensitively on the detailed barrier distribution at the interface. Any spatial variation in the barrier causes the current to flow preferentially through the barrier minima. A quantitative expression for the effective barrier height is given by the following equations:

$$J(V) = A^* T^2 e^{-\frac{q\phi_n}{kT}} \left(e^{\frac{qV}{kT}} - 1 \right) \tag{3.6}$$

$$\phi_n = \overline{\phi_n} - \frac{q{\sigma_s}^2}{2kT} \tag{3.7}$$

with $\overline{\phi_n}$ and σ_s being the mean value and the standard deviation of the spatial Schottky barrier height distribution, respectively.

As discussed, if the spatial distribution is on a length scale less than the space charge width, then $\overline{\phi_n}$ should match the Schottky barrier height obtained by $C-V$ measurements. In order to fit the experimental results with this model, the Schottky barrier height value from $C-V$ measurements was used, leaving the standard deviation as the only fit parameter. Please refer to the *C-V* measurements of Schottky barriers on low doped Ge. Using this A^*-independent measurement technique, the Schottky barrier height was calculated to be 0.569 eV. Again, a value of 50 A cm^{-2} K^{-2} for the Richardson constant is used. The resulting fit, using a standard deviation of 52 meV, is shown in Fig. 3.15. An excellent fit is obtained throughout the range of measurements. The value of the standard deviation of the barrier height is in good agreement with ballistic electron emission microscopy values on Au/Si [41]. The ideality factor which in most other models is just a fitting factor follows logically from this interpretation as well as outlined in Ref. [6,27]. These results hence indicate

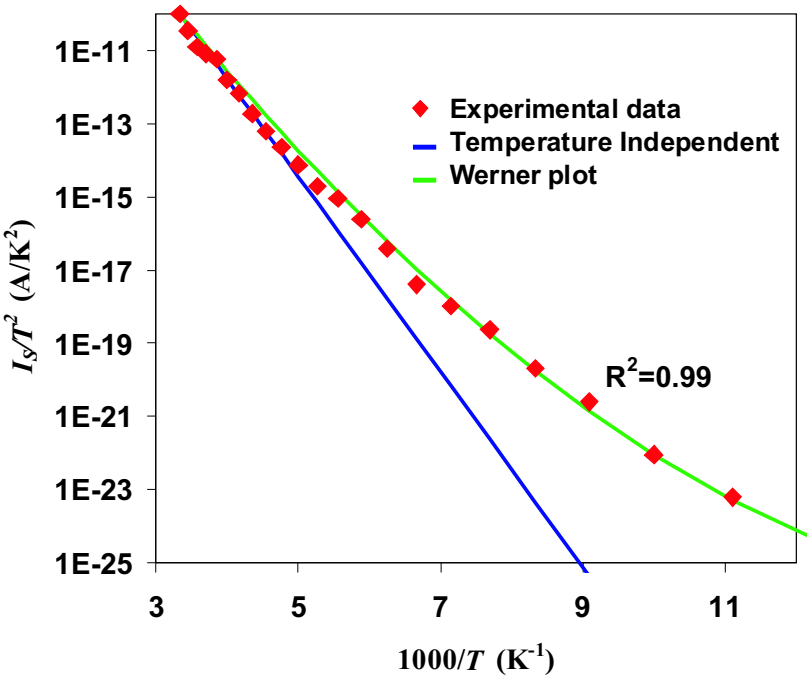

Figure 3.15: Activation energy diagram (Arrhenius plot) of the same electrodeposited Ni/Ge contact as in Fig. 3.11 (sample #1). The measurements are fitted using a temperature-independent thermionic emission model (ϕ_n = 0.53 eV) and the model of Werner and Guttler [40] (ϕ_n = 0.57 eV and σ_s= 52 meV).

that the inhomogeneous Schottky barrier model is an accurate description for Ni/Ge Schottky barriers and that its use is valid.

By using a similar approach for exprapolating the saturation current density for the Ni/nGe Schottky barrier in sample #2, a non-Arrhenius behaviour of temperature dependence is observed in Fig. 3.16. The experimental results were fitted using the Werners model with a mean ϕ_n of 0.57 eV and a standard deviation of 48 meV. These results confirm the reproducibility of the observed spatial variation of the Ni/nGe Schottky barriers.

The physical origin of the inhomogeneity of the Schottky barriers is open to interpretation. It can be argued that the polycrystalline nature of Ni at a Schottky interface results in a variation in the metal work function. However, the strong Fermi-level pinning strongly reduces the importance of the metal work function and the X-ray diffraction measurements only show (please refer to Chapter 4) the evidence of Ni(111) peak, this explanation is hence not satisfactory. If one assumes that MIGS

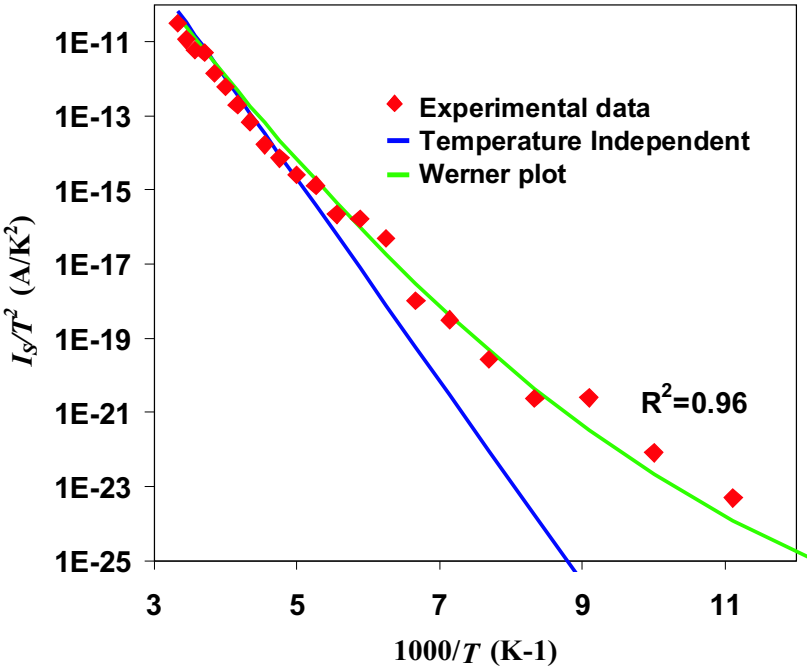

Figure 3.16: Activation energy diagram (Arrhenius plot) of the Ni/nGe Schottky barrier as in Fig. 3.13 (sample #2). The measurements are fitted using a temperature-independent thermionic emission model ($\phi_n = 0.54$ eV) and the model of Werner and Guttler [40] ($\phi_n = 0.57$ eV and σ_s= 48 meV).

at the semiconductor surface determine the barrier height, the inhomogeneity of the Schottky barriers must be due to the spatial variation of the MIGS. This variation might be due to the presence of a very thin oxide layer between the semiconductor and the metal. As shown in Ref. [26] a 0.6 nm thin GeO_x layer between Al and nGe reduces the barrier height by 40 meV. Although no oxide was grown intentionally, it is likely that some GeO_x would indeed have formed on the Ge surface before Ni deposition. A local variation (non-Gaussian) in this oxide thickness of the order of 0.5 nm would hence be consistent with the experimental data. It also suggests that for Fermi-level de-pinning a non-uniform oxide layer might actually be more beneficial than a uniform layer.

3.6 Conclusions

Fermi-levels at any metal/Ge interfaces are pinned near the valence band edge of Ge due to the existence of MIGS. Schottky barrier heights of metals with Ge are hence independent of the metal work functions. The Fermi-level pinning, however, could be overcome using a thin oxide layer at the metal/Ge interface. Electrodeposited Ni on Ge form very high quality Schottky barriers with high rectification and extremely low leakage currents. The barrier heights are spatially varying which results in a non-Arrhenius behaviour of temperature dependence. This temperature dependence of Schottky barrier heights is well fitted with Werner and Guttler's model who assumed a spatial distribution of the barrier heights expressed by a Gaussian function. A physical explanation of the spatial variation of the Schottky barrier heights could be attributed to the existence of a spatially varying thin oxide layer at the metal/Ge interface that results in a spatially varying pinning of the Fermi-level. Maintaining an adequate tunneling probability through the oxide layer is critical to obtain a low resistance metal/semiconductor junction in the source/drain of MOSFETs. Therefore, for Fermi-level de-pinning a non-uniform oxide layer might actually be more beneficial than a uniform layer. The information found from the experiments in this Chapter hence could be used to purposely adjust the Schottky barrier height at the source/drains of Ge based nMOSFETs by inserting a non-uniform ultrathin insulator between the metal and Ge interface.

Chapter 4

NiGe/Ge contacts for Schottky barrier MOSFETs

Ge channel SB-MOSFETs suffer from high drain/body leakage at the required elevated substrate doping concentrations to suppress source-drain leakage. Electrodeposited Ni/Ge and NiGe/Ge Schottky barriers on highly doped Ge show low off current, which might make them suitable for SB-pMOSFETs. The fabricated Schottky barriers showed rectification of up to 5 orders in magnitude. At low forward biases the overlap of the forward current density curves for the as deposited Ni/nGe and NiGe/nGe Schottky barriers indicates Fermi-level pinning in the Ge band gap. The Schottky barrier height for electrons remains virtually constant at ∼0.52 eV (indicating a hole barrier height of 0.14 eV) under various annealing temperatures. The series resistance decreases with increasing annealing temperature in agreement with four point probe measurements indicating the lower specific resistance of NiGe as compared to Ni, which is crucial for high drive current in SB-pMOSFETs. Numerical simulation reveals that by incorporating such high quality Schottky barriers in the source/drain of a Ge channel pMOSFET, highly doped substrate could be used to minimise the subthreshold source to drain leakage current.

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4.1 Introduction

Ge channel MOSFETs are considered as promising devices for future high-speed complementary metal-oxide-semiconductor (CMOS) technology as they offer high carrier mobilities suitable for large drive current. Schottky barrier source/drain MOSFETs overcome the problems faced by the conventional transistor scaling caused by the stringent conditions required for doping with low series resistance [42–44]. The Ge based SB-pMOSFETs, however, suffer from increased leakage currents due to its narrow bandgap and low Schottky barrier height [45–47]. Ni/Si Schottky barriers prepared by electrodeposition exhibit superior properties to physical vapour deposition prepared diodes [5, 6]. The work presented in this chapter reveals that electrodeposited Ni/Ge and NiGe/Ge Schottky barriers formed on highly doped Ge exhibit near ideal Schottky behaviour with low reverse leakage current. The experimental data of the diodes are used to calibrate numerical simulations of the Ge channel SB-MOSFET. At short channel lengths SB-MOSFETs suffer from source to drain leakage currents. Simulation results are presented to show that a highly doped Ge substrate is the key to limiting subthreshold source to drain leakage currents. The low off current of the electrodeposited Schottky barriers on highly doped substrate might make this possible without increasing junction leakage current at the drain/body of SB-pMOSFETs.

4.2 The Schottky barrier MOSFET

The source and drain of an SB-MOSFET are different from a conventional MOSFET in that they consist only of metal silicide contacts replacing the doped regions as shown in Fig. 4.1. SB-MOSFETs can operate either as n-type or p-type transistors, however, in this research only pMOSFET operation is considered because the small p-type barrier height allows higher drive current and the n-type Ge wafer prevents leakage into the substrate.

With the down-scaling of transistor gate length, the junction depth of source/drain extensions must be scaled down in order to suppress short channel effects. For conventional MOSFETs, the formation of ultra-shallow junctions requires ultra-low energy ion implantation and dopant diffusion caused by high temperature annealing must

be avoided in order to get a high scalability and a low resistance of the source/drain extensions. This is a major challenge for current processing technology. In contrast, the structure of SB-MOSFETs as shown in Fig. 4.1 is composed of a silicide source and drain. This means that Schottky contacts replace the p-n junctions. Compared to a p-n diode, a Schottky diode exhibits a larger leakage and it may be rather difficult to fabricate reproducibly since the Schottky barrier height is very sensitive to small process fluctuations [5, 48]. However, this unique change in structure offers many advantages. The ultra-shallow junction can be formed easily and accurately, since the silicide junction depth is controlled by the deposited metal thickness and the thermal budget, yielding a high potential scalability. As can be found in the experiments in this thesis the silicides/germanides have a very low sheet resistance as opposed to highly doped source/drain extensions. Low thermal budget and simple processing allows the integration of a high-k gate insulator and a metal-gate.

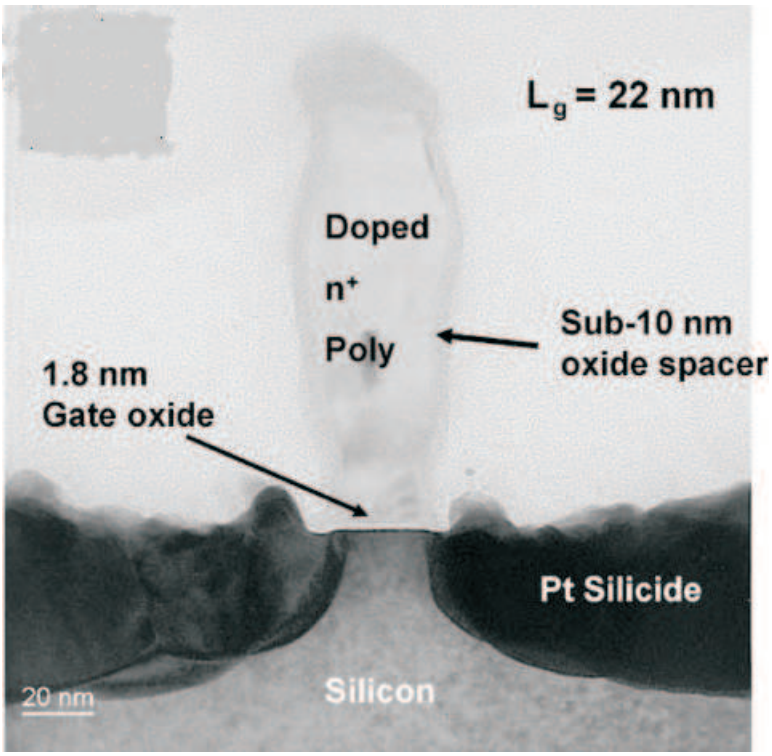

Figure 4.1: Cross-sectional tunneling electron microscope image of a 22 nm gate length SB-MOSFET (reproduced from Ref. [45]).

The basic operating principles of an SB-pMOSFET are illustrated in Fig. 4.2. The Fermi-level pinning at the metal semiconductor interface is assumed as is appropriate

for materials such as NiGe. The Ge channel is considered as being highly doped. Without external voltage, the energy band diagram is in equilibrium and the band bending is very steep due to the Ge doping as shown in Fig. 4.2a. By application of a drain voltage (V_d) the Fermi-levels are raised, the built-in Schottky barrier and substrate doping combine to limit electron and hole emission into the channel as shown in Fig. 4.2b. Therefore, one advantage in SB-MOSFET is that the channel doping required to achieve a given off-state leakage current is low compared to the conventional MOSFET. As the gate voltage (V_g) is increased, as shown in Fig. 4.2c, the conduction and valence bands are pulled up, the SB-MOSFET is turned ON and tunneling through the built-in Schottky barriers increases until the gate induced electric field at the source renders the Schottky barrier virtually transparent to field emission of charge carriers from the source into the channel region. The net field emission current through the source is exponentially sensitive to the electric field intensity at the source. The physics and models required to understand the ON-state drive current of a SB-MOSFET are fundamentally different from those used in a doped source/drain MOSFET. An accurate calculation of the field emission require detailed analysis of the carrier velocity distribution, density of states, Fermi function, and tunneling probability of carriers that tunnel from the metal into the semiconductor through the sharp triangular barrier at the source end.

For a short-channel device, the potential distribution along the channel is strongly affected by source and drain, which modifies the potential distribution of the entire channel. The depletion regions of drain penetrate deep into the channel region with increasing drain bias and influence the control of the channel charge by the gate. In this case a SB-MOSFET exhibits a larger subthreshold swing and no saturation in the output characteristics [45]. This results in short channel effects which deteriorate the device performance.

In SB-MOSFET the subthreshold leakage (OFF) current is dominated by three constituents: (1) Ambipolar conduction resulting in a gate-induced-drain-leakage (GIDL)-like off-state current I_{GIDL}; (2) junction leakage current I_j and (3) source to drain leakage current I_{sd}. In an SB-pMOSFET I_{GIDL} is due to the tunneling of electrons through the large but thin barrier at the drain side in the OFF state, which is a result of the close proximity of the drain to the gate. This tunneling of electrons

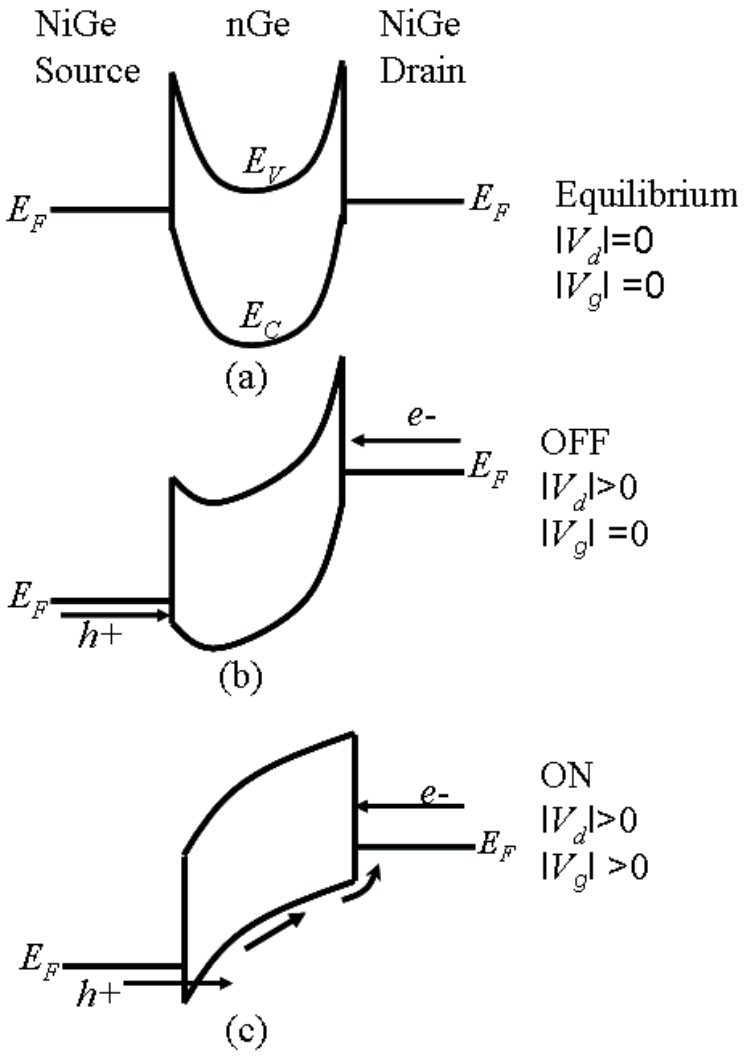

Figure 4.2: Schematic band diagrams of a NiGe/Ge SB-pMOSFET: (a) without any bias at equilibrium, (b) with only drain bias (V_d) and (c) with both drain and gate bias (V_g). Here an electron and a hole are represented by e- and h+, respectively.

is strongly sensitive to the Schottky barrier height to the substrate. Therefore a large Schottky barrier should be used to reduce this leakage current. Junction leakage I_j for an SB-pMOSFET is caused by the reverse biased Schottky barrier at the drain electrode. When the substrate is heavily doped I_j increases. This leakage could be reduced by reducing the doping profile and the drain depth. The source to drain leakage current I_{sd} in an SB-MOSFET is significant and could be controlled by low concentration channel doping profile [45].

The SB-MOSFETs suffer from a large leakage current and a poor ON/OFF ratio due to high GIDL-like off-state current. This mechanism of leakage is often termed as the ambipolar conduction. In Fig. 4.2b, the current due to the electron injection from the drain is the origin of the ambipolar leakage current. For a pMOSFET when V_g becomes more positive, the conduction and valence bands in the bulk Ge are pushed down and the thickness of the drain sided Schottky barrier for electrons is reduced. As a result, the parasitic band-to-band tunneling current of electrons increases and the ambipolar conduction occurs. This conduction results in a V-shaped current-voltage curves in SB-MOSFETs as shown in Fig. 4.3. In order to increase the drive

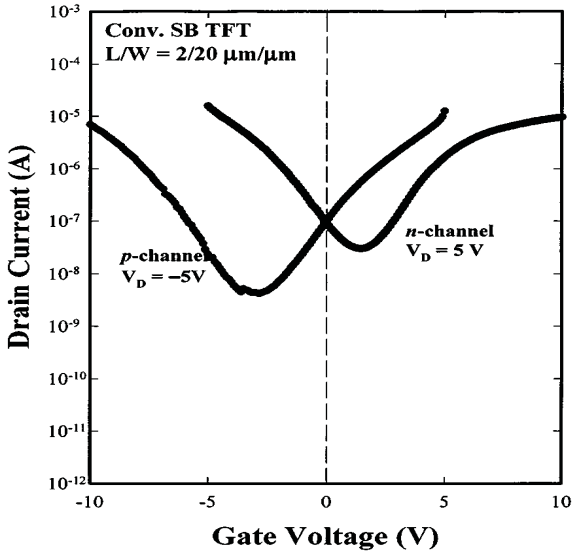

Figure 4.3: Typical ambipolar subthreshold characteristics of SB-MOSFETs (reproduced from Ref. [49]).

capability of a SB-MOSFET, a smaller barrier is needed for the source/drain contact. However, the leakage current increases at the same time, as the thermal emission

increases when the source barrier becomes lower. In addition, the leakage current of a SB-MOSFET increases with increasing drain bias as a result of the GIDL-like effect. Zhang *et al.* [50] proposed to use a recessed channel (shown in Fig. 4.4) and asymetric source/drain Schottky barriers, in which nMOSFET has a higher Schottky barrier at the source and a lower Schottky barrier at the drain, which suppresses the ambipolar leakage current. The schematic of this model is shown in Fig. 4.4. They showed that the recessed channel practically isolates the effect of the drain voltage on the source contact suppressing the short channel effects.

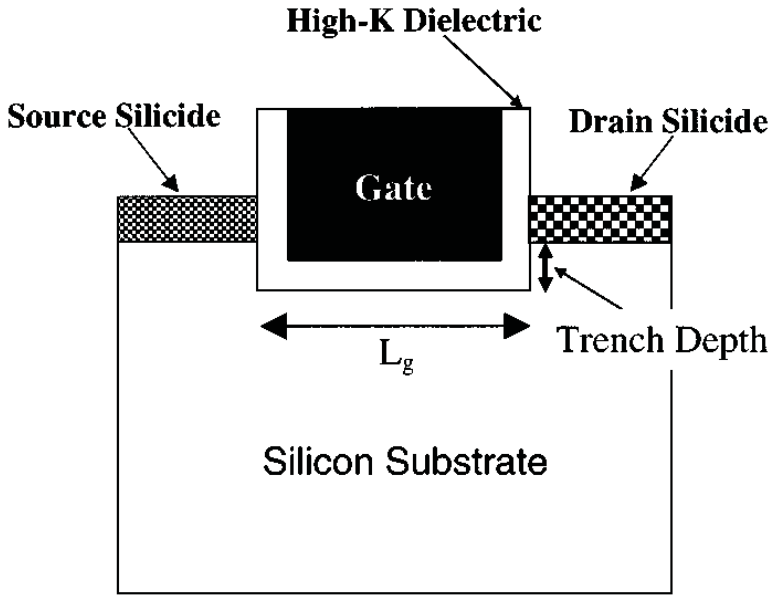

Figure 4.4: A schematic representation of a recessed asymmetric SB-MOSFET (reproduced from Ref. [50]).

Lin *et al.* [49] experimentally showed that by using a field induced drain extension between the channel and the drain the ambipolar leakage could be reduced. Their device structure (shown in Fig. 4.5) features an undoped Si active channel, a top metal field plate (subgate), and Schottky source/drain. During device operation, a high fixed voltage is applied to the subgate to form a field-induced drain extension under the sub-gate region. During the OFF state of the n-channel device, formation of the field-induced drain with the band diagram tends to suppress the emission of holes from the drain as observed in Fig. 4.5.

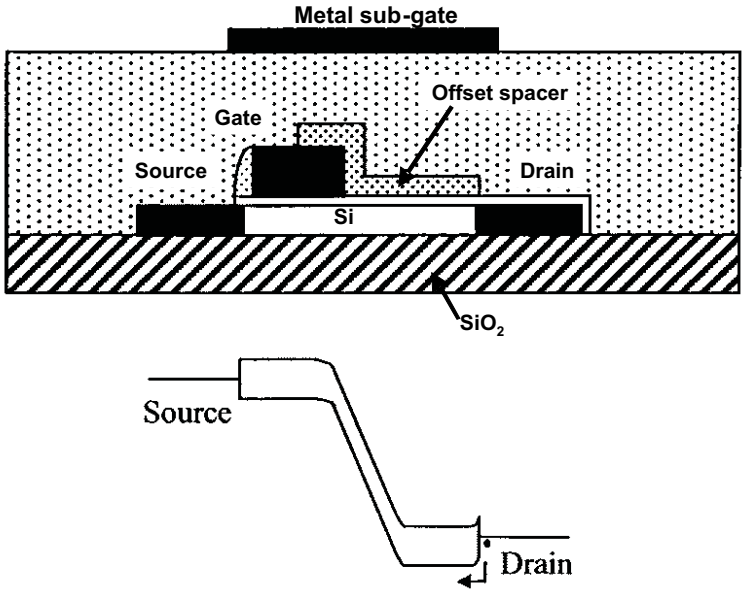

Figure 4.5: Band diagrams for n-channel operation of an SB-MOSFET with field-induced drain extension at off-state (reproduced from Ref. [49]).

4.3 Ge based Schottky barrier MOSFETs

SB-MOSFETs have been proposed as an alternative to conventional MOSFETs for sub-100nm applications and have received an increasing attention in recent years because of the dramatic down-scaling requirement of transistor devices. However, the early works on SB-MOSFETs could not produce high drive currents from the devices. Again the recent works resulted high off-state leakage current in the devices limiting the MOSFETs from using in the practical applications.

SB-MOSFETs were first considered in 1968 [3] because of their simpler fabrication and elimination of high temperature diffusion steps. This work showed that room temperature operation was comparable to traditional MOSFETs and 77 K operation was dominated by tunneling. However, the devices showed poor performance with room temperature drive current ten times lower than that of a conventional MOSFETs. Later, Mochizuki *et al.* [51] investigated an SB-nMOSFET fabricated using tantalum as the barrier metal on p-type silicon. These devices were never considered for practical applications because of low drive currents and difficulty in fabricating the Schottky barriers with reproducible electrical characteristics.

With the arrival of improved device fabrication and self-aligned processes the

development of SB-MOSFET technology has advanced significantly in the past ten years. Several attempts have been taken to improve the drive current and the transistor current ON/OFF ratio. One approach was to use semiconductors with narrow band-gap, eg. Ge, so that the resulting Schottky barrier in the source/drain is low resulting high drive currents. It should be noted that having a high barrier in n-type substrate will result in a low barrier (p-type) in the channel region for p-channel MOSFETs and vice versa.

The motivation for Ge based SB-MOSFET is straight forward firstly because of its much higher carrier mobilities than Si. Moreover, a major problem for ultra short channel MOSFETs, the increased series resistance in the source/drain region, could be solved by germanidation. At the moment researchers focus is on the Ni-mono-germanide phase due to its low resistivity low processing temperature and large processing window (350°C - 500°C) [52–54]. Fig. 4.6 shows the Ni/Ge phase diagram. The crystal structure of NiGe is orthorhombic with four atoms in its unit cell. The simplest way to form a thin germanide film is to deposit Ni on Ge and induce the germanide formation by thermal annealing. Depending on the annealing temperature, a metal rich phase forms first followed by the mono-germanide phase , e.g. according to

$$Ni \rightarrow Ni_2Ge \rightarrow NiGe \tag{4.1}$$

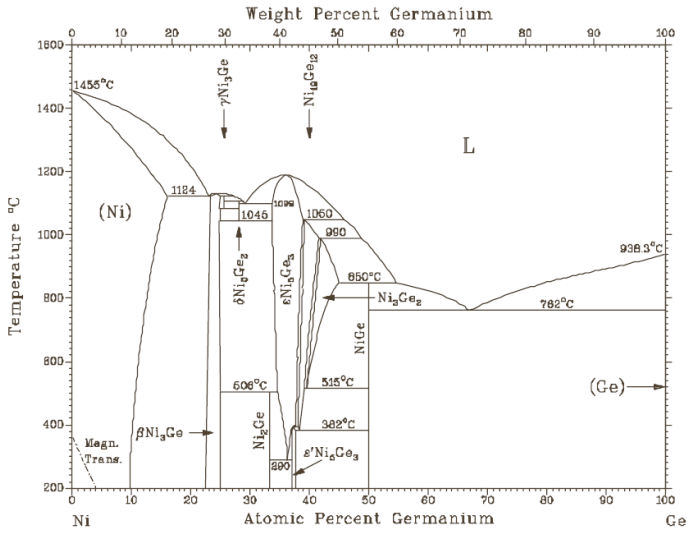

Figure 4.6: Binary phase diagram for Ni/Ge (reproduced from Ref. [55]).

The advantage of Ni-germanidation is that there are no Ge rich phases formed at high anneal temperatures as opposed to Ni-silicidation where $NiSi_2$ phases forms at high temperatures causing agglomeration in the Si rich phase resulting in increased resistivity of Ni-silicides [52].

Several investigations have been performed on Schottky barriers using Ge substrates. Ikeda *et al.* [56] characterised PtGe/Ge Schottky barrier height for Ge channel SB-MOSFET. The barrier height for PtGe/p-Ge was found to be 0.1 eV over a wide range of anneal temperatures making Pt-germanide a promising source/drain material for Ge channel MOSFETs. In another work [57] the same group have successfully demonstrated the barrier height modulation of NiGe/Ge by the segregation sulfur during Ni-germanidation. Implanted sulfur has modulated Schottky barrier height by 0.46 eV, resulting in an electron Schottky barrier height of as low as 0.15 eV for nGe. This method showed that sulfur can mitigate the Fermi level pinning in the Ge band-gap as a result of the reduction in the interface states. In 2005, Zhu *et al.* [54] investigated the NiGe/Ge Schottky barriers on nGe and were able to obtain an electron barrier height of 0.47 eV. The rectification obtained was only 2 order in magnitude. This is due to the barrier height being relatively low and the ideality factor being high which is related to the sharpness of the interface. An optimisation of the Schottky barrier fabrication process could improve the interface properties. Investigation on SB-nMOSFET lacked obviously because of the lack of proper metal silicide that would produce a high barrier height on pSi. Studies were performed on SB-nMOSFET using metals with low work function, such as Yb (2.59 eV) Er (3.12 eV) that would produce high hole barrier height (low electron barrier height). One such attempt was taken in 2004 by Zhu *et al.* [58]. They reported that Yb provided a smoother YbSi/Si interface as opposed to ErSi and DySi, providing improved manufacturability for the SB-nMOSFETs. YbSi provided an I_{ON}/I_{OFF} ratio of 10^7 for a 4 μm gate length device.

SB-pMOSFETs, on the other hand, are investigated extensively, because of the high electron barrier heights of most metals on n-type substrates resulting in low hole barrier heights. Although this has resulted in increased drive currents in the device, their off-state leakage current is still not satisfactory when compared to the conventional doped source/drain MOSFETs. Zhu *et al.* [47] investigated NiGe SB-

pMOSFET on nGe with a channel length of 8 μm and HfAlO gate dielectric. They were able to achieve a drive current 5 times higher to that of a similar structure made from PtSi source/drain pMOSFETs on nSi as presented in Fig. 4.7. This high drive current of Ge based MOSFET was attributed to the smaller hole barrier between NiGe source and the Ge channel of the MOSFET than that of the PtSi/Si barrier of the similar structure. However, the I_{ON}/I_{OFF} ratio of the NiGe SB-MOSFET is $10^2 \sim 10^3$, about five orders of magnitude smaller than that of the PtSi SB-MOSFET. This was due to the large OFF current (0.15 μA/μm at V_d= -1 Volt) in the NiGe MOSFET as a result of relatively low electron barrier height in the drain/substrate contact as compared to that of the PtSi drain/substrate barrier. The larger drive current in the Ge device could also be attributed to the higher carrier mobility.

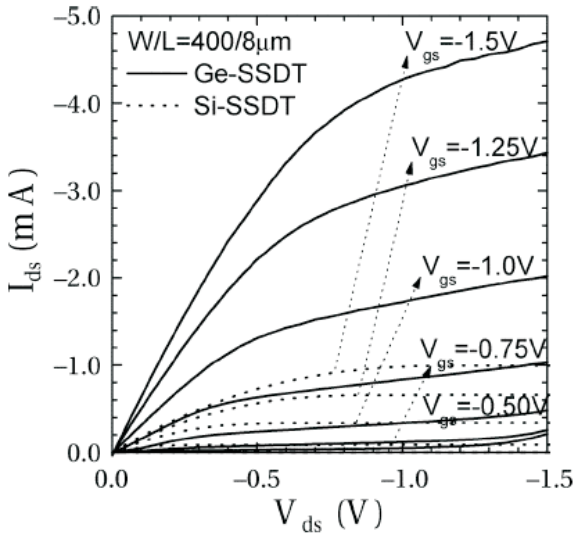

Figure 4.7: I_d-V_d curves of a 8 μm SB-pMOSFETs using NiGe/Ge source/drain. For comparison I_d-V_d of a PtSi/Si SB-pMOSFETs having the same size are shown in dotted lines (reproduced from [47]).

Li *et al.* [43] successfully reduced this leakage current to as low as 1 nA/μm using PtGe/nGe contact in a 8 μm channel SB-pMOSFET. This reduction in I_{OFF} is attributed to the relatively higher electron barrier hight in PtGe/nGe than in NiGe/nGe Schottky barriers. Compared to the conventional Boron-doped source/drain Ge MOSFET of similar device dimensions, this leakage current is still 80% higher [59].

For short channel SB-pMOSFETs, extensive investigation have been done by Larson *et al.* [45, 60]. Results on sub-30 nm gate length pMOSFET with PtSi Schottky

barrier source/drain are reported. These deeply scaled transistors, having low series resistance and high drive current and very low leakage currents, are promising for high speed analog applications. A summary of their results along with previously discussed literature on SB-MOSFETs has been presented in Table 4.1 showing their I_{ON}/I_{OFF} ratio, off state leakage current (at V_g of 1 Volt), channel doping densities and source/drain Schottky electron barrier heights. However, making direct comparison is somewhat difficult since the devices had differing oxide thickness, channel length and bias conditions.

Ref.	Technology	$L_g(\mu m)$	I_{OFF}	I_{ON}/I_{OFF}	Doping	ϕ(eV)
[47]	NiGe,PMOS	8	0.15 μA/μm	10^3	8x10^{14}	0.50
[46]	NiGe,PMOS	8	-	10^3	8x10^{14}	0.74
[44]	PtGe,PMOS(GOI)	10	5.5x$10^{-5}$$\mu$A/$\mu$m	10^3	8x10^{15}	-
[58]	YbSi,NMOS	4	10^{-6} A/cm^2	10^7	-	0.27
[43]	PtGe,PMOS	8	$10^{-3}$$\mu$A/$\mu$m	10^4	10^{14}	0.76
[45]	PtSi,PMOS	0.025	6149 nA/μm	102	10^{15}	0.89
[60]	PtSi,PMOS	0.025	168 nA/μm	2700	$10^{15} + As$	0.89
[45]	PtSi,PMOS	0.060	12 nA/μm	2.6x10^4	10^{15}	0.89
[45]	PtSi,PMOS	0.080	6 nA/μm	5x10^4	10^{15}	0.89

Table 4.1: A summary of SB-MOSFETs literature.

The source to drain leakage current I_{sd} in an SB-MOSFET is significant of all the leakage currents and could be controlled by low concentration channel doping profile [45]. In a short channel device the subthreshold leakage from source to drain is significantly reduced when a channel implant is used. This was addressed by Larson *et al.* In addition to having a lower doping concentration in the channel an implant profile was used which is laterally uniform but vertically nonuniform. Fig. 4.8a provides the results from an un-implanted 25-nm gate length device which shows I_{ON} is 629 μA/μm and I_{OFF} is 6140 nA/μm and the ON/OFF current ratio is 102 for the lightly doped substrate (10^{15} cm^{-3}). However, when an As channel implant was performed on the same device structure, I_{ON} and I_{OFF} is recorded as 460 uA/um and 168nA/um respectively with an ON/OFF ratio of 2700 as shown in Fig. 4.8b. Therefore an optimisation of the doping concentration in the channel area will be required to reduce the source to drain subthreshold leakage currents.

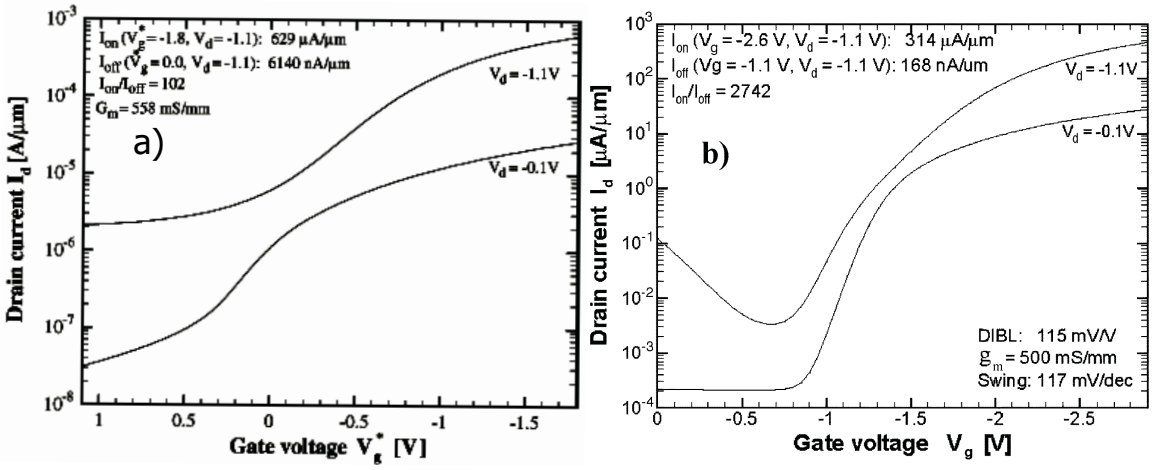

Figure 4.8: I_d-V_g curves of a 25 nm Si channel SB-pMOSFET having (a)no channel implant and (b)with an As implant for leakage current reduction (reproduced from Ref. [45]).

The early works for Schottky barrier formation discussed above were based physical vapour deposition of metal on semiconductor e.g. evaporation and sputtering. In evaporation, the substrate is placed inside a vacuum chamber, in which a block (source) of the material to be deposited is also located. The source material is then heated to the point when it starts to melt and evaporate. The vacuum is required to allow the molecules to evaporate freely in the chamber, and then subsequently condense on the substrates. In sputtering, an Ar plasma is accelerated toward the source target and sputtering off the molecules which deposit on the wafer. In contrast to these metal deposition techniques, electrodeposition is not a standard silicon fabrication process. However, this technique is very attractive since it produces a sharp interface between the metal and the semiconductor.

The work presented in this research adds to the literature in the following way. It has been pointed out by Kiziroglou *et al.* [5, 6] that Ni/Si Schottky barriers prepared by electrodeposition show superior properties to physical vapour deposition. Therefore, in this work, Ni/Ge Schottky barriers grown by electrodeposition will be investigated for possible application as source/drain in SB-MOSFETs. The objective is to obtain thermal stability in the Schottky barriers with high rectification and low reverse bias current and low series resistance for the source/drain.

4.4 Experimental procedure

For the fabrication of Ni/Ge Schottky barriers, Sb-doped Ge (100) wafers were taken as the starting materials. Square patterns of sizes from 10 μm to 400 μm were transferred to the photoresist coated substrates by conventional lithography which was followed by the electrodeposition of Ni. The complete process flow for the Schottky barrier fabrication is shown in Fig. 4.9. The back ohmic contacts on Ge were defined by Au-Sb(0.1%) evaporation and annealing the samples in an $H_2(2\%)/N_2$ inert atmosphere at 300°C for 30 minutes. A test structure containing back-to-back contacts were also created. The corresponding current voltage characteristics of back-to-back contacts for different Ge resistivity are presented in Fig. 4.10. The linear increase in current for the various applied biases confirms the formation of back ohmic contacts on Ge. Buffered HF pretreatment on Ge 30 seconds followed by de-ionised water wash was performed several times immediately prior to electrodeposition. For electrodeposition, a Ni sulphate bath and an Autolab AUT72032 potentiostat three-electrode system with a Pt counter electrode and a saturated calomel reference electrode were used. In order to determine an optimum deposition potential for Ni deposition on Ge, a cyclic voltammogram was initially obtained for the Ge substrates. For Ni electrodeposition on the photoresist patterned Ge substrates, the deposition potential ranged between -1.10 to -1.15 Volts was chosen that resulted in a smooth, continuous Ni film. The Ni film thickness was controlled by measuring the charge accumulated at the cathode during electrodeposition and using the equation presented in section 2.3.2. The various film thicknesses were also measured using SEM on a cross-section of the electrodeposited film. In this experiment two different thicknesses of 70 nm and 20 nm of Ni film were electrodeposited on the Ge substrates.

$I-V$ and $C-V$ characteristics measurements were performed using a Hewlett Packard 4155C semiconductor parameter analyzer and a Hewlett Packard 4280A, 1 MHz, capacitance Meter/$C-V$ plotter. Germanidation of the Ni films was performed by annealing the samples for 20 minutes in an inert atmosphere at temperatures ranging from 300°C to 500°C.

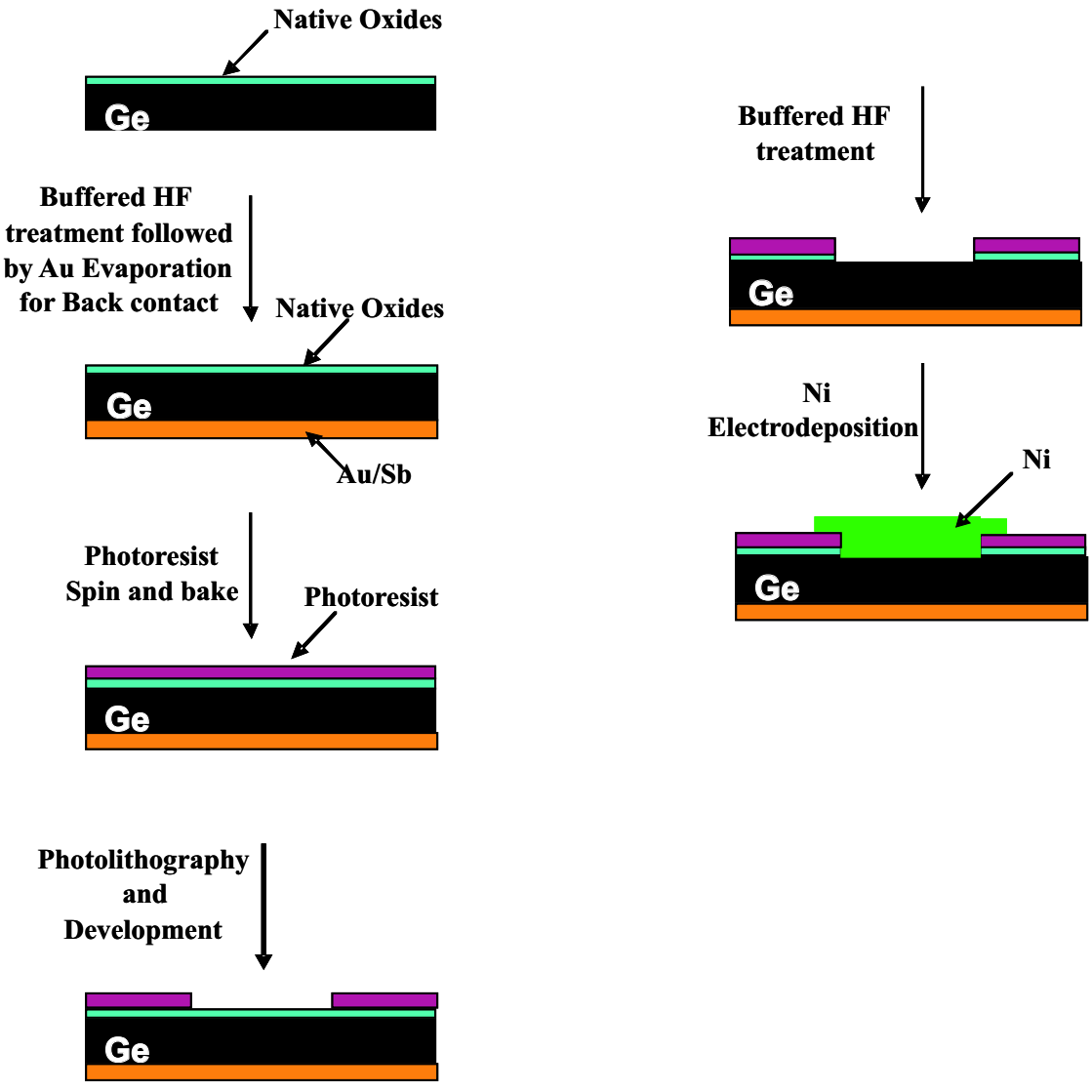

Figure 4.9: Process flow for a Ni/Ge Schottky barrier fabrication.

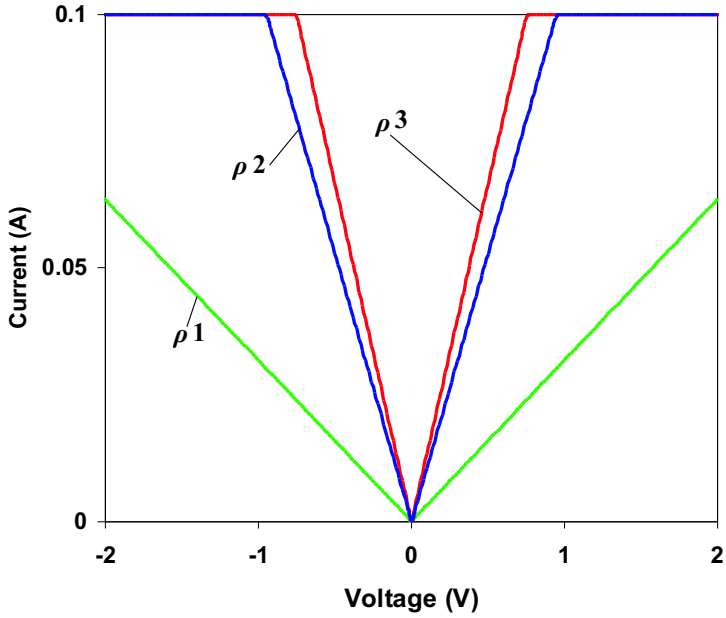

Figure 4.10: *I-V* characteristics of the back-to-back ohmic contacts created on Ge wafers with resistivity of ρ1=2-2.4 Ω-cm, ρ2=0.13-0.15 Ω-cm and ρ3=0.005-0.02 Ω-cm.

4.5 Results and discussions

4.5.1 Germanidation of Ni

The electrodeposited Ni films on Ge (0.005-0.02 Ω-cm) were annealed for 20 minutes at temperatures ranging from 300°C to 500°C to investigate their germanidation mechanism. Phase identification and crystallographic structure determination were carried out using XRD with Cu Kα radiation (λ = 1.5418 $\mathring{A}$) in a θ-2θ geometry. Fig. 4.11a shows the XRD spectra for as-deposited and annealed Ni/Ge samples for initial Ni thicknesses of 70 nm. The initial Ni (111) peak at 44.68° completely disappears after annealing indicating complete reaction of the Ni film with Ge. Peaks at 34.8°, 35.2°, 44.2°, 45.7°, 53.8° and 54.4° are observed when the sample was annealed at 500°C. These peaks are in excellent agreement with the θ-2θ pattern of the NiGe Joint Committee on Powder Diffraction Standards data. The peaks were identified as NiGe(111), (210), (211), (121), (002) and (301), respectively. No peaks corresponding to other Ni-germanides, e.g., Ni_2Ge $NiGe_2$, etc. are observed. This clearly

shows only polycrystalline Ni-mono-germanide (NiGe) phase forms at the annealing temperatures.

Using the peak positions of the XRD spectra the lattice constants for the orthorhombic NiGe can be determined using Bragg's law given by

$$n\lambda = 2d\sin\theta \tag{4.2}$$

where n is an integer, λ is the wavelength and d is the lattice spacing given by

$$d = \frac{1}{\sqrt{\frac{h^2}{a^2} + \frac{k^2}{b^2} + \frac{l^2}{c^2}}} \tag{4.3}$$

where *h,k,l* are Miller indices and *a,b,c* are lattice constants. From the peak positions of the XRD spectra shown in Fig. 4.11a, using a least square approach, the lattice constants of the formed NiGe are determined to be $a = 5.81$ $\mathring{A}$, $b = 5.37$ $\mathring{A}$, and $c = 3.40$ $\mathring{A}$, in agreement with the reported values [52, 53].

For a 20-nm Ni on Ge sample the peaks of the XRD spectra for the various NiGe crystal orientations are found to be relatively weak as shown in Fig. 4.11b. As happened in the case of the 70 nm Ni film samples, the Ni (111) peak also disappears when the sample is annealed at 300°C. When the annealing temperature is increased, the peaks of NiGe (111), (130), (002), and (301) are observed.

In order to investigate the crystallite sizes of the electrodeposited Ni and that of NiGe (111) formed by annealing of the 70 nm and 20 nm Ni film, further XRD scan is taken within close intervals surrounding the peak positions of the corresponding phases. The XRD spectra of the Ni(111) peak as a function of annealing temperatures for the 70 nm and 20 nm Ni/Ge samples is shown in Fig. 4.12. The crystallite sizes are calculated from the full width half maximum of the peaks using the Scherrer relation

$$Crystallite\ size = \frac{0.9\lambda}{d_b cos\theta} \tag{4.4}$$

where λ is the wavelength of the X-rays and d_b is the broadening of the XRD peak due to crystallite size measured in radians. For increased accuracy of the calculation of crystallite size, the resolution ($d_{Res} = 0.06°$, obtained from the Ge (004) peak widths (not shown)) of the XRD was also taken into account and the accurate broadening is calculated from:

$$d_b = \sqrt{{d_{Observed}}^2 - {d_{Res}}^2} \tag{4.5}$$

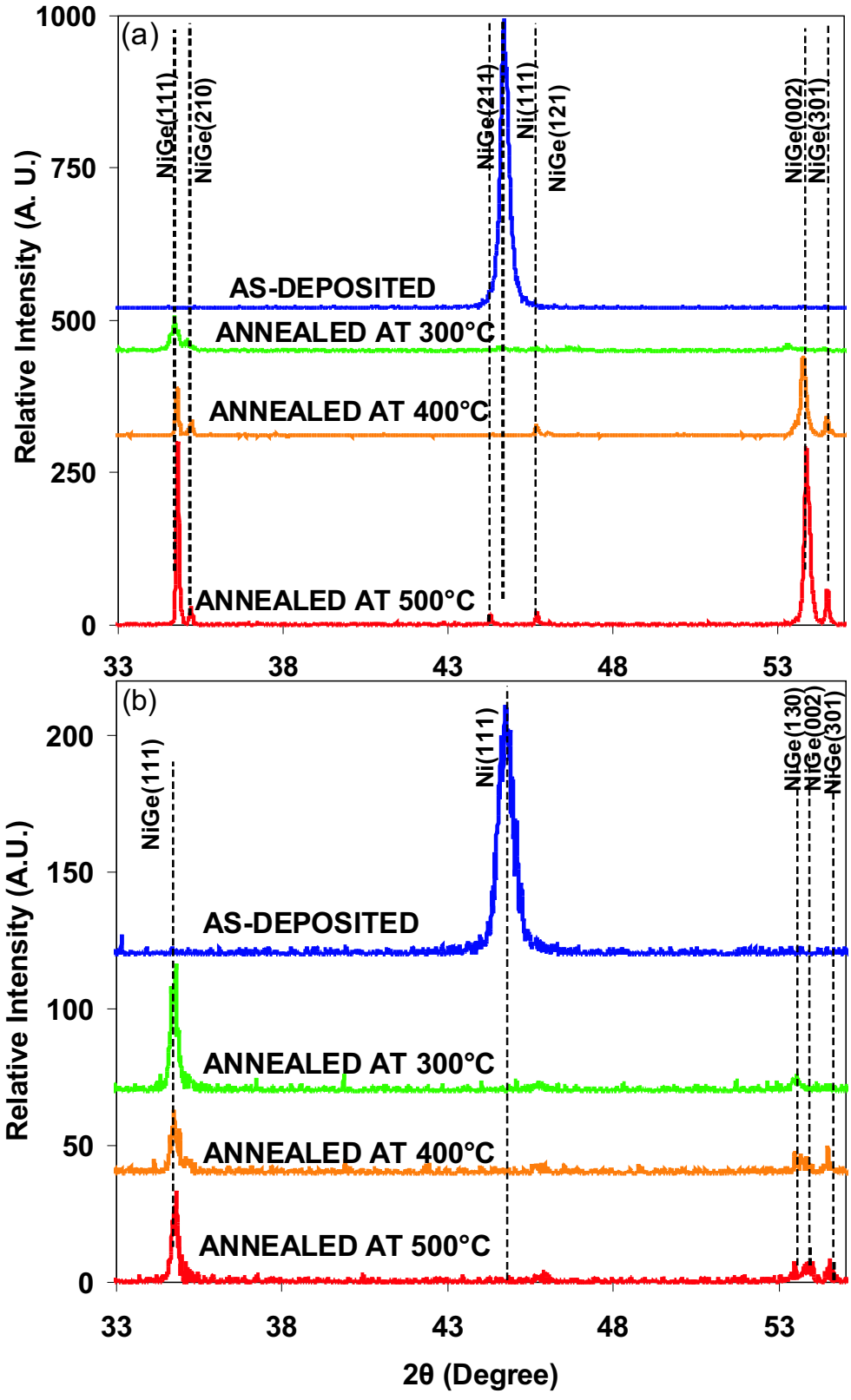

Figure 4.11: The XRD spectra for (a)70 nm and (b)20 nm as-deposited and annealed Ni/Ge samples showing transformation from Ni to NiGe.

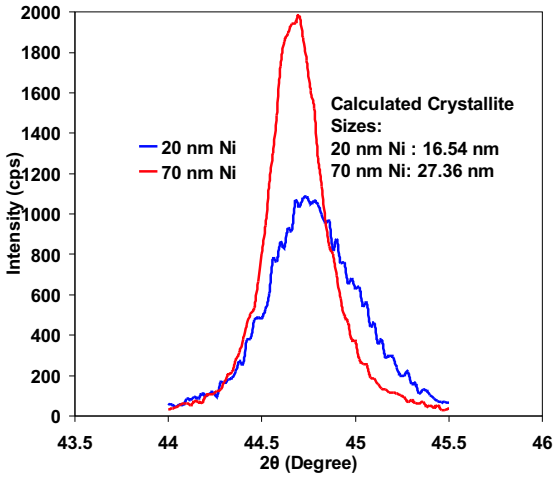

Figure 4.12: XRD spectra of the as-deposited 70 nm and 20 nm Ni on Ge samples. The calculated crystallite sizes are presented in the inset.

The crystallite sizes of the 70 and 20 nm electrodeposited Ni film is calculated to be 27.36 nm and 16.54 nm respectively.

The crystallite sizes for NiGe(111) are calculated from the XRD scan presented in Fig. 4.13 for the 70 nm and 20 nm Ni/Ge samples annealed at various temperatures and are presented in Table 4.2. For the 70-nm as-deposited Ni/Ge sample the crystallite sizes are seen to increase with increasing anneal temperatures. However, for the 20-nm-Ni/Ge sample the crystallite sizes of NiGe(111)annealed at 300°C, 400°C and 500°C showed no significant change, indicating that the solid state reaction to form NiGe has already been completed at 300°C.

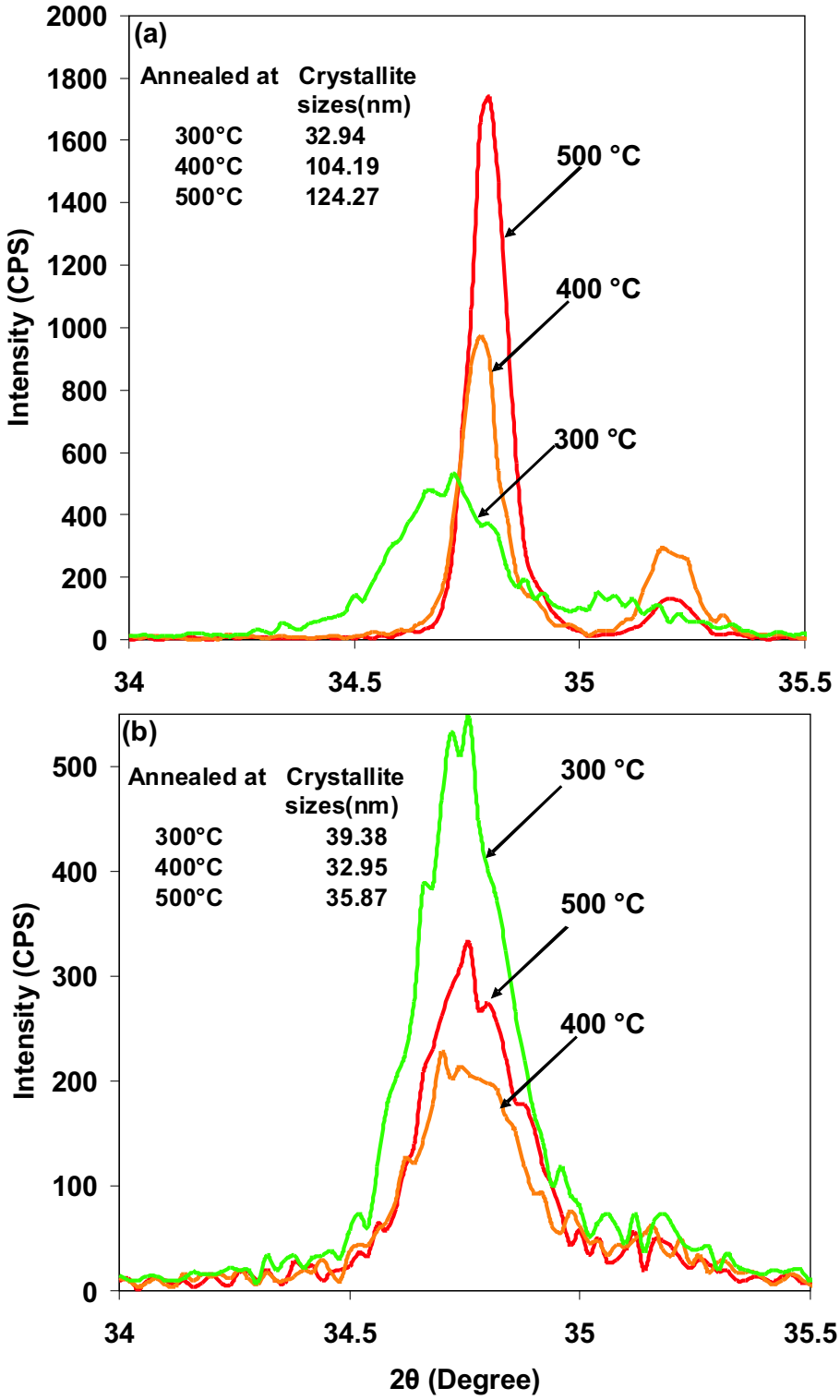

Figure 4.13: XRD spectra showing the NiGe(111) peak of the (a) 70 nm and (b) 20 nm Ni films on Ge samples annealed at various temperatures. The calculated crystallite sizes are presented in the inset.

Anneal Temp (°C)	Crystallite (nm): 70 nm Ni	Crystallite (nm): 20 nm Ni
As-deposited	27.36	16.54
300°C	32.94	39.38
400°C	104.19	32.95
500°C	124.27	35.87

Table 4.2: Crystallite sizes of the as-deposited 70 nm and 20 nm Ni and the transformed NiGe(111) films at various annealing temperatures.

The variation of thickness of the Ni and NiGe as a function of annealing temperature was determined by cross-sectional SEM. Fig. 4.14 shows the SEM images of the 70 nm as deposited Ni on Ge sample annealed at various temperatures. The Ni and NiGe films are clearly visible in white on grey Ge substrates. The SEM images of the samples with 20 nm Ni at various annealing temperatures were unclear and ambiguous and hence, not presented. The average measured thicknesses of the films obtained from Fig. 4.14 are presented in Table 4.3.

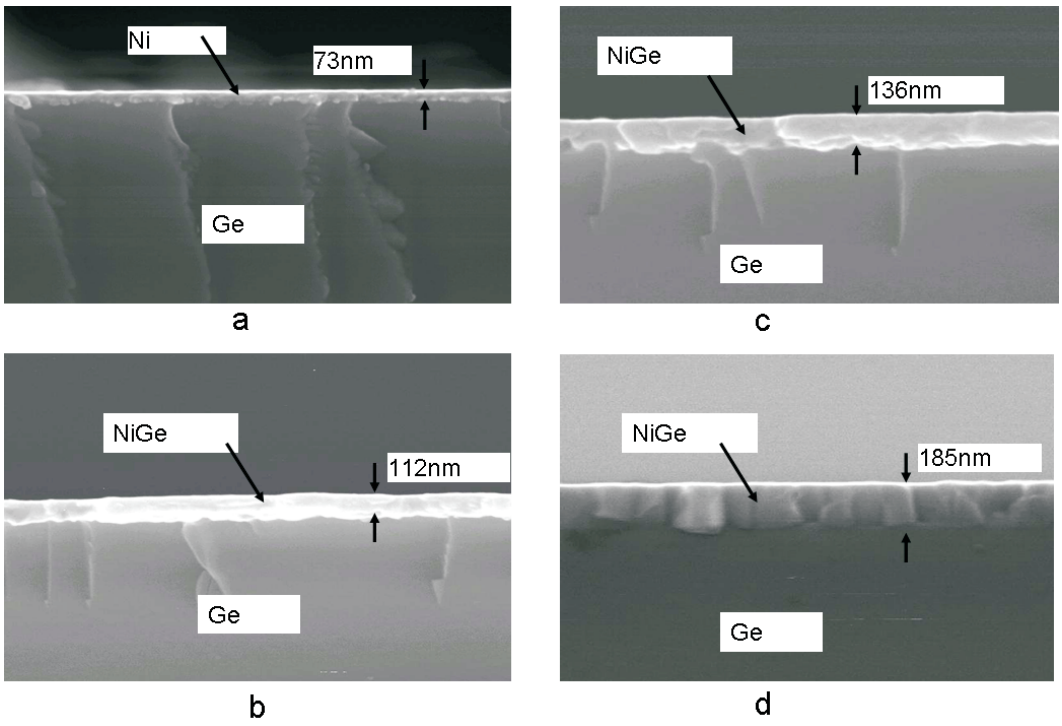

Figure 4.14: Cross sectional SEM images of the various Ni/Ge samples: (a) as-deposited, (b) annealed at 300 °C, (c) annealed at 400 °C, and (d) annealed at 500 °C.

Annealing Condition	Film thickness (nm)
As-deposited	73
300°C Anneal	112
400°C Anneal	136
500°C Anneal	185

Table 4.3: Film thicknesses measured as a function of various annealing temperatures for Ni/Ge contact with 70 nm Ni.

The as deposited Ni film thickness on Ge sample is found to be 73 nm as seen in Fig. 4.14a. As the sample is annealed, Ni diffuses into Ge and starts solid state reaction forming various phases of thicker germanide films. The average thickness of the Ni-germanide film is seen to increase at annealing temperatures of 300°C, 400°C and 500°C as presented in Table 4.3. At 500°C annealing temperature, the maximum average thickness of the film was measured to be 185 nm. The corresponding film grains are seen clearly to grow vertically from Ge surface as presented in Fig. 4.14d.

With increasing annealing temperature the thickness varies firstly due to the diffusion of Ni into Ge and then the formation of a combination of any Ni-rich phases of germanides and the Ni mono-germanide. However, the XRD results presented in Fig. 4.11 could not verify the existence of any Ni rich phases. This could be due to the phases being amorphous or very thin at these annealing temperatures. Therefore at the annealing temperatures of 300°C and 400°C the reaction starts forming little amount of the Ni-rich Germanides and Ni mono-germanides. The ratio of the thickness the Ni-Germanide film annealed at 500°C to the as-deposited Ni thickness is calculated to be 2.53. The ratio of the theoretically calculated atomic volume of Ni-mono-Germanide to Ni is 2.44 as presented in Table 4.4. This concordance of the ratios indicates that the deposited Ni (70 nm) has been totally transferred to NiGe at 500°C annealing temperature. It follows that 1 volume of Ni produced 2.53 volume of NiGe. These results are in good agreement with those obtained by Zhu *et al.* [54] and Spann *et al.* [53].

In order to further exploit the germanidation mechanism the sheet resistance R_{sh} of the grown films was measured using the four-point probe method. The obtained R_{sh} values were multiplied by the film thicknesses to calculate the film resistivity ρ. The results are plotted as a function of annealing temperatures in Fig. 4.15. It is

Mat	Structure	$a(\AA)$	b $(\AA)$	c $(\AA)$	Atoms	At. Vol. $(\AA^3)$	Vol. Ratio to Ni
Ni	fcc	3.520	3.520	3.520	4	10.90	1
Ge	Diamond	5.660	5.660	5.660	8	22.67	2.07
NiGe	Orthorhombic	5.814	5.375	3.404	4	26.59	2.44

Table 4.4: Lattice constants and the calculated atomic volume of Ni, Ge and NiGe.

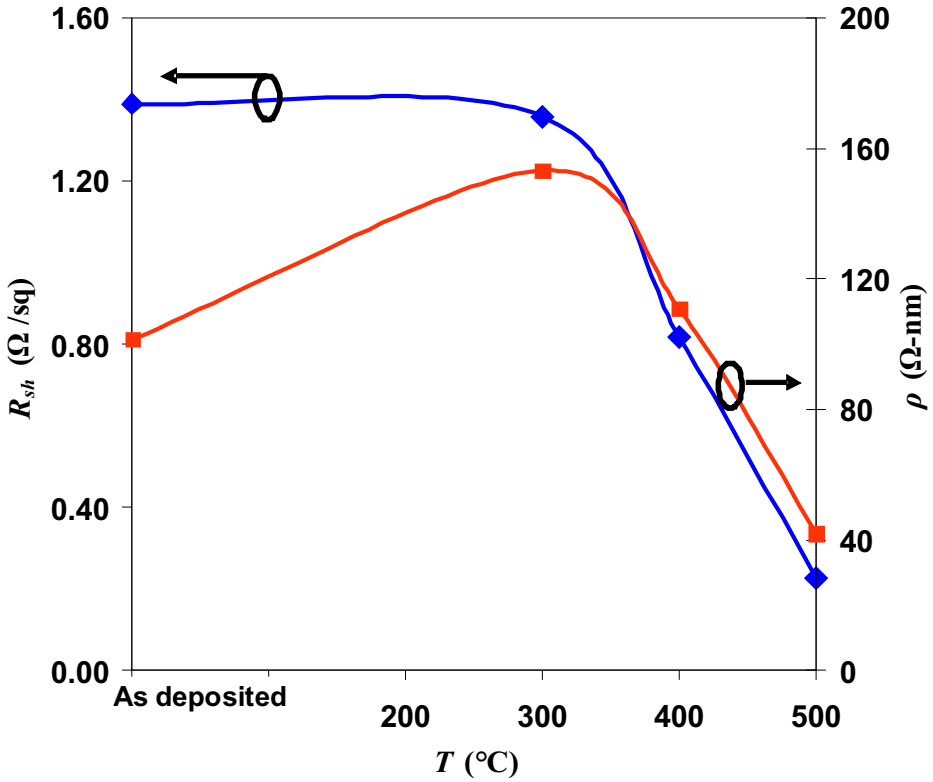

Figure 4.15: R_{sh} and ρ of Ni and NiGe films at various anneal temperatures T. The initial Ni thickness was 70 nm. The substrate resistivity was 0.005-0.02 Ω-cm.

observed that R_{sh} decreased with increasing temperature T. The measured R_{sh} of NiGe is 0.23 Ω/sq when annealed at 500 °C. The low R_{sh} could be attributed to the increase in crystallite size at 500 °C as observed in Fig. 4.13a. The resistivity of NiGe also decreased when the films were annealed above 300 °C.

4.5.2 Electrical characteristics

Typical $J-V$ characteristics of electrodeposited Ni/Ge Schottky barriers for three different substrate resistivities (ρ1=2-2.4 Ω-cm, ρ2=0.13-0.15 Ω-cm and ρ3=0.005-0.02 Ω-cm) and of 10 μm square contact area are presented in Fig. 4.16.

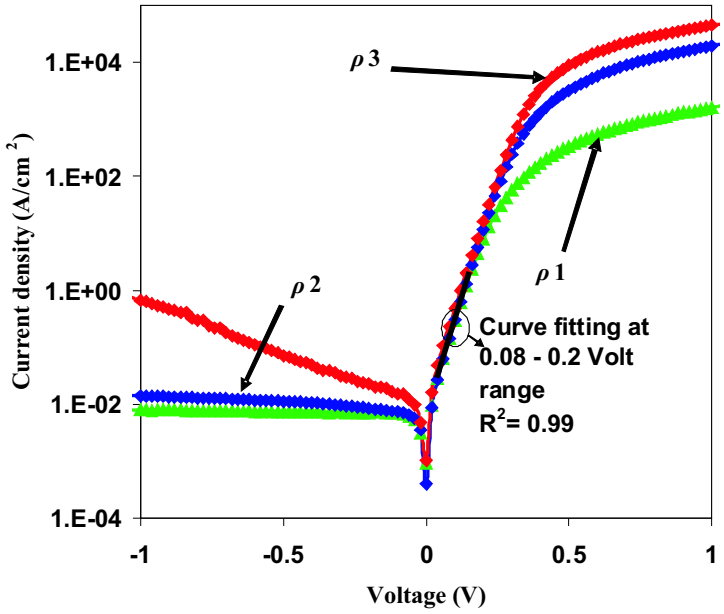

Figure 4.16: $J-V$ characteristics of the Ni/Ge Schottky diodes (10 μm square contact) as a function of Ge resistivities (ρ1=2-2.4 Ω-cm, ρ2=0.13-0.15 Ω-cm and ρ3=0.005-0.02 Ω-cm). The TE model was fitted in the voltage range of 0.08-0.2 Volts.

A high-quality rectifying behaviour is observed for the Schottky barriers. For the highly resistive (ρ1) Ge, excellent Schottky barriers are achieved with very low reverse bias current, being ∼5 orders of magnitude smaller than the forward bias current at 1 Volt bias. Tunneling effects of this Schottky barrier are negligible in the reverse bias. Schottky barriers on the medium resistive (ρ2) Ge showed similar rectifying behaviour with a little tunneling current in the reverse direction. On the low resistive substrate (ρ3), Ni/Ge Schottky barrier showed increased tunneling effects in the reverse bias. However, even these diodes showed excellent rectifying behaviour with the reverse bias current of the diodes at the low resistive (ρ3) substrate still 5 orders in magnitude smaller than the forward bias current. All currents can be explained by standard TE and additionally TFE theory for the reverse biased Schottky barrier. In

the following section it will be shown by numerical simulation that both forward and reverse bias currents are dominated by electron transport. This is a significant improvement over similar work done in literature [54, 56] where Schottky barriers grown by evaporation technique exhibited rectification of only 2-3 orders even on highly resistive Ge substrates. Breakdown of the diodes was not observed up to -3 Volts bias indicating that edge effects are suppressed as explained in Ref. [35].

From the $J-V$ curves in Fig. 4.16, the Ni/Ge Schottky electron barrier height ϕ_n, ideality factor η and series resistance R_S can be extracted assuming the TE model in the forward bias [61]. The calculated Schottky barrier parameters are presented in Table 4.5 for all type of substrates. For these calculations Richardson constant (A^*) of 50 A cm^{-2} K^{-2} [36, 37] was used. The standard deviation of the electron barrier height and the ideality factor are obtained from the data of eight different samples grown under the same electrodeposition conditions. It is seen from Table 4.5 that the Schottky barrier heights are virtually constant for the Ge substrates of various resistivities. The low ideality factors indicate TE to be the dominant current conduction mechanism in the forward bias for the Schottky barriers on different substrates.

$C-V$ measurements of Schottky barriers on Ge were performed for A^*-independent measurement of the Schottky barrier height. Inverse square capacitance versus voltage characteristics are shown in Fig. 4.17 for Schottky barriers on Ge substrates of various resistivity and having a contact area of 400 μm square. As expected, a straight line is observed, and from its intercept on the voltage axis the Schottky barrier height ϕ_n is calculated [1]. Furthermore, from the slope of this characteristic, the Ge doping concentration N_d can be determined. For example a value of 2.9×10^{17} cm^{-3} for N_d is obtained corresponding to a resistivity of 0.006 Ω-cm, which matches the specification of the Ge substrate. Similar $C-V$ measurements were performed on Schottky barriers on the medium (0.13-0.15 Ω-cm) and highly (2-2.4 Ω-cm) resistive Ge and barrier heights (ϕ_n) of 0.53 eV and 0.56 eV and substrate doping densities of 1.45×10^{16} cm^{-3} and 8.7×10^{14} cm^{-3} were obtained, respectively. The barrier heights obtained are in good agreement with those obtained from the $J-V$ measurements as observed in Table 4.5. The standard deviation of the electron barrier heights are obtained from the data from five different devices grown under the same electrodeposition potential.

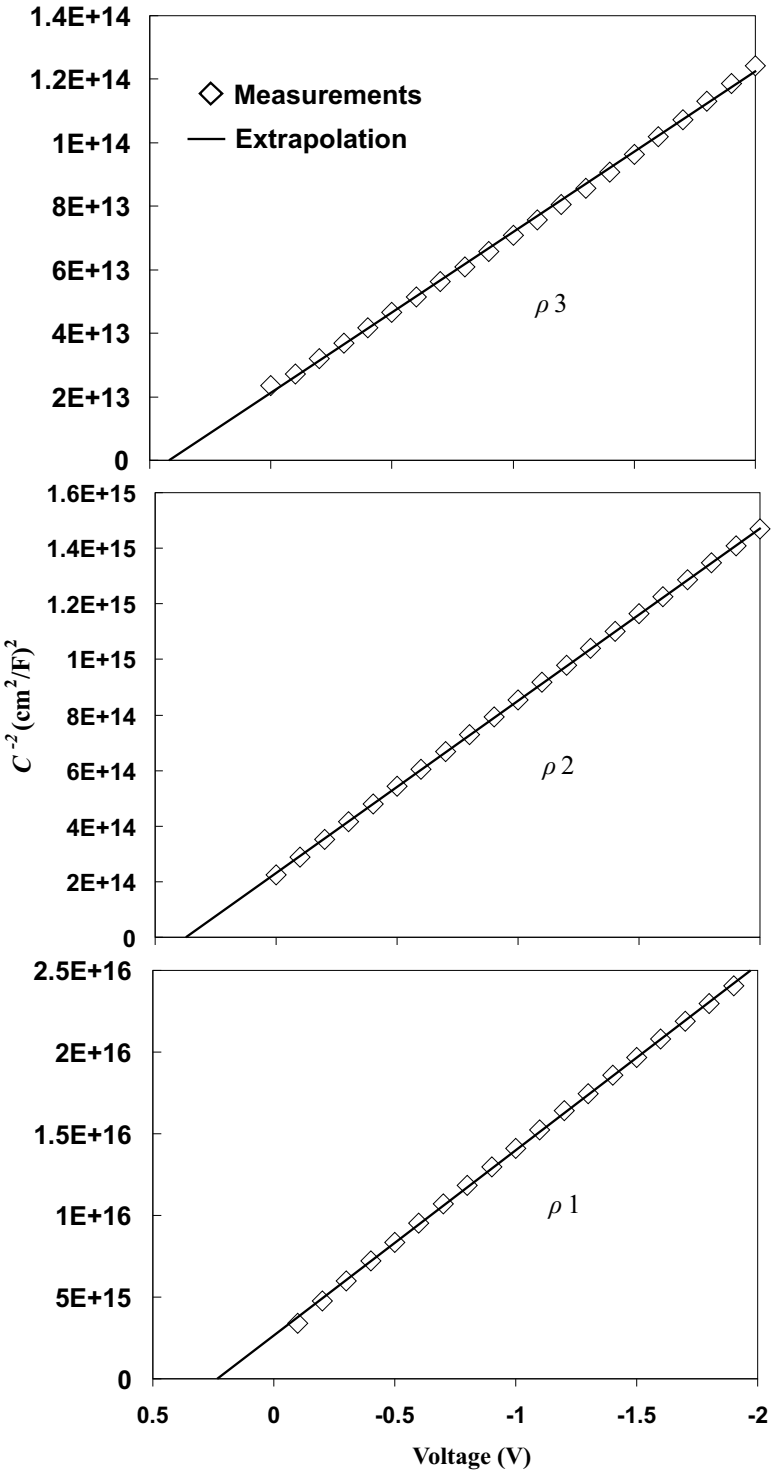

Figure 4.17: $C^{-2} - V$ curve of electrodeposited Ni/Ge Schottky barriers (400 μm square) for various substrate resistivities (ρ1=2-2.4 Ω-cm, ρ2=0.13-0.15 Ω-cm and ρ3=0.005-0.02 Ω-cm).

Resistivity Label ⇒	$\rho 1$	$\rho 2$	$\rho 3$
η (8 devices)	1.12 ± 0.01	1.04 ± 0.02	1.09 ± 0.02
R_S (Ω)	30.77	16.05	11.72
ϕ_n(eV) (from J-V) (8 devices)	0.52 ± 0.01	0.53 ± 0.01	0.52 ± 0.02
ϕ_n(eV) (from C-V) (5 devices)	0.569 ± 0.003	0.534 ± 0.002	0.534 ± 0.002
N_d(cm^{-3})	8.7×10^{14}	1.45×10^{16}	2.9×10^{17}
Resistivity (Ω-cm) (nominal)	2-2.4	0.13-0.15	0.005-0.02
Resistivity (Ω-cm) (from C-V)	1.84	0.11	0.006

Table 4.5: Extracted ϕ_n, η, R_S (from $J-V$ method) and ϕ_n, N_d, substrate resistivity ($C-V$ method) of the Ni/Ge Schottky barriers.

Typical current $I-V$ characteristics of the grown Ni/Ge Schottky barriers under various annealing conditions on low resistive (0.005-0.02 Ω-cm) Ge are presented in Fig. 4.18 for a contact pad size of 20 μm square. A high quality rectifying behaviour ($\sim$4-5 orders in magnitude) is observed for all annealing conditions. Again, ϕ_n, η and R_S are calculated assuming the TE model in the forward bias region and are presented in Table 4.6. The values of ϕ_n are virtually constant at 0.52 eV. Assuming a Ge band gap of 0.66 eV the corresponding hole barrier height is 0.14 eV. This value is low enough to guarantee a large ON current in SB-MOSFET. At low forward bias there is a considerable overlap of the current curves of the non-annealed Ni/Ge, and NiGe/Ge Schottky barriers as observed in Fig. 4.18. This indicates both thermal stability and Fermi-level pinning in the Ge band gap as the barrier height is independent of the metal work function. The reverse current at 1 Volt bias is $\sim$1 μA for the various annealed diodes. This is a significant achievement as this value is more than an order of magnitude smaller than the reported value in literature [54] for NiGe/Ge diodes formed by evaporation on highly resistive (4-6 Ω-cm) Ge.

The low values of ideality factor for the Schottky barriers presented in Table II indicate TE to be the dominant current conduction mechanism in the forward bias.

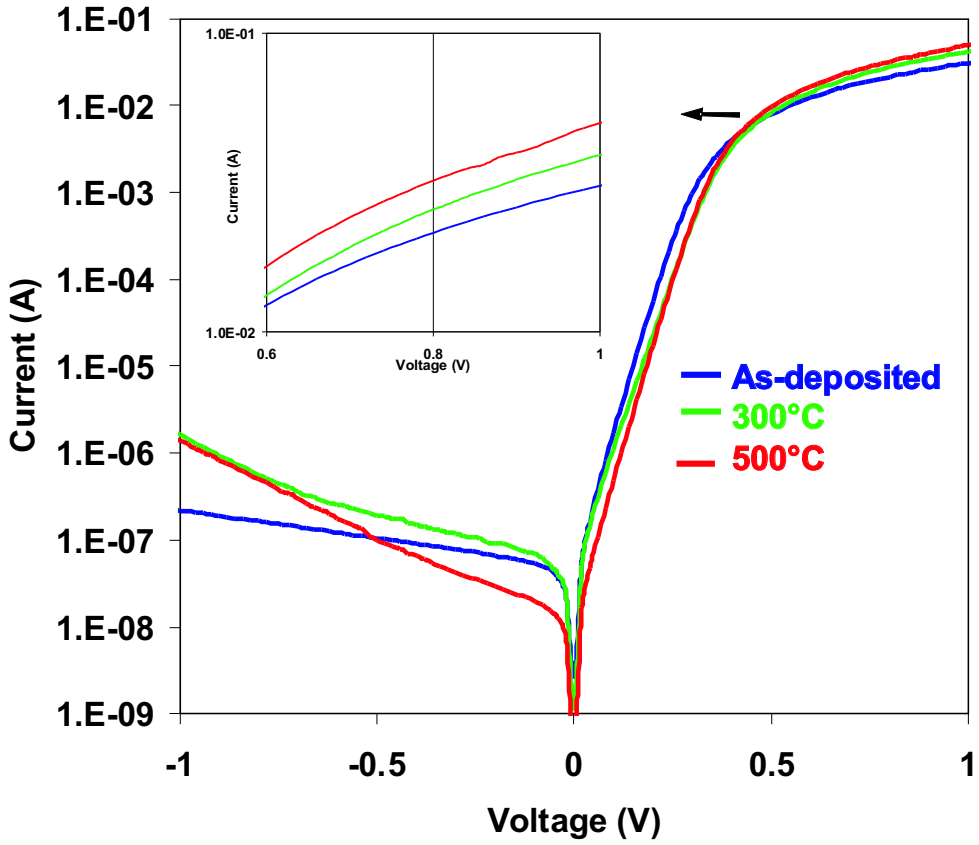

Figure 4.18: $I-V$ characteristics of the Ni/Ge Schottky barriers, having a contact area of 20 μm square, as a function of annealing temperatures. Ge resistivity was 0.005-0.02 Ω-cm. The high forward bias region is magnified in the inset.

The series resistance decreases with increasing T (see the inset of Fig. 4.18) indicating lower specific resistance of NiGe than Ni. This is consistent with the four point probe measurement presented in Fig. 4.15.

In order to validate the findings presented in the experiments the reproducibility of the electrical characteristics under various annealing conditions for a number of Ni/Ge Schottky barriers grown under the same electrodeposition conditions are investigated. Fig. 4.19 and Fig. 4.20 show the $I-V$ characteristics as a function of annealing temperatures of a number of Ni/Ge Schottky barriers grown under an electrodeposition potential of -1.10 Volts against the reference electrode when Ge resistivity was 0.005-0.02 Ω-cm. These devices are different only in their contact areas (20 μm square for Fig. 4.19 and 40 μm square for Fig. 4.20). The overlap in the

T(°C)	ϕ_n(eV)	η	R_S (Ω)
None (8 devices)	0.52 ± 0.02	1.09 ± 0.02	21.32
300 (6 devices)	0.52 ± 0.02	1.27 ± 0.08	14.79
400 (6 devices)	0.55 ± 0.01	1.13 ± 0.03	11.83
500 (6 devices)	0.55 ± 0.01	1.08 ± 0.03	10.85

Table 4.6: Extracted ϕ_n, η and R_S of the Ni/Ge Schottky barriers with 20 μm square contact area as a function of annealing temperature T.

$I - V$ characteristics of all the Schottky barriers in the low forward bias region observed in both Fig. 4.20 and Fig. 4.19 validates the fact that Fermi-level pinning is independent of the annealing temperatures in the Ni/Ge Schottky barriers. Moreover, in the high forward bias region a trend of increase in the current with increasing annealing temperature is observed. This further validates that with increasing annealing temperature the series resistance decreases due to the formation of thicker Ni-mono-germanides.

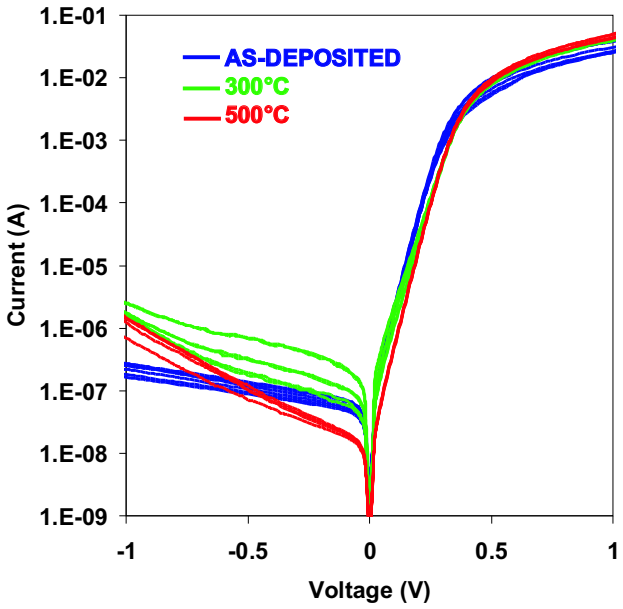

Figure 4.19: $I - V$ characteristics of Ni/Ge Schottky barriers grown under the same electrodeposition potential (-1.10 Volts against the reference electrode), having a contact area of 20 μm square, as a function of annealing temperatures. Ge resistivity was 0.005-0.02 Ω-cm.

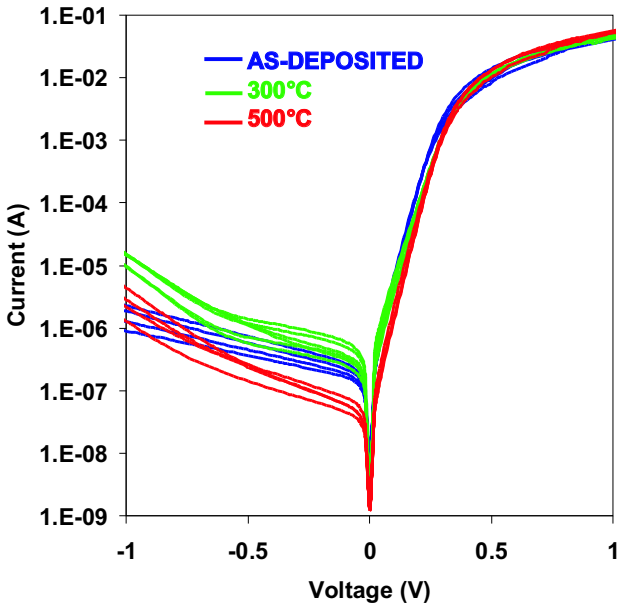

Figure 4.20: $I - V$ characteristics of Ni/Ge Schottky barriers grown under the same electrodeposition potential (-1.10 Volts against the reference electrode), having a contact area of 40 μm square, as a function of annealing temperatures. Ge resistivity was 0.005-0.02 Ω-cm.

4.6 SB-MOSFET simulation

4.6.1 Calibration of simulation to experiments

The devices were generated using Sentaurus Structure Editor and its Meshing engine. The simulator was at first calibrated by using the Schottky barrier heights and the various experimental doping densities N_d of the substrates obtained by the $C-V$ methods which were presented in Table 4.5. In order to incorporate the Fermi-level pinning effect, the metal work functions were tuned to obtain the experimental Schottky barrier heights. For example, to simulate a 0.52 eV electron Schottky barrier height the work function of the metal was taken to be 4.59 eV. Taking into account the electron affinity of 4.07 eV for Ge at 300 K, this indeed results in a barrier height of 0.52 eV.

For accuracy and efficiency of the simulator, Schottky barrier having a 1 μm square area, with 1 nm square mesh, was considered for simulation to compare with the 10 μm experimental device. This is because the current density of a Schottky barrier in the reverse bias and in the low forward bias is independent of the contact area as presented in Table 4.7.

Area μm sq	N_d=8.7×10^{14}cm^{-3}		
	J(-0.5V) A cm^{-2}	J(+0.25V) A cm^{-2}	J(+0.5V) A cm^{-2}
0.1	0.005	20.63	6841
0.5	0.005	20.63	6841
1	0.005	20.63	6841
2	0.005	20.63	6841
Area μm sq	N_d=1.45×10^{16}cm^{-3}		
	J(-0.5V) A cm^{-2}	J(+0.25V) A cm^{-2}	J(+0.5V) A cm^{-2}
0.1	0.005	34.98	6841
0.5	0.005	34.98	6841
1	0.005	34.98	6841
2	0.005	34.98	6841
Area μm sq	N_d=2.9×10^{17}cm^{-3}		
	J(-0.5V) A cm^{-2}	J(+0.25V) A cm^{-2}	J(+0.5V) A cm^{-2}
0.1	0.073	94.29	90353
0.5	0.073	94.29	90353
1	0.073	94.29	90353
2	0.073	94.29	90353

Table 4.7: Values of J obtained by numerical simulation of a Ni/Ge Schottky barrier at various bias voltages and contact area showing the area independence of J on reverse bias and low forward bias.

At high forward biases in Schottky barriers, however, the current is limited by the bulk series resistance. In order to include this effect, the bulk spreading resistance of a 10 μm square contact on a bulk (1 cm square) substrate with 400 μm thickness is calculated by a systematic 3D simulation and is presented in Table 4.8. A background resistance of $\sim$10 Ω is further included and the obtained resistance values are added as a lumped resistance to the Ni/Ge Schottky barrier under simulation.

The corresponding calculated $J-V$ curves for the various substrate doping densities are presented in Fig. 4.21 along with the experimental curves. Separation of

N_d (cm^{-3})	8.7×10^{14}	1.45×10^{16}	2.9×10^{17}
R (Ω)	57.45	3.44	0.17

Table 4.8: The bulk spreading resistance R of a 10 μm contact on a 1 cm square Ge substrate with 400 μm thickness for various N_d.

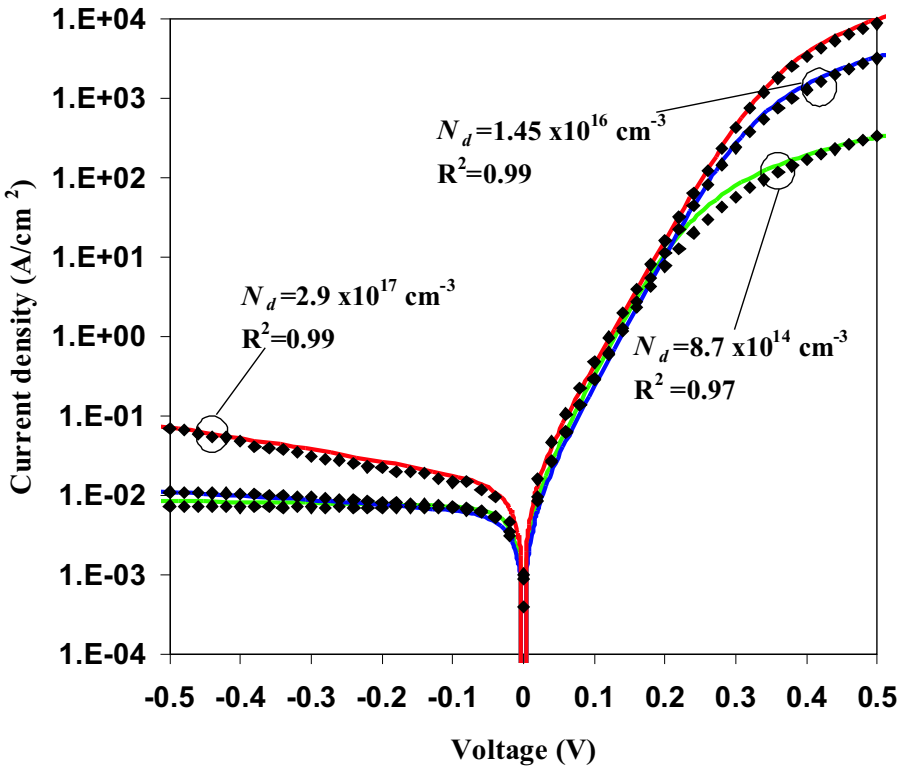

Figure 4.21: $J-V$ characteristics (solid lines) for 10 μm Ni/Ge contacts for various doping density modelled by Sentaurus Device simulator tool. The corresponding experimental curves (symbols) are also presented for reference.

the electron and hole currents in the simulation (not shown) indicates that holes play a negligible role in the reverse and forward bias currents. The concordance of the experimental and simulated current density curves at the various conditions confirms the full calibration of the simulator tool to both TE and TFE.

4.6.2 Leakage current suppression

The simulated device structure is presented in Fig. 4.22. Sentaurus Structure Editor meshing defines the Schottky junctions of a metal to semiconductor as a contact

inctead of a metal body. Therefore, for the SB-MOSFET simulation the meshing was performed accordingly. The mesh of the simulated SB-MOSFET is shown in Fig. 4.23. A summary of the nominal parameters of the device is given in Table. 4.9.

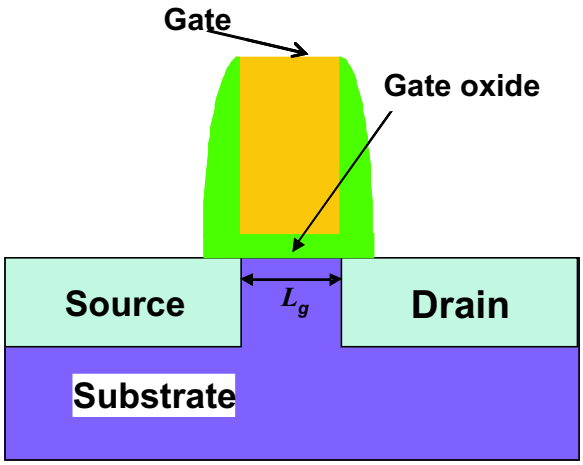

Figure 4.22: A schematic representation of the simulated SB-MOSFET. Here, source and drain are Schottky contacts.

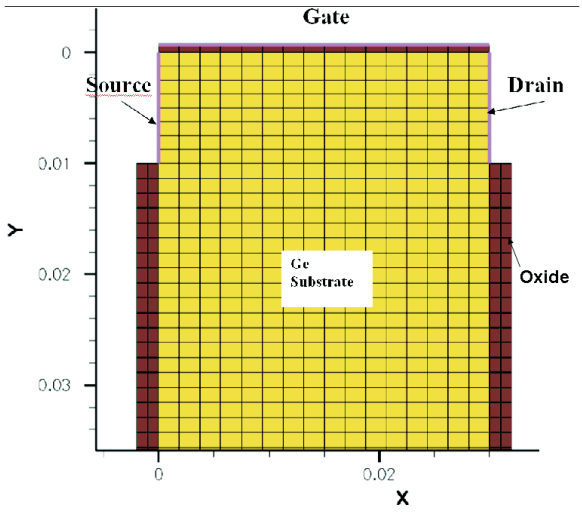

Figure 4.23: Mesh used for the simulations of a 30 nm gate length SB-MOSFET. Source and drain are Schottky contacts.

parameters	range
Gate length (L_g)	30 nm
Gate oxide (t_{ox})	0.7 nm
Body thickness	1 μm
Doping (N_d)	varied
source/drain barrier heights	tuned

Table 4.9: Nominal parameters for the simulation of the SB-MOSFET.

A typical input file for this simulation is presented below. To accurately model the SB-MOSFET a fully coupled 2D simulation, was performed that included physical models eg. band gap narrowing effect using the Slotboom model and the dependence of mobility to normal electric field using the Lombardi model.

A typical input file for Simulation of the Ge channel Schottky barrier MOSFET

```
File{
   Grid    = "s9rms2_msh.grd"
   Doping  = "s9rms2_msh.dat"
   Plot    = "s9rms2_des5a.tdr"
   Current = "s9rms2_des5a.plt"
   Param   = "bar.par"
}

Electrode{
   { Name="Anode"    Voltage= 0.0 Schottky Workfunction=4.59}
   { Name="Cathode"  Voltage= 0.0 Schottky Workfunction=4.59}
   { Name="Gate"    Voltage= 0.0 }
   { Name="Substrate"    Voltage= 0.0 }

}

Physics( Electrode="Anode") {
Recombination (eBarrierTunneling)
BarrierLowering
}

Physics( Electrode="Cathode") {
Recombination (eBarrierTunneling)
BarrierLowering
}

Physics (Material="Germanium"){
   Temperature = 300
   Mobility(DopingDep Enormal HighFieldSat)
#  Mobility models including doping dependence, high field velocity saturation
#and transverse field dependence are specified.

   EffectiveIntrinsicDensity(BandGapNarrowing (OldSlotboom))
}

Plot{eCurrent hCurrent
     eDensity hDensity Potential ElectricField
     DonorConcentration AcceptorConcentration

}

Math {
```

```
    Extrapolate
    RelErrControl
}


Math (Electrode="Anode"){
 Nonlocal(Length=20e-7)
 Digits(Nonlocal)=3
 EnergyResolution(Nonlocal)=0.001
}
Math (Electrode="Cathode"){
 Nonlocal(Length=20e-7)
 Digits(Nonlocal)=3
 EnergyResolution(Nonlocal)=0.001
}


Math {Iterations=30}

Solve {
   NewCurrentFile="init"
   Coupled(Iterations=100){ Poisson }
   Coupled{ Poisson Electron Hole}

   Quasistationary(
      InitialStep=0.01 Increment=1.35
      Minstep=1e-6 MaxStep=0.5
      Goal{ Name="Anode" Voltage=-0.5}
   ){ Coupled{ Poisson Electron Hole} }

   Quasistationary(
      InitialStep=0.01 Increment=1.35
      Minstep=1e-6 MaxStep=0.1
      Goal{ Name="Gate" Voltage=1 }
   ){ Coupled{ Poisson Electron Hole} }

   NewCurrentFile=""
   Quasistationary(
      InitialStep=0.01 Increment=1.35
      Minstep=1e-9 MaxStep=0.01
      Goal{ Name="Gate" Voltage=-1}
   ){ Coupled{ Poisson Electron Hole}}
}
```

I_d-V_g characteristics for a bulk SB-pMOSFET with channel length (L_g) of 30 nm, gate oxide thickness (t_{ox}) of 0.7 nm are calculated as a function of various N_d of Ge and are presented in Fig. 4.24.

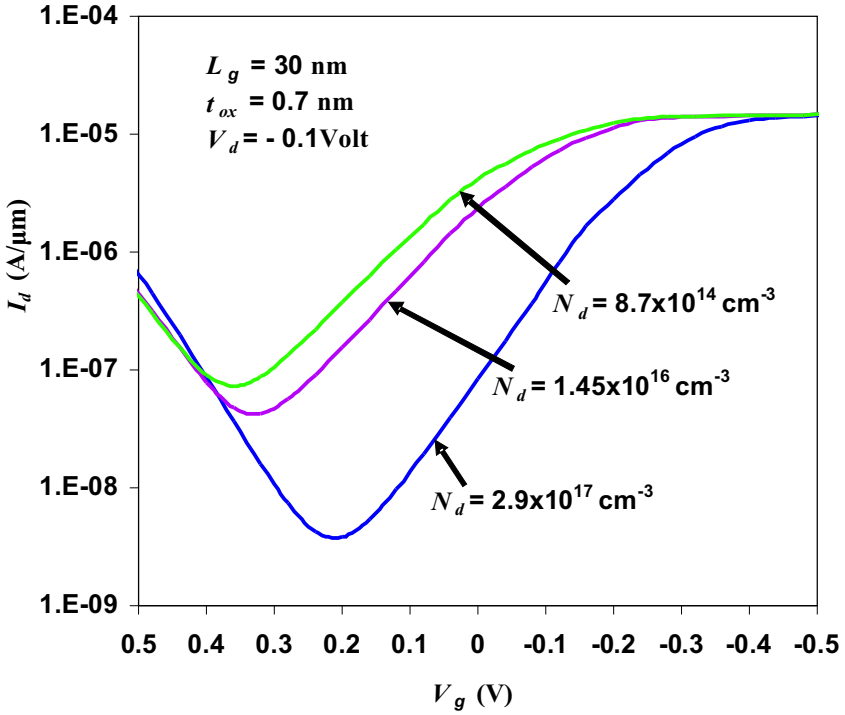

Figure 4.24: Simulated I_d-V_g characteristics of a 30 nm Ge channel bulk SB-pMOSMET showing the decrease of leakage currents with increasing substrate doping density N_d.

The source to drain subthreshold leakage current can be readily obtained from the curves at V_g=0. It is found that for a fixed V_d of -0.1 Volts the leakage current is 4.5×10^{-6} A/μm when N_d of 8.7×10^{14} cm^{-3} was used. However, the leakage current decreased to 2.1×10^{-6} A/μm and 8.1×10^{-8} A/μm when N_d was increased to 1.45×10^{16} cm^{-3} and 2.9×10^{17} cm^{-3}, respectively. Therefore, by increasing the bulk doping concentration the source to drain leakage current is reduced, at no cost of additional drain/body leakage due to the extremely low reverse bias currents in the electrodeposited Ni/Ge Schottky barriers. This technique hence could be used for low leakage SB-MOSFET on highly doped Ge.

At higher positive V_g the leakage current is observed to increase for the various N_d. This is attributed to the ambipolar behaviour typical of an SB-MOSFET that

results in GIDL-like current. For higher drain voltages eg. V_d= -1 Volt this leakage current is very high.

There are several methods available to suppress the GIDL-like leakage in SB-MOSFETs. One method uses a field-induced drain extension [49] located between the channel and the drain, which is shown in Fig. 4.25. Here, numerical simulation is performed to investigate the effect of the offset gate structure in the bulk Ge based SB-pMOSFET. The corresponding mesh of the simulated structure is shown in Fig. 4.26.

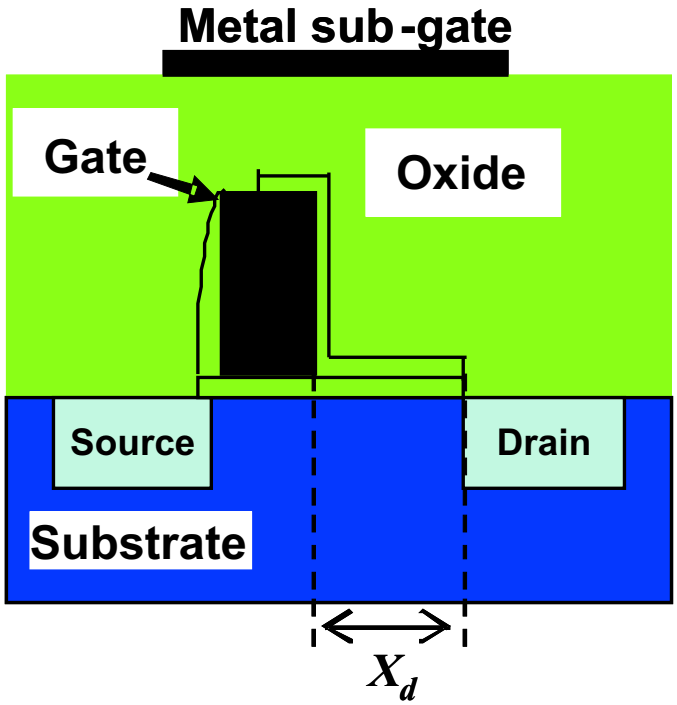

Figure 4.25: Schematic representation of the simulated field-induced drain SB-pMOSFET based on the structure described in Ref. [49]. X_d is the offset between the drain and gate edge.

I_d-V_g characteristics, with L_g= 30 nm, t_{ox} = 0.7 nm and drain offset of X_d = 30 nm are calculated for V_d=-0.1 Volt, and sub gate voltage V_{gsub}=-10 Volts as a function of various N_d and are presented in Fig. 4.27. It is observed that the ambipolar leakage current is completely eliminated by using the field- induced drain structure. The source to drain leakage is minimum for highly doped Ge.

The high supply voltage for the subgate of the field-induced drain MOSFET may not be available in electronic circuits. Therefore, as an alternative to this method

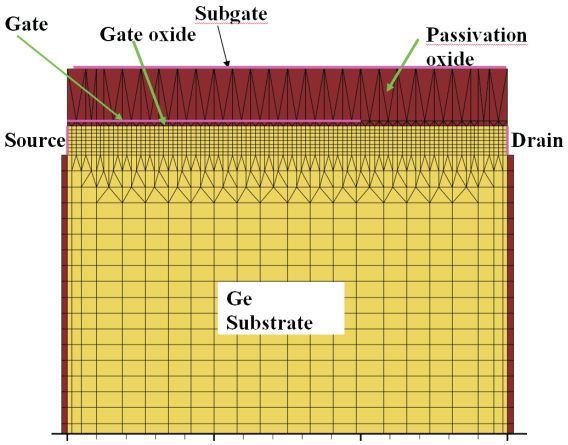

Figure 4.26: Mesh used for the simulation of the field-induced drain SB-pMOSFET as described in Fig. 4.25.

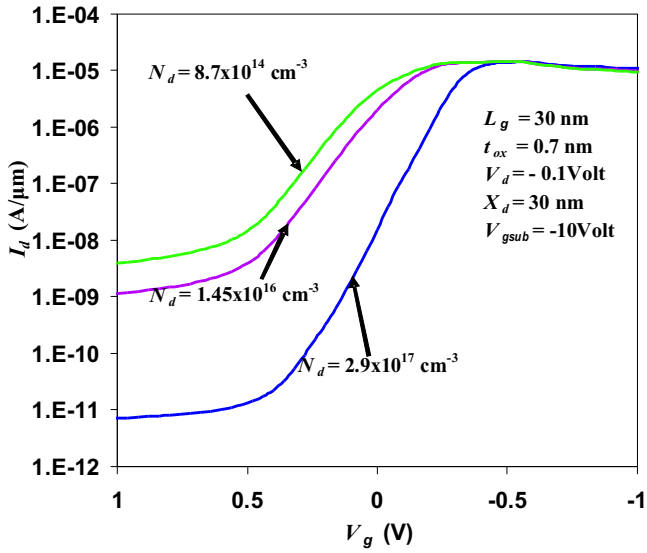

Figure 4.27: Simulated I_d-V_g characteristics of a 30 nm Ge channel bulk SB-pMOSFET with field-induced drain showing the elimination of the ambipolar leakage current.

an offset gate structure shown in Fig. 4.28a could be used for a 30 nm gate length device. Here the effect of the gate bias responsible for the hole conduction is reduced by increasing the distance (X_d) between the edges of the gate and the drain.

Here, numerical simulation to investigate the effect of the offset gate structure in the bulk SB-pMOSFET is performed. I_d-V_g characteristics, with L_g= 30 nm, t_{ox} = 0.7 nm and N_d = 2.9 $\times 10^{17}$ cm^{-3}, are calculated for V_d=-0.5 Volts, as a function of various X_d and are presented in Fig. 4.28b. It is observed that for the highly doped substrate the leakage current is extremely high for a conventional bulk SB-pMOSFET (X_d=0). As X_d is increased superior p-channel device performance is realised on the SB-MOSFET. It can be seen that not only the hole conduction is gradually eliminated but the off-state source-drain subthreshold leakage current has also decreased with increasing X_d. The parasitic resistance with increasing X_d, however, has not decreased the ON current. This is due to the domination of the source-to-channel tunnel resistance over the resistances in the current conduction path. Therefore, by using the offset-gate structure the OFF current of an SB-MOSFET could be significantly reduced without affecting the ON current of the device.

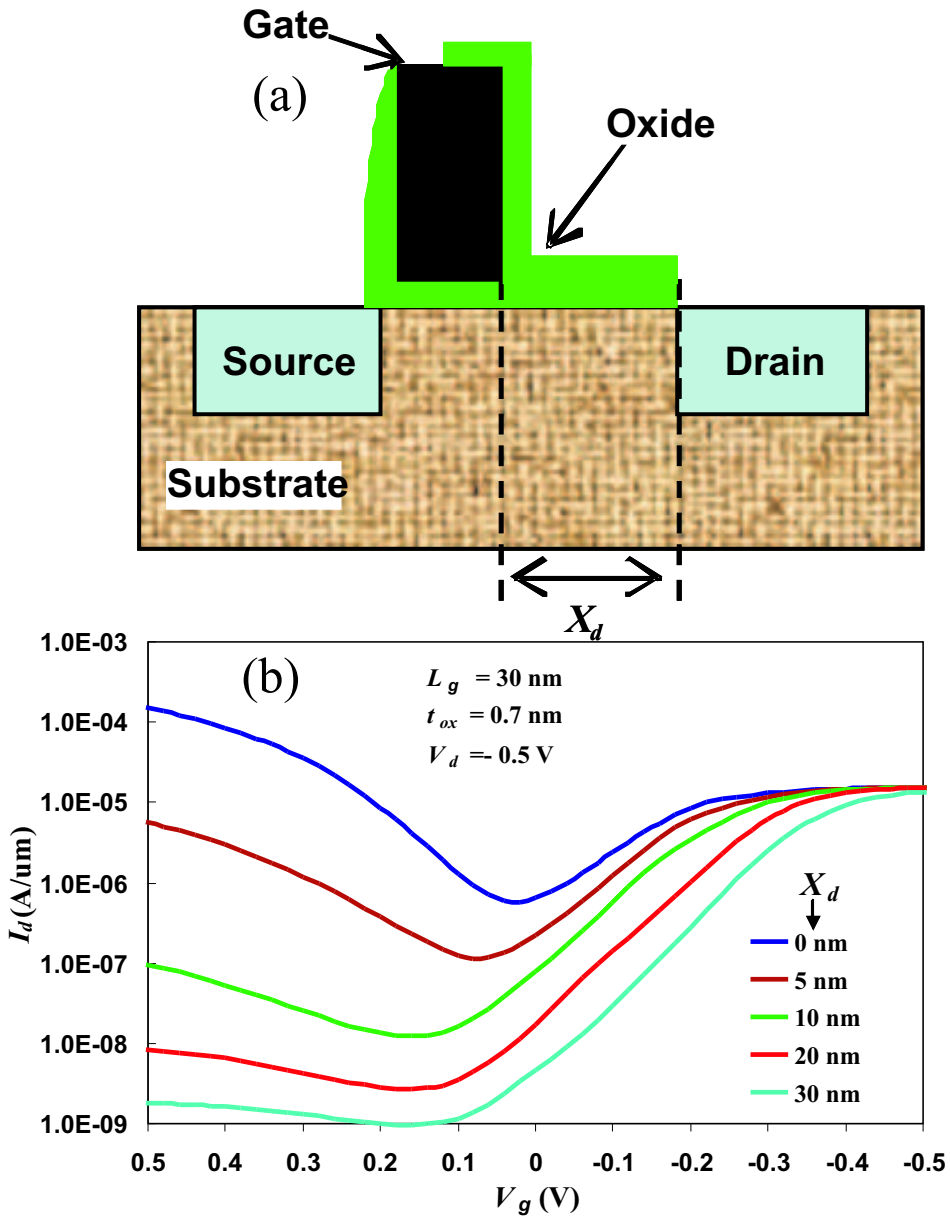

Figure 4.28: (a)Schematic representation of an SB-pMOSFET structure with gate offset. X_d is the length of offset region from the drain;(b)I_d-V_g characteristics of a 30 nm Ge channel bulk SB-pMOSFET for various X_d showing the decrease of leakage currents with increasing X_d.

4.7 Conclusions

An SB-MOSFET is a potential alternative to conventional doped source/drain MOSFETs when the source/drain scaling limit is reached. In order to overcome short channel effects in these MOSFETs a highly doped substrate could be used. However, this imposes a challenge to the conventional method of source/drain formation using physical vapour deposition techniques since increasing the substrate doping increases the leakage currents in the the source/body and drain/body junctions. Ni/Ge Schottky barriers formed by Ni electrodeposition on Ge show high rectification with low leakage current in reverse bias even for a highly doped Ge. Ni/Ge Schottky barriers transform into NiGe/Ge Schottky barriers upon annealing. Despite the compositional change, the Schottky barrier properties are virtually unaltered due to Fermi-level pinning. Therefore, these junctions could be used as source/drains in an SB-MOSFET to suppress junction leakage. The series resistance of NiGe decreases with annealing temperature which is important for high drive current in Ge based SB-MOSFETs. Based on the results found by numerical simulation, it can be concluded that the source-to-drain subthreshold leakage current in an SB-MOSFET could be minimised by using a highly doped Ge substrate, which in effect suppresses the short channel effects. An increase in the body doping would not additionally increase the drain/body leakage due to the extremely low leakage currents exhibited by an electrodeposited Ni/Ge Schottky barrier. Therefore, electrodeposition could be used for source/drain formation of a highly doped Ge-based SB-MOSFET to achieve low subthreshold leakage current.

Chapter 5

Negative differential conductance in a reverse-biased Ni/Ge Schottky barrier

In this chapter the experimental observation of negative differential conductance (NDC) in a Ni/Ge Schottky barrier diode is reported. With the aid of theoretical models and numerical simulation it is shown that, at reverse bias, electrons tunnel into the large electric field of the depletion region of the Ni/Ge Schottky barrier. This scatters the electrons into the upper valley of the Ge conduction band, which has a lower mobility. The observed NDC is hence attributed to the transferred-electron effect. This shows that Schottky barriers can be used to create hot electrons for transferred-electron devices.

The work presented in this chapter was published in IEEE Electron Device Letters, Vol.30, No.9,pp.966-968, 2009.

5.1 Introduction

The transferred-electron effect leads to negative differential resistivity in semiconductors having two-valley conduction band profile eg. in GaAs [62], InP [63] and Ge [64]. The corresponding device, known as the transferred electron device, has been extensively used in microwave circuits. Injection limited cathode contacts, in partic-

ular, graded $Al_xGa_{1-x}As$, have been used [65] instead of ohmic contacts in GaAs based devices to improve device performance. The extreme Fermi-level pinning in semiconductors hampers the use of TE mechanism over a Schottky barrier for hot electron injection [66]. Here, the first experimental observation of NDC is reported in a reverse-biased Ni/Ge Schottky barrier at low temperature and it is shown that TFE through the Schottky barrier is the mechanism.

5.2 The transferred-electron device

The transferred-electron effect is the transfer of conduction electrons from a high-mobility energy valley to a low mobility higher energy satellite valleys of particular semiconductors eg. GaAs, InP and Ge. As observed in Fig. 5.1, the conduction band main minimum in GaAs is in the Γ-point. Two other satellite valleys L and X are in the directions [111] and [100], respectively. The conduction band electrons occupy the bottom of the central valley at equilibrium. When an electric field is applied, the electrons accelerate until they collide with imperfections of the crystal lattice. As the electric field is incremented further, the mean electron energy becomes higher, and higher energy states in the conduction band can be occupied. When the electron kinetic energy reaches the intervalley transfer energy (for GaAs 0.32 eV), electrons have the additional possibility of occupying the L-valley. In the satellite valleys, the curvature in the energy vs. wave vector graph is much lower corresponding to a higher effective mass of the electrons. This leads to a decrease in the drift velocity with increasing field in a bulk semiconductor. This manifests itself as a bulk negative differential resistance.

The effect resulted in practical applications in the form of transferred-electron devices/Gunn diodes, which are used in microwave circuits. The operating principle of a Gunn diode is explained in Fig. 5.2. Consider a uniformly doped n-type GaAs sample of length L_p, biased with a constant voltage source V_O. The constant electric field in the sample is given by E_3=V_O/L_p. The electrons flow from cathode to anode with a constant velocity of v_3.

A noise process or a defect in the doping uniformity causes a fluctuation in the electron density. The fluctuation results in an electric dipole, consisting of a depletion

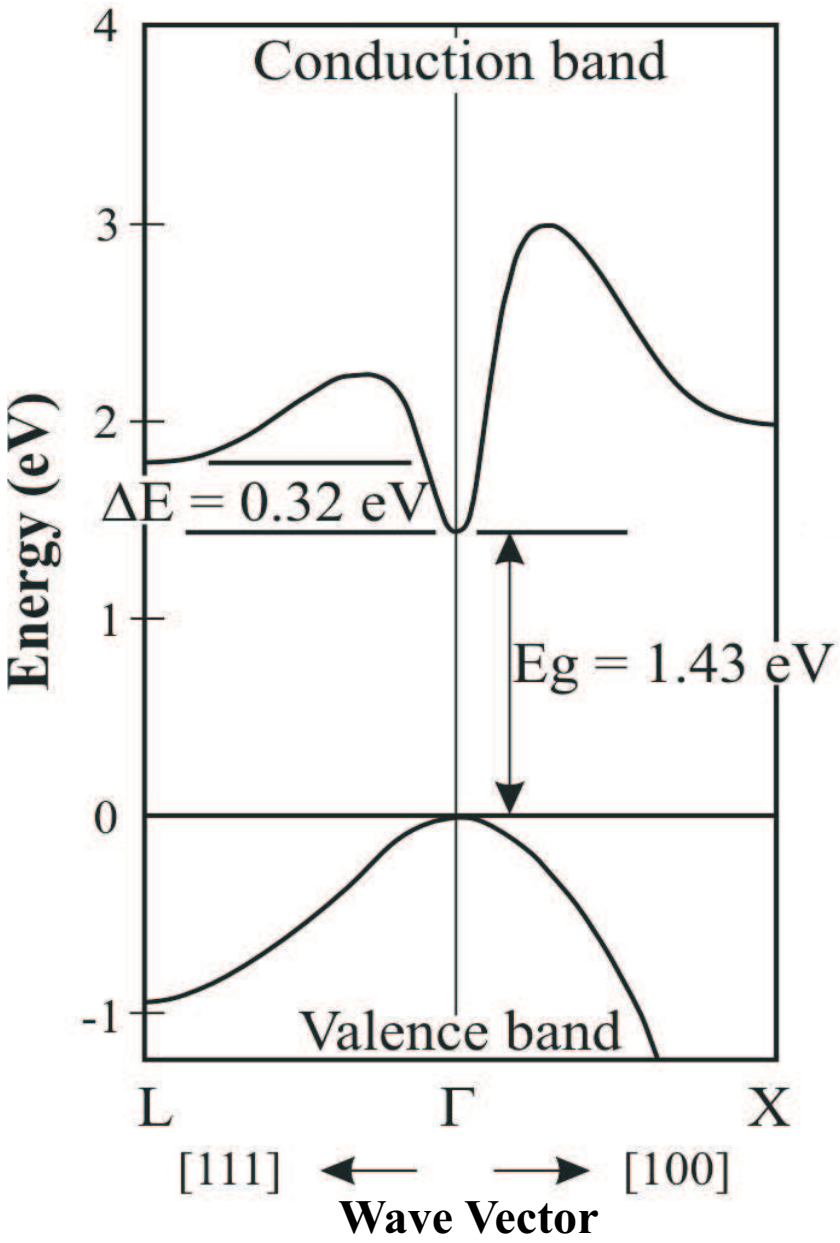

Figure 5.1: Energy band structure of GaAs (reproduced from Ref. [1]).

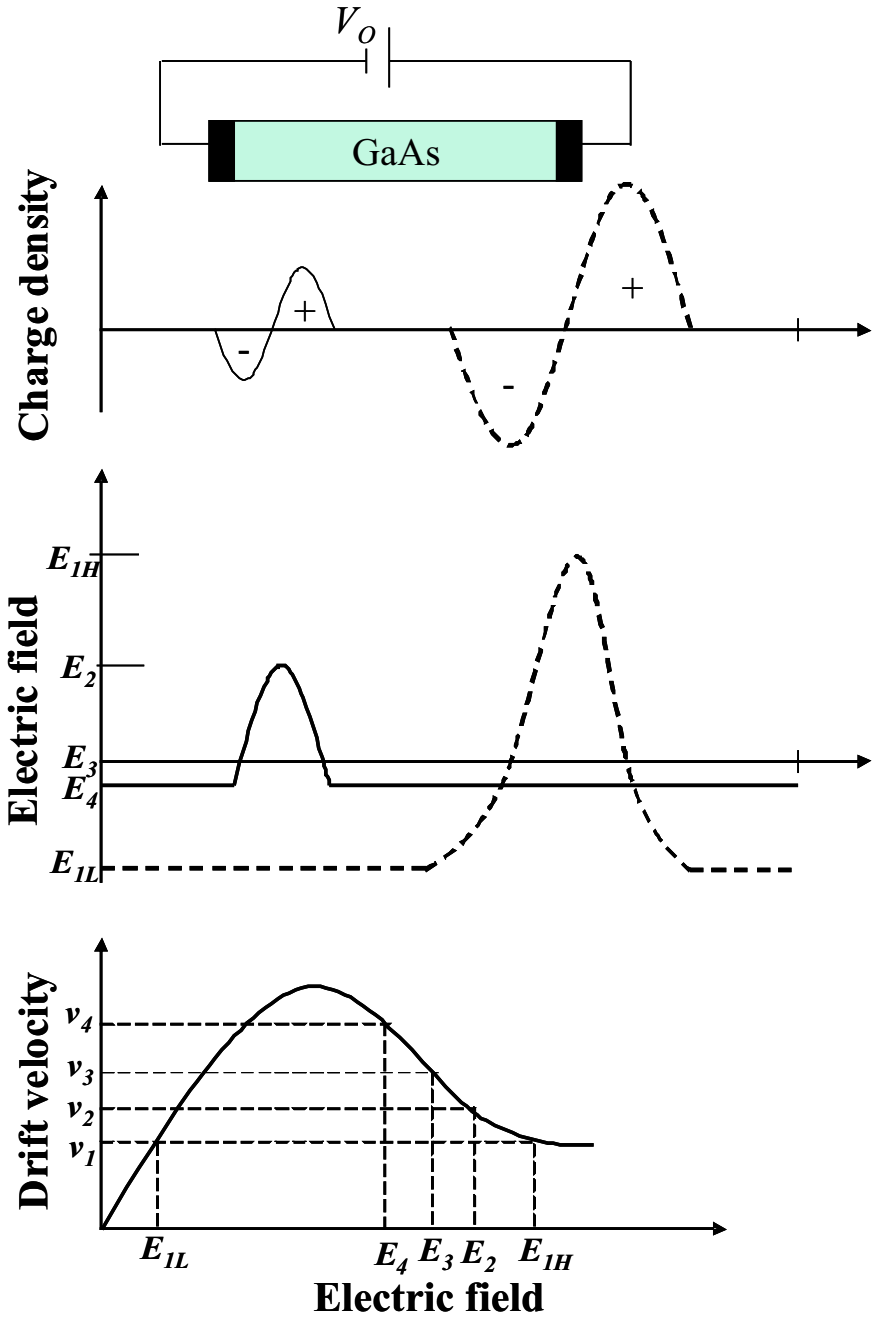

Figure 5.2: Illustration of the growth of space-charge fluctuation to a stable high field domain in GaAs (redrawn from Ref. [65]). Here, V_O is the applied voltage and v_1, v_2, v_3 and v_4 are the electron drift velocity in GaAs corresponding to the fields E_1, E_2, E_3 and E_4, respectively.

region and an accumulation region. The resulting electric field is presented as a solid line. The corresponding electron drift velocity at low field (E_4) and high field (E_2) point is v_4 and v_2, respectively with $v_4 > v_2$. Consequently, a pile-up of electrons will occur between these two points, increasing the net negative charge in that region. The space-charge region swells increasing the electric field in the domain. This dipole domain will grow while propagating towards the anode until a stable domain has been formed, which is represented by dashed curves. At this point in time, the domain has grown sufficiently to ensure that electrons at both high field and low field points move at the same velocity v_1. Therefore, the electric field in the rest of the sample falls below the threshold field and hinders formation of a second domain. The growth of the domain determines a fall in the sample current. The domain travel from the negative to positive electrode of the sample with the same velocity as the electrons in the uniform-field region outside the domain. As the high field domain disappears into the positive electrode, the field outside the domain and therefore the current through the sample, increase towards their starting values. When these values are reached, a new high-field domain starts to grow and the current decreases again. In this way periodic current oscillations and periodically propagating domains are generated.

A conventional GaAs Gunn diode consists of three epitaxial layers: a relatively low doped (n-) transit region, as the active layer, sandwiched between two highly doped (n+) contact layers which form the emitter and collector of the device (see Fig. 5.3a). During operation, a portion of the active layer is used to accelerate the electrons injected from the emitter until they have sufficient energy to be transferred into the upper L-valleys and a high field domain is created. This 'dead-zone' depends mainly on the electric field level and does not support domain formation. The dead-zone narrows the active region and introduces an undesirable positive serial resistance reducing the RF power and the efficiency of the device. To overcome this limitation, hot electron injectors (e.g. graded gap injector) are normally incorporated at the cathode. If the electron energy is equal to the intervalley energy separation, stable domains will form very near to the emitter and move across the transit region as soon as the field is high enough to sustain domain formation and propagation eliminating the dead zone formation. This is schematically shown in Fig. 5.3b. It was proposed in literature [65,67] that a Schottky barrier can serve as a hot electron injector. However,

no one has succeeded using the Schottky barrier injector because of the electron Schottky barrier heights of GaAs to most metals are much higher than the intervalley separation in its conduction band. In the next sections, the first experimental evidence that Schottky barriers can indeed be used to create hot electron injectors will be shown.

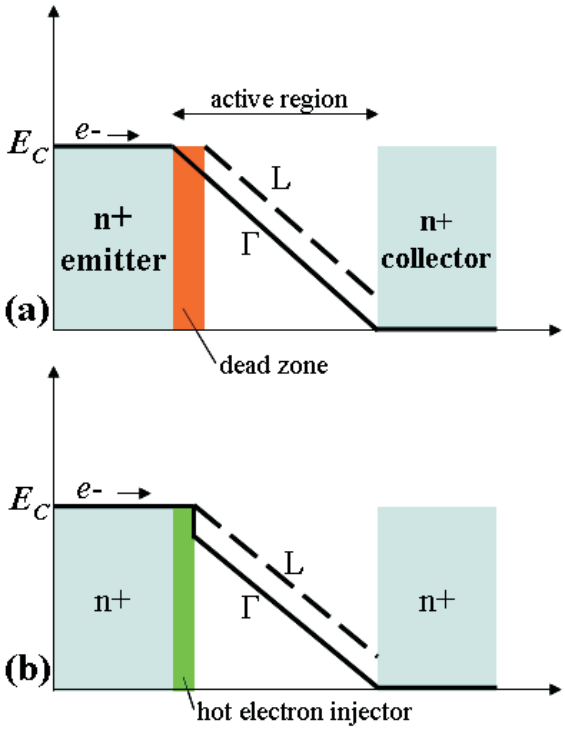

Figure 5.3: Schematic representation of the (a) normal electron injection producing a 'dead zone' and (b) hot electron injection eliminating the 'dead zone' in a Gunn diode. Here, GaAs conduction band valleys are represented by Γ and L.

5.3 Electrical characteristics of Ni/Ge diode

Room temperature current density J-V characteristics of a Ni/n+Ge Schottky barrier are shown in Fig. 5.4. For comparison, the J-V curve of a Ni/nGe Schottky barrier is presented in which TE is the dominant transport mechanism. By extrapolation from the exponential forward bias region, a Schottky barrier height ϕ of 0.53 eV is obtained. Taking the image force lowering and the substrate doping density N_d of $8.7\times10^{14}\text{cm}^{-3}$ (obtained by $C-V$ method [68]) into account, the theoretical

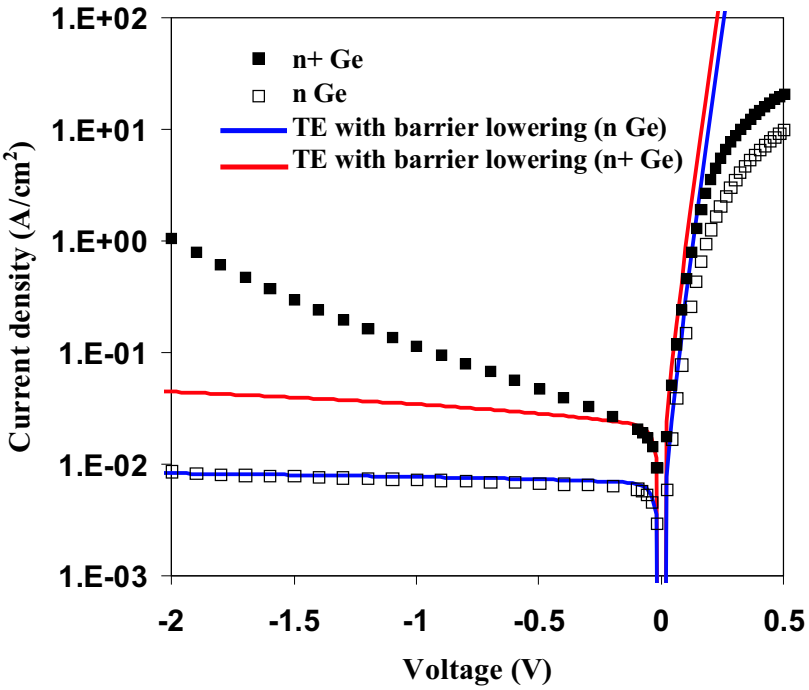

Figure 5.4: Room temperature $J-V$ characteristics of electrodeposited Ni/n+Ge and Ni/nGe contacts. Theoretical models using the Schottky barrier height extracted from the forward bias characteristic are also shown.

fitting characteristic is shown as a solid line in Fig. 5.4. For the Ni/n+Ge contact, excess current is evident in the reverse bias. The theoretical TE characteristic of this diode considering barrier lowering was calculated using a substrate doping density of $2.9\times10^{17}\text{cm}^{-3}$ (obtained by $C-V$ method) and a barrier height of 0.52 eV (obtained by $J-V$ method). Although a significant increase in current is caused by image force lowering, it is not enough to explain the excess currents for n+Ge. The above considerations suggest TFE as the dominant transport mechanism at electrodeposited Ni/n+Ge Schottky barriers. In order to investigate the TFE of the Ni/n+Ge contact at low temperatures, $I-V$ measurements were performed down to 50 K. In order to validate the repeatability of the results, four devices were tested on different samples, which were grown under the same experimental conditions. $I-V$ measurement results of two Ni/Ge Schottky barriers on sample #1 and sample #2 will be considered. For clarity, only five $I-V$ curves measured on an Ni/Ge Schottky barrier on sample #1 are plotted in Fig. 5.5a. As the temperature was reduced, the change in the

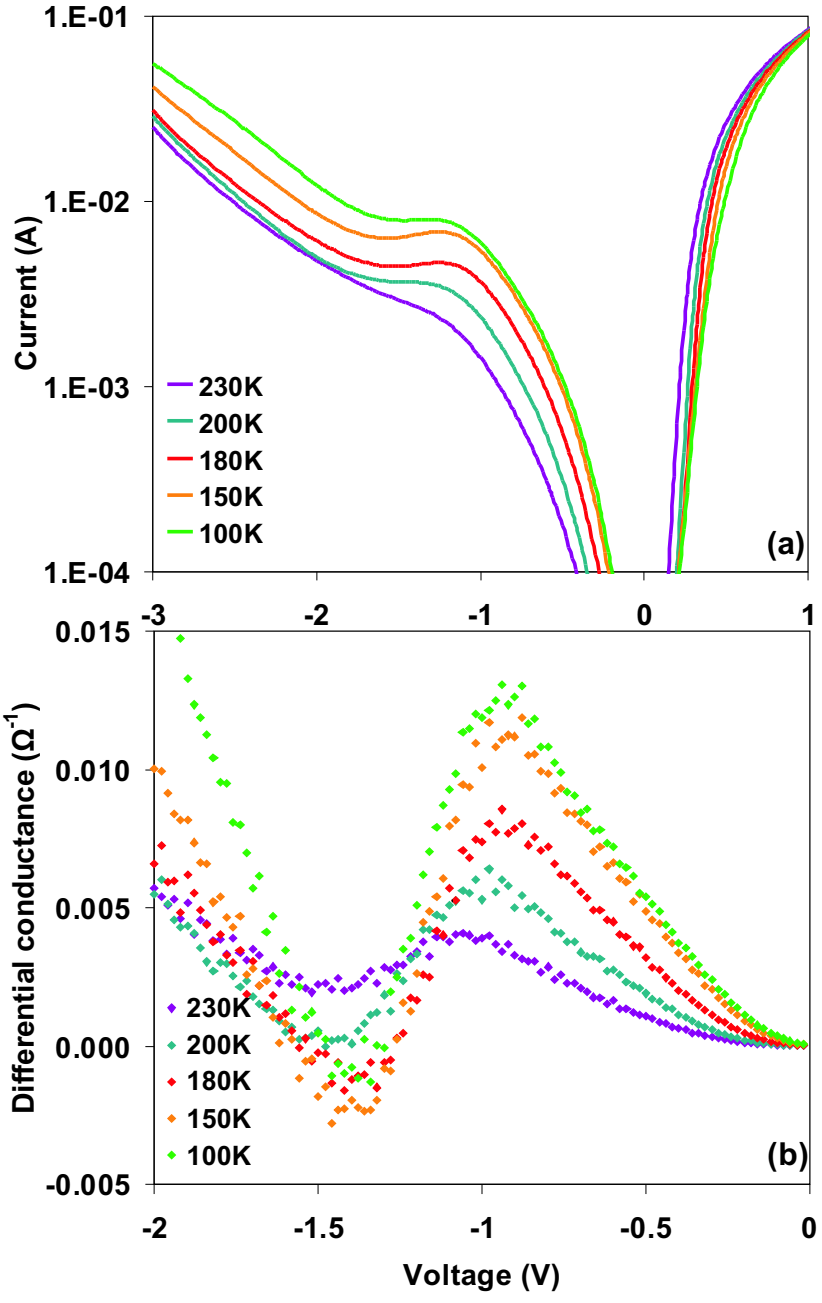

Figure 5.5: (a) $I-V$ characteristics measured at low temperatures for an electrodeposited Ni/n+Ge Schottky barrier on sample #1. The substrate doping density was $2.9\times10^{17}\text{cm}^{-3}$. The Schottky barrier contact area is 400 μm square. (b) The corresponding differential conductance as a function of voltage for various T.

saturation current in the forward bias was insignificant. This is in agreement with the TFE model for a highly doped semiconductor [35]. However, in the reverse bias an unusual current conduction mechanism at low temperature is observed. At biases in the range of -1 to -1.5 Volts, the effect of NDC is revealed for $T \leq 200$ K. From the $I - V$ curves in Fig. 5.5a the differential conductance was calculated for each bias voltage and is plotted as a function of T in Fig. 5.5b. A small but clear indication of NDC is observed at $T \leq 200$ K and at reverse bias voltage of $\sim$1.5 Volts.

In Fig. 5.6a, low temperature I-V characteristics are presented which were measured on an Ni/n+Ge Schottky barrier on sample #2. The change in saturation current in the forward bias with change in temperature is insignificant, which is very similar to the observed behaviour for the device in sample #1. Again a clear indication of NDC in the reverse bias is observed in Fig. 5.6b at $T \leq 200$ K and at reverse bias voltage of $\sim$1.5 Volts.

To exclude a bulk NDC effect, the application of similar applied biases ($\sim$ 1.5 Volts) in a bulk Ge substrate is investigated as in the Ni/Ge Schottky barriers. Back-to-back ohmic contacts of Au-Sb were deposited on the Ge substrates followed by annealing under the same condition as for ohmic contacts of the Schottky barriers. Electrical measurements at low temperatures (shown in Fig. 5.7) revealed the absense of any NDC in the bulk Ge.

The observed NDC in the Ni/nGe Schottky barrier is attributed to an intervalley or intersubband electron transfer to a low mobility band in Ge. The intersubband spacing (shown schematically in Fig. 5.8) between the L-point and the X-point minima of the Ge conduction band is 0.18 eV [69]. The X-point minimum is characterised by a lower mobility (heavier effective mass). Therefore, any scattering to this minimum would exhibit NDC. To gain enough energy for this transfer a high electric field is required, which in our case is supplied by the depletion region of the Ni/n+Ge Schottky barrier in reverse bias. The control sample did not show any NDC due to the applied field ($\sim$37 V/cm) being much lower than the threshold field (2.3 KV/cm at 77 K [1]) for a transferred-electron effect in Ge. It is also noted that NDC has been observed in Schottky barrier based MOSFETs due to the existence of gate-oxide charge traps [70, 71] but this explanation is not relevant to our device.

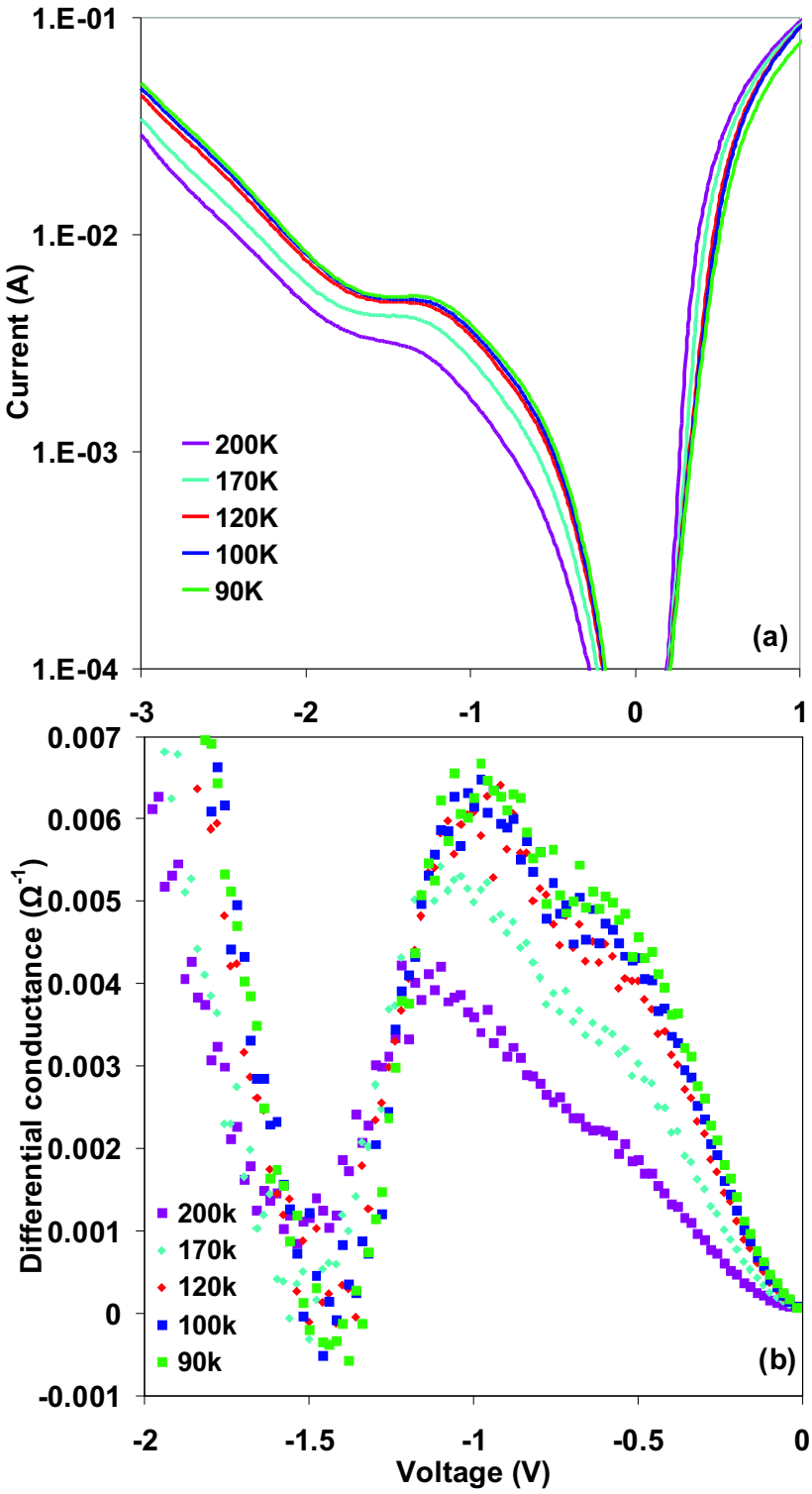

Figure 5.6: (a) $I-V$ characteristics measured at low temperatures for an electrodeposited Ni/n+Ge Schottky barrier on sample #2. The substrate doping density was $2.9\times10^{17}\text{cm}^{-3}$. The Schottky barrier contact area is 400 μm square. (b) The corresponding differential conductance as a function of voltage for various T.

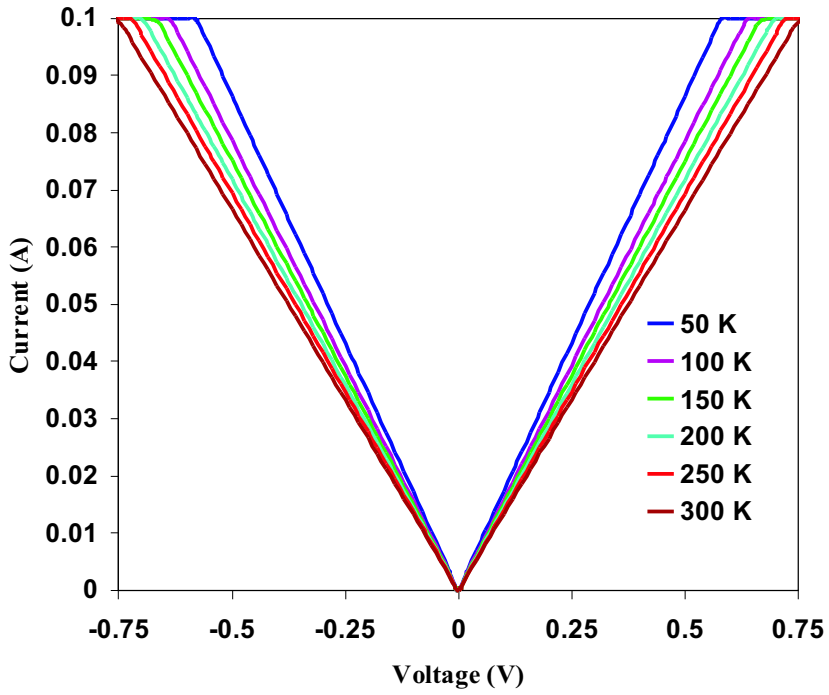

Figure 5.7: Temperature dependent $I - V$ characteristics of back-to-back ohmic contacts made on Ge substrate showing the absense of NDC in the bulk.

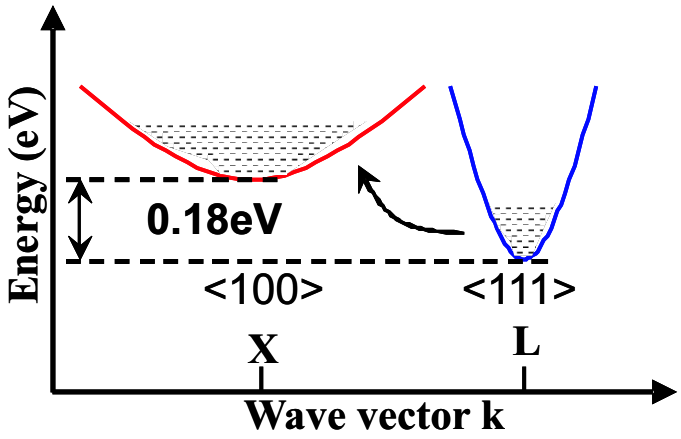

Figure 5.8: A schematic representation of the conduction band of Ge showing the minima at the X (high energy, low mobility) and the L (low energy, high mobility) band.

5.4 Calculation of the energy of tunneling electrons

To determine the excess energy of the tunneling electrons in the reverse biased Schottky barrier, the distribution of electrons is calculated. This distribution is given by the product of the probability P of a triangular barrier being penetrated by an electron with energy above the metal Fermi level E and the probability of finding an electron at that energy. The tunneling probability P, calculated assuming the WKB approximation, is given by [48]

$$P(E) = \exp\left\{\frac{-\frac{2}{3}(\phi - E)^{3/2}}{E_{00}(\phi - V - \xi)^{1/2}}\right\} \tag{5.1}$$

where ξ is the depth of the Fermi level below the conduction band and E_{00} is given by

$$E_{00} = \frac{\hbar}{2}\sqrt{\frac{N_d}{m^*\epsilon}} \tag{5.2}$$

where m^* is the effective mass of electrons and ϵ the static dielectric constant of semiconductors. The electron distribution is given by the Fermi equation

$$F(E) = \frac{1}{1 + \exp\left(E/kT\right)} \tag{5.3}$$

where k is the Boltzmann constant. The peak of the distribution given by the product of $P(E)$ and $F(E)$, at various bias voltages and temperatures, gives the most probable energy E_m of tunneling electrons. Typical distribution obtained by such multiplication for various temperatures and at a reverse bias of 1 Volt is presented in Fig. 5.9.

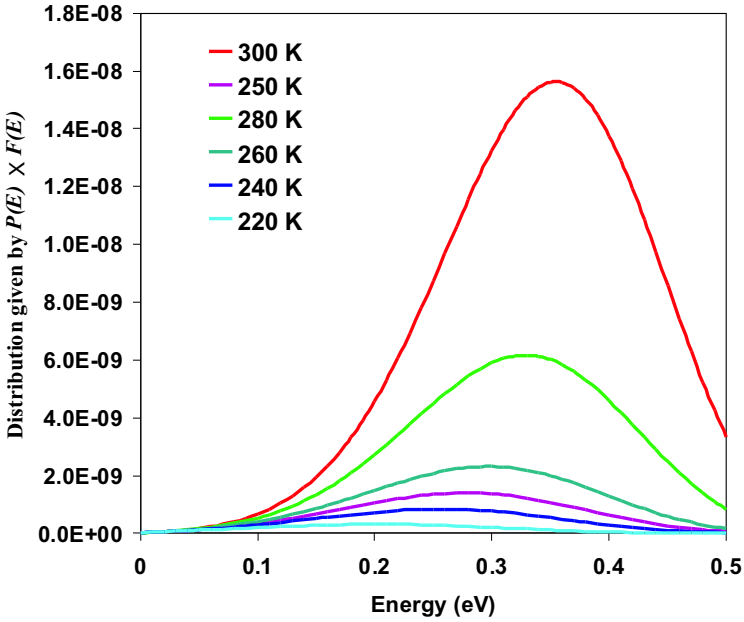

Figure 5.9: Typical energy distribution given by the product of $P(E)$ and $F(E)$ for various temperatures for a Ni/Ge diode when a 1 Volt reverse bias is applied. The peaks represent the corresponding most probable energy E_m of tunneling electrons for various temperatures. Here, a substrate doping density N_d of $2.9\times10^{17}\text{cm}^{-3}$ was considered.

The obtained values of E_m are plotted in Fig. 5.10 as a function of temperature for various reverse biases. A relative transverse effective mass of 0.08 [69] for <111>-valley conduction electrons in Ge was used for the calculations. At the reverse bias of 1.25 Volts, for example, the peak energy E_m occurs at ∼0.18 eV and ∼0.04 eV for temperatures of 230 K and 180 K, respectively. These distribution functions are shown schematically in Fig. 5.11.

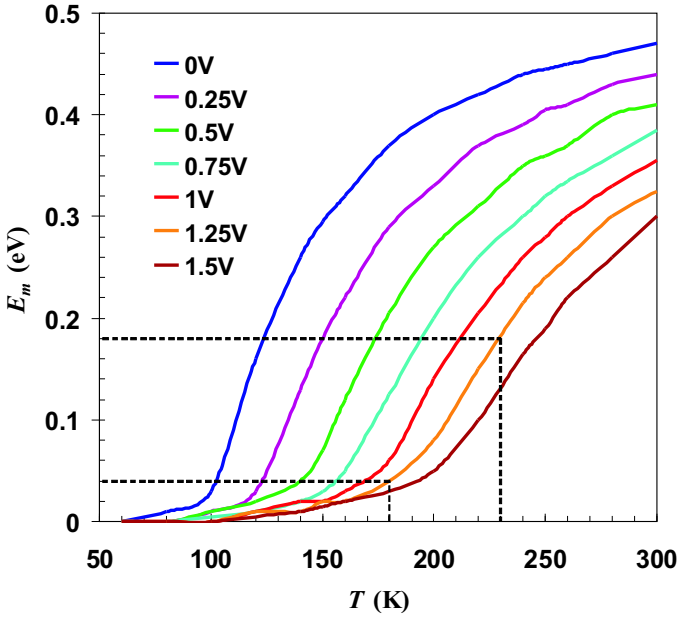

Figure 5.10: Calculated most probable energy E_m of tunneling electrons vs. T for various reverse bias voltages applied to a Ni/Ge Schottky barrier. Here, a substrate doping density N_d of $2.9\times10^{17}\text{cm}^{-3}$ was considered.

The conduction band at the depletion region in a reverse biased Ni/n+Ge Schottky barrier was calculated using the commercial TCAD simulator Sentaurus Device. The effect of image force barrier lowering and band gap narrowing has been taken into account. The calculated conduction band energy in the Ni/Ge Schottky barrier at a reverse bias of 1.25 Volts is presented in Fig. 5.11.

Following the previous calculations, TFE occurs at an energy of 1.43 eV (1.25 + 0.18) at 230 K. Upon tunneling, the injected electrons (represented by point A in Fig. 5.11) will be thermalised after traveling a distance of a mean free path λ and belong to either the upper valley or the lower valley depending upon the energy of electrons. As an approximate estimation, we assume for this distance a phonon mean free path ($\simeq 105\mathring{A}$) [1]. The injected electrons experiences a depletion field $\mathscr{E}$ of 2.8×10^5 V/cm at point A. Therefore, electrons of most probable energy, which tunnel at an energy level 1.43 eV, will have energy of $\lambda\mathscr{E}$= 0.28 eV upon thermalisation (point B). Similarly, electrons tunneling at 180 K (point A') will have an energy of 0.26 eV upon thermalisation (point B'). These hot electrons could easily undergo intervalley scattering of 0.18 eV and thereby exhibiting NDC in the Ni/Ge Schottky

diode. The electric field in the bulk n+ region at 1.5 Volts reverse bias, calculated to be $\sim 5\times10^{-5}$ V/cm, is low enough to exclude the onset of transferred electron effect from the bulk. The increasing trend in current at reverse-biases larger than 2 Volts observed in Fig. 5.5a can be attributed to the fact that the lower valley of the conduction band, after the onset of NDC, has a very low population of carriers, and the current is increasing with applied bias mainly due to the relatively slow drifting carriers in the upper valley of the conduction band as explained in literature [72].

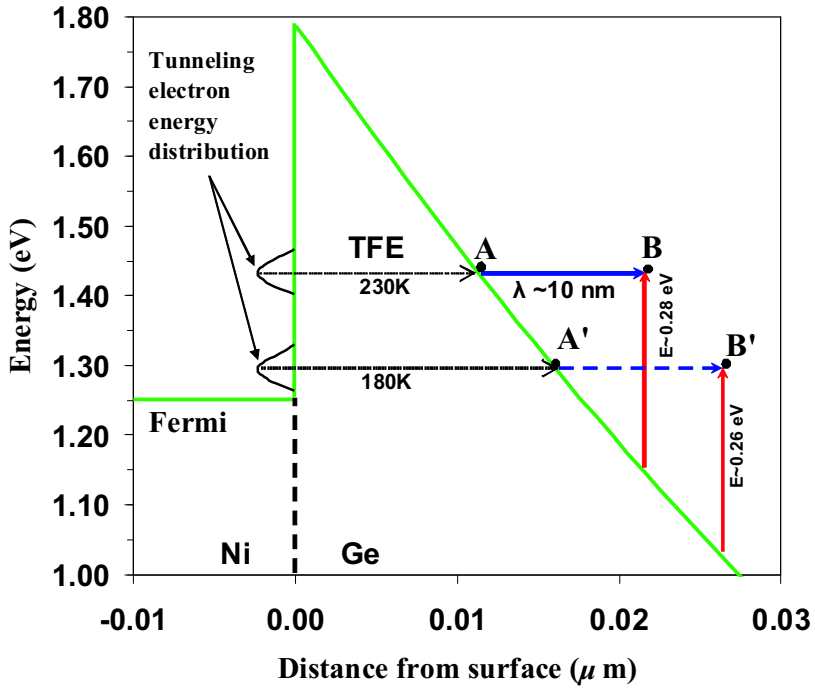

Figure 5.11: Conduction band profile obtained by numerical simulation of a Ni/Ge Schottky barrier at a reverse bias of 1.25 Volts. Here, a substrate doping density N_d of 2.9×10^{17}cm^{-3} was considered. The TFE mechanism is schematically shown at 230 K and 180 K. A, B and A', B' are the energy of a tunneling electron at 230 K and 180 K, respectively, immediately, and after thermalisation.

At NDC the Ni/n+Ge Schottky barriers show current density of $\sim$1-5 A/cm^2 (from Fig.5.5a). This needs to be many orders of magnitude higher to be useful for Gunn device applications. One way to increase the reverse bias current density could be the growth of a thin ($\sim$2 nm) heavily n-doped (1×10^{20}cm^{-3}) δ-Ge layer at the Ni/Ge interface. The simulation results (presented in Fig. 5.12) show that this could increase the current density by up to five orders in magnitude.

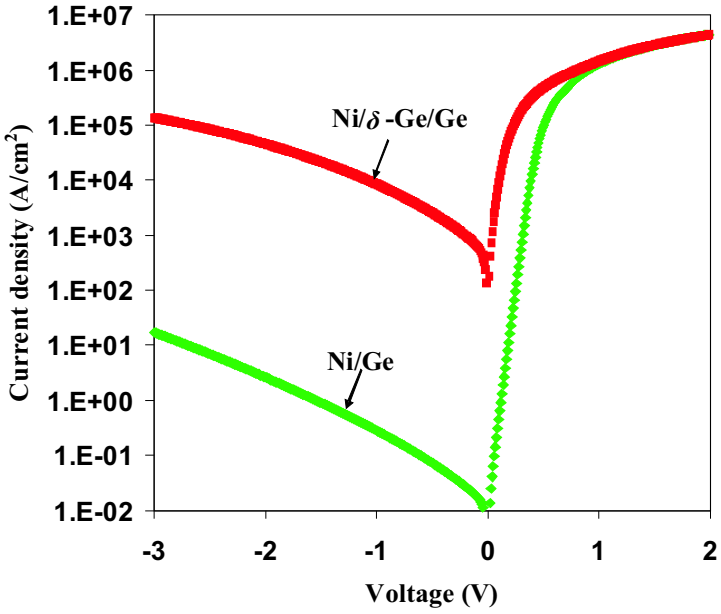

Figure 5.12: Simulated J-V characteristics of a Ni/Ge Schottky barrier with a thin (2 nm) heavily n-doped (1×10^{20}cm^{-3}) δ-Ge layer at the Ni/Ge interface showing the increase in reverse current density over the regular Ni/Ge Schottky barrier.

5.5 Conclusions

The first experimental observation of NDC in a reverse biased Ni/Ge Schottky barrier is reported. This Ni/Ge Schottky barrier was fabricated on a highly n-doped Ge by electrodeposition technique. At reverse bias, electrons with most probable energy are injected into the depletion region of the Schottky barrier where they are driven by the high depletion field into a low mobility higher energy conduction band valley in Ge. This results in the observed NDC behaviour of the Schottky barriers. The observed effect is particularly important for hot carrier injection in Gunn diodes. The TFE mechanism through an Schottky barrier can be used for hot electron injection in Gunn diodes as opposed to the conventional Gunn diodes where the carrier injection is performed using the TE mechanism over a graded gap injector. The relatively lower Schottky barrier heights on Ge as opposed to GaAs or InP would generate relatively higher current injection in a Schottky-based Gunn device. However, since the bulk material parameters of the semiconductor determine the performance potential of a Gunn device and the electron drift velocity in Ge is lower than that in GaAs and

InP [1], Ge may not be suitable for application in Gunn devices. Instead, an Schottky barrier injector on GaAs or InP could result in high performance Gunn devices. Moreover, an Schottky barrier injector is simpler to fabricate than a graded gap injector, which is typically used in conventional Gunn diodes. The results presented in this chapter hence could have an impact on the design of Gunn diodes.

Chapter 6

Electrical spin injection and extraction in Si using Schottky barriers

Schottky barriers formed between ferromagnetic metal and semiconductor are of particular interest for spin injection and detection experiments. Here, a brief review of the mechanism underpining electrical spin injection and extraction in semiconductor is presented. Then electrical spin polarised carrier injection and extraction in Si has been investigated using a Co/Si/Ni vertical structure built on a 250 nm thick Si membrane. I-V measurements performed on the devices at low temperatures showed evidence of the conduction being dominated by TFE mechanism, which is believed to be the key to spin injection using a Schottky barrier. This, however, proved inconclusive as the devices did not show any magnetoresistance signal even at low temperatures. This is attributed partially to the high resistance-area product in the Schottky barriers at spin injection biases. The potential of this vertical Spin-device for future experiments is shown by numerical simulation. The results reveal that by growing a thin highly doped Ge layer at the Schottky junctions the resistance-area products could be tuned to obtain high magnetoresistance.

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6.1 Introduction

The inclusion of semiconductors in spintronics is of particular interest as it would imply compatibility with conventional electronics and introduction of non- linear effects, which are essential for active devices. The generation, preservation, modulation and detection of spin polarised current in non-magnetic semiconductors are very important milestones towards this goal. In order to make a spintronic device, the primary requirement is to have a system that can generate a current of spin polarised electrons, and a system that is sensitive to the spin polarisation of the electrons. The simplest method of generating a spin polarised current is to inject the current through a ferromagnetic material. An example of such application is the GMR device. A typical GMR device consists of at least two layers of ferromagnetic materials separated by a spacer layer. When the two magnetisation vectors of the ferromagnetic layers are aligned, electrical current will flow freely, and the resistance of the system is low, whereas, if the magnetisation vectors are antiparallel, the resistance of the system is higher. GMR devices have been extensively used in data storage applications. The success of this all-metal structure enhanced the interest in semiconductor spintronics. The fundamental requirements for successful implementation of a semiconductor spin transistor are efficient electrical injection of spin polarised carriers from an appropriate contact into the semiconductor, adequate spin diffusion lengths and lifetimes for transport within the semiconductor medium, effective control/manipulation of the spin carriers to provide the desired functionality, and spin selective extraction of carriers to provide the output. Once the spin polarised carrier is injected, spin polarisation must be largely preserved while the spin current undergoes propagation through the device. Moreover, in order for the extraction of spin polarised current from the semiconductor after spin injection, layers must be thinner than the spin diffusion length of electrons in the semiconductor channel. One advantages of semiconductors is that the spin diffusion length is much higher than metals. Gregg *et al.* [73] determined that the spin diffusion length in Si is greater than 64 μm. The spin polarisation of the carriers may be manipulated for proper functionality of the device eg. improving gain of spin transistor. Modulation of the spin-polarised current in the semiconductor can be achieved either by conventional means (e.g. control of the carrier concentration in the semiconductor channel) or by spin effects such as

spin-orbit interaction as demonstrated theoretically by Datta and Das [13].

6.2 Spin injection and extraction in a semiconductor

The primary requirement for realising a spin transistor is the injection of spin polarised carriers from a magnetic contact to a nonmagnetic semiconductor. Fig. 6.1a presents a density of states diagram for a simplified band picture of the 3d band of a transition metal ferromagnet like Ni, Co or Fe. The two spin sub-bands are shifted by their exchange energy. This exchange splitting of the electron conduction bands presents different parts of the band structure to the Fermi energy and these different band structure segments generally have different densities of states. Current transport involves electrons within a thermal energy range, $E_F \pm kT$, it is obvious that an electric current will be carried by electrons from a single spin sub-band. This implies that the current within the ferromagnet is spin polarised. Generally, any transport current entering a nonmagnetic metal or semiconductor from a ferromagnetic metal would be spin polarised. The spin injection experiment of Johnson [74] was the first empirical demonstration of this generalisation, which is shown schematically in Fig. 6.1b.

The process of spin injection mentioned above is not very straight forward in semiconductors and suppressed in the case of ohmic contacts. The conductivity mismatch problem for electrical spin injection from a ferromagnet to a semiconductor ohmic contacts arises as the spin dependent resistance of the ferromagnet up to its spin flip length is very much lower than the spin independent resistance of the semiconductor up to its spin diffusion length. Once injected at the interface the spin up and spin down currents lose their polarisation since the resistance offered to them by the semiconductor is the same and spin independent. The effect was modelled by Schmidt *et al.* [76, 77] on a system composed of a 2-dimensional electron gas (2DEG) semiconductor sandwiched between two ferromagnets. They showed that for a certain current polarisation in a semiconductor only a potential difference between the two spin channels, having the same conductivity at the interface, can cause different current densities (eg. of the order of μA) in the channels. In order to obtain the same potential difference at the interface a very high current density (eg. of the order of

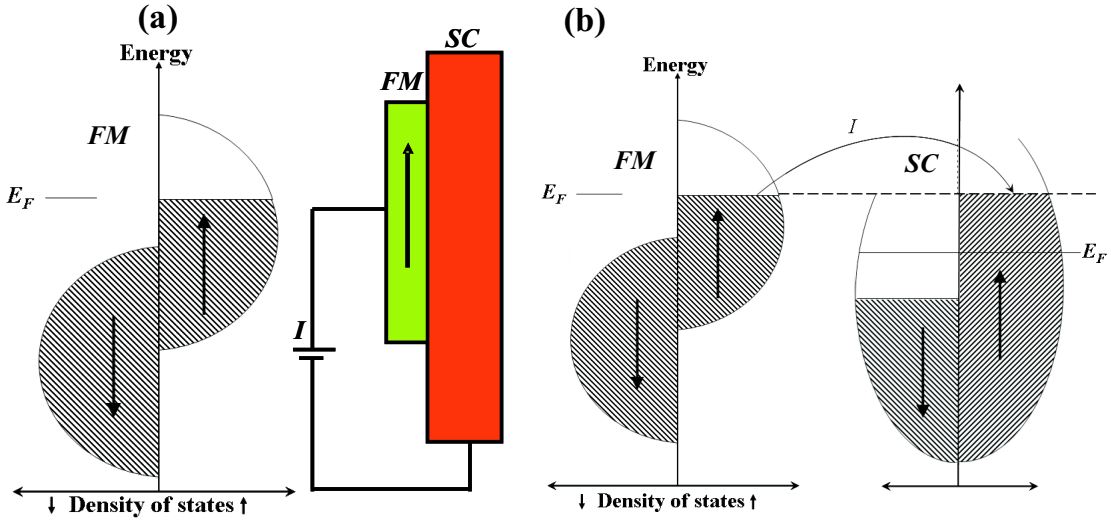

Figure 6.1: (a) Density of states diagram for a simple band model of a transition metal ferromagnet represented by *FM*.(b) Spin injection results in a non-equilibrium magnetisation in a nonmagnetic semiconductor *SC*, when current *I* is driven into it from *FM* (Redrawn from Ref. [75]).

mA) in the ferromagnet is required. Taking current conservation into account this cannot happen since the same current is flowing through both the semiconductor and the ferromagnet. As a solution to the conductivity mismatch problem for spin injection, the following techniques have been proposed:

Dilute magnetic semiconductors: A large difference in resistance between the spin-up channel and the spin-down channel can only be realised if the spin polarisation is close to 1. In this case, the spin channel with the lower resistance carries almost all the current, while the other spin channel acts like a barrier. Ideally, these conditions can be achieved by using a material that is fully spin polarised. One class of materials, which allows for such a high spin polarisation, is the dilute magnetic semiconductors. A dilute magnetic semiconductor is a semiconductor that contains a certain percentage of magnetic ions, usually Mn. In the absence of a magnetic field the conduction band and the valence band states are degenerate for two spin directions and the charge carriers are unpolarised. When an external field is applied at low temperatures, the conduction band and the valence band exhibit a giant Zeeman-splitting as schematically shown in Fig 6.2a. This splitting in the conduction band guarantees a spin polarisation of almost 100 %. Dilute magnetic semiconductors are thus good candidates as spin aligners, as cause the alignment of the spins of all passing electrons

to that of the lower Zeeman level (schematically shown in Fig 6.2b). Moreover, a dilute magnetic semiconductor provides a good sharp interface with semiconductors for spin injection. However, a downside is that the external field required for the Zeeman splitting is very high (in Teslas) and high spin polarisation is achieved at very low temperatures ($< 10K$) [78] and no polarisation is achieved at room temperature.

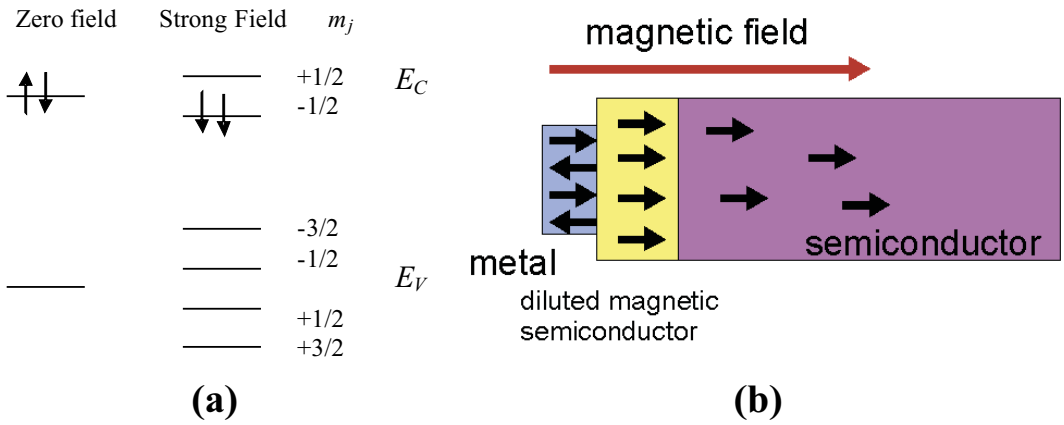

Figure 6.2: (a) Zeeman splitting in a typical dilute magnetic semiconductor. At zero field the electron spin states are degenerate. At strong field the energy splitting of the spin state occurs. The quantum states m_j for the valence band and conductin bands are shown schematically. (b) A schematic representation of a dilute magnetic semiconductor as a spin aligner between a ferromagnetic metal and a semiconductor.

Tunnel contacts: Tunnel barriers with a magnetic material on one side of the barrier are suitable as interface resistance that introduce a large resistance with a high spin asymmetry. The conductance of such a contact is proportional to the product of densities of states at the Fermi-level on both sides of the barrier. Due to the different densities of states in the spin sub-bands in a ferromagnet, the tunnelling rates from the ferromagnet to the semiconductor are different for the two spin sub-bands. Therefore, the tunnel barrier represents a spin dependent resistance and such a barrier can be used as a contact for spin injection. Spin injection by Al_2O_3 tunnel barriers has been successfully shown by Motsnyi *et al.* [79] and Jonker *et al.* [80]. The observed spin polarisation was 9% and 10 % at 80 K in GaAs and Si, respectively.

Al_2O_3 tunnel barriers are amorphous [81]. It was predicted that crystalline tunnel barriers may give rise to higher tunnel spin polarisations [82]. One such tunnel barrier is MgO (100). Parkin *et al.* [81] reported tunneling spin polarisation values of up to 85% at 0.27 K and room-temperature tunneling magnetoresistance values of 220% in

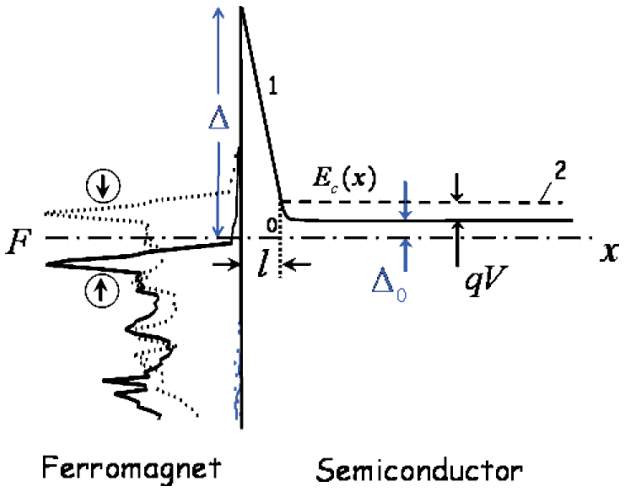

Figure 6.3: Energy diagrams of ferromagnet-semiconductor heterostructure with a thin highly doped layer (F is the Fermi level; Δ the height and l the thickness of an interface potential barrier; Δ_0 the height of the thermionic barrier in n-semiconductor). The standard Schottky barrier (1); $E_c(x)$ the bottom of conduction band in n-type semiconductor in equilibrium, under bias voltage V (2). The spin-polarised density of states in Ni is shown at $x < 0$ (reproduced from [85]).

CoFe/MgO(100) tunnel junctions. Spin polarised carrier injection into GaAs from a CoFe/MgO(100) tunnel injector was investigated [83] by the same group. They obtained 47% spin polarisation in GaAs at 290 K. Therefore, MgO (100) based tunnel spin injectors are attractive for future semiconductor spintronic applications.

Schottky contacts: Schottky barriers that form between semiconductors and metals can be used as spin filters. When the barrier is biased in the reverse direction and the transport is dominated by field emission, the carriers tunnel through the barrier at the Fermi energy and the density of states in the ferromagnet leads to a spin dependent tunnelling probability. It should be noted that even in reverse bias the injection could be minimal due to a wide depletion region in the semiconductor. The use of a thin, heavily doped surface region in the ferromagnet/semiconductor barrier reduces the depletion width, significantly enhancing the probability for tunnelling. This has been shown experimentally by Hanibicki *et al.* [84], where they achieved spin injection of up to 32 % by using reverse biased Schottky barriers of Fe/AlGaAs. Bratkovsky *et al.* [85] showed theoretically that spin injection could be significantly increased by introducing a highly doped layer between the ferromagnet and semiconductor. This would make the barrier become thinner and the probability of electron

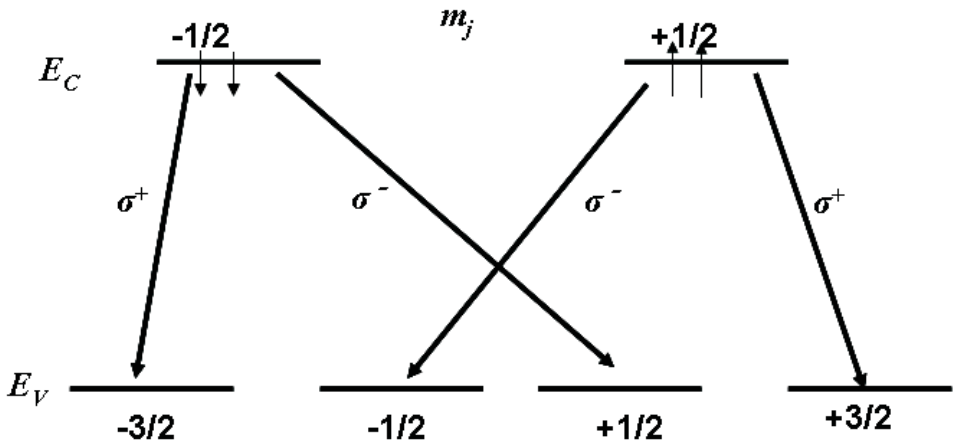

Figure 6.4: A schematic representation of the allowed radiative transitions in GaAs. E_c and E_v are the nondegenerate conduction and valence bands, respectively. The nondegenerate quantum states m_j are shown for holes in the valence band and electrons in the conduction band. σ^+ and σ^- are the left and right circularly polarised components of electroluminescence.

tunnelling through the barrier increased. The band structure as shown schematically in Fig. 6.3 is such that 100% injection is expected for the hot electrons.

Optical detection of small spin polarisations has been a common approach for detecting injected spins in semiconductors. It is known from quantum mechanics that in zincblende type semiconductors like GaAs, the selection rules for radiative recombination of electrons and holes are spin selective. Due to the nature of the heavy hole and light hole band splitting in a GaAs quantum well, as shown schematically in Fig. 6.4, two radiative recombination mechanisms for holes and electrons are possible. An electron from the nondegenerate conduction band ($m_j = \pm$ 1/2) may recombine either with a light hole ($m_j = \pm$ 1/2) or a heavy hole ($m_j = \pm$ 3/2), with the probability of the heavy hole process being three times as high as for the light hole process, where m_j's are the quantum states. Here, the transitions are spin selective, e.g. a spin-up electron ($m_j =$ + 1/2) can either recombine with a spin-up heavy hole ($m_j =$ + 3/2) resulting in a left (σ^+) circularly polarised components of electroluminescence or with a spin-down ($m_j =$ - 1/2) light hole resulting in a right (σ^-) circularly polarised components of electroluminescence and vice versa as shown in Fig. 6.4. If a GaAs LED is driven by spin-polarised electrons from the n-side, while unpolarised holes are supplied from the p-side, the spin polarisation may thus be de-

termined from the degree of circular polarisation of the electroluminescence signal as shown in Fig. 6.4. Hanbicki *et al.* [84] obtained electron-spin polarisations of 32% in a GaAs quantum well via electrical injection through a reverse-biased Fe/AlGaAs Schottky contact.

The optical detection technique is applicable to GaAs-based structures where the structural inversion asymmetry in the crystal lattice allows spin sensitive optical emission which is not possible in case of Si or Ge due to crystal lattice symmetry and indirect band-gap. An alternative method for spin injection and detection could be the all-electrical system where both injection and extraction are performed electrically. Back-to-back ferromagnet/semiconductor Schottky barriers could be used to show spin injection and extraction in a nonmagnetic semiconductor. In this structure, shown in Fig. 6.5, the ferromagnetic electrodes will have different coercivities (i.e. different widths in the hysteresis loop). By varying the relative orientation of magnetisation in these two electrodes it might be possible to detect spin polarised current (spin injection) in terms of magneto resistance. Depending on the relative orientation of magnetisations between these two ferromagnets the device will exhibit different magnetoresistances.

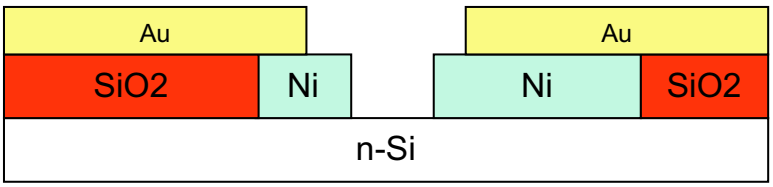

Figure 6.5: Schematic representation of a device containing back to back Schottky barrier for electrical spin injection and extraction.

6.3 Si-based vertical geometry for spin injection

The conductivity mismatch of a ferromagnet and a semiconductor to spin polarised electrons prevent ohmic contacts from being used for spin injection [77, 86]. As an alternative, Schottky barriers and ferromagnet / oxide / semiconductor contacts have been used [80, 84] that introduce a spin dependent resistance at the ferromagnet/semiconductor interface. Accordingly, all-electrical spin injection and extraction

device has been investigated in lateral [87] and vertical [9] geometry. A ferromagnet / semiconductor / ferromagnet back-to-back Schottky barrier-based spin injection and extraction device has been proposed [85].

The current conduction of a ferromagnet/semiconductor Schottky barrier in a lowly n-doped semiconductor is usually dominated by the TE mechanism [6], which is believed to be unsuitable for spin injection and extraction as the electron transmission occurs well above the Fermi-level (Fig. 6.6a). The image force lowering effect pushes the barrier peak away from the interface at a point in the semiconductor where the density of states are not spin-dependent. On the other hand, the current conduction of a reverse-biased ferromagnet/semiconductor Schottky barrier in a highly n-doped semiconductor is dominated by the TFE mechanism [35], where the electron tunneling takes place at a lower energy at a point where spin-dependent density of states exists resulting in spin polarised transmission (Fig. 6.6b).

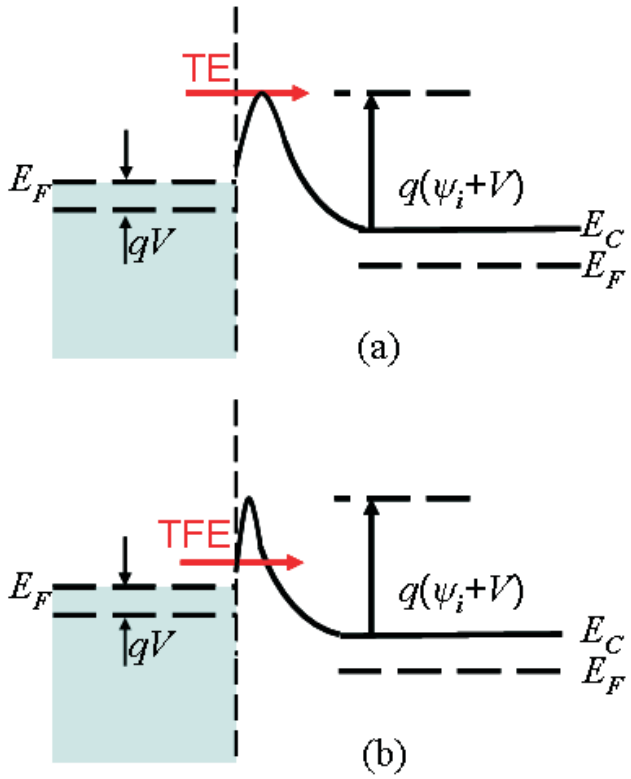

Figure 6.6: A schematic representation of the effect of image force lowering on the (a) TE and (b) TFE mechanism for spin injection in a reverse-biased Schottky contact.

The motivation towards a Si based device is due to its technology dominance in

the device industry. Si also offers long spin lifetimes and diffusion lengths due to its weak spin orbit interactions. Lateral spin transport structures based on Si have recently been reported [88], where a nonlocal detection technique has been adopted, which benefits from excluding any spurious contributions from anisotropic magnetoresistance or local Hall effects on spin currents. For practical applications, however, electrical spin injection and detection in semiconductor needs to take place locally requiring additional stringent conditions eg. large tunnel spin polarisation (for a tunnel contact) and a proper resistance-area product [89].

In the present work, a vertical spin transport structure of Co/Si/Ni junctions fabricated on a Si membrane has been investigated that uses Co/Si and Ni/Si Schottky barriers as the spin injection and extraction electrodes. The structure benefits from increased control over vertical scalability of Si enhancing the potential spin transfer between the two electrodes. Thermionic field emission mechanism has been observed to be dominant in the $I - V$ characteristics of the devices which is confirmed by fitting numerical simulation results. No magnetoresistance signal was observed in any of the devices even at low temperatures which is partly attributed due to high resistance-area product at the interfaces. However, this experiment shows that an electrically well functioning back-to-back Schottky barriers can be fabricated using the membrane technique and further experiments can build upon these results. As an example, it is shown by numerical simulation that by using a highly doped thin Ge layer at the Schottky interface the resistance-area products could be tuned to obtain high magnetoresistance.

6.4 Experimental procedures

The Co/Si/Ni devices have been fabricated on Si membranes using SOI wafers as starting material. The top and back square windows of 50 μm^2 area have been created by using a combination of standard lithography, oxidation, and KOH anisotropic etching. The nominal thickness of the membrane is 250 nm and the active Si membrane is separated from the Si handle layer by 400 nm of SiO_2. A range of dopant concentrations of 4×10^{17} cm^{-3}-4×10^{19} cm^{-3} in the Si membranes were obtained by P implant. These processing steps were performed at CRANN, Trinity College, Dublin.

As discussed in Chapter 3, the rectifying behaviour of Schottky barriers fabricated by electrodeposition superior to those prepared by evaporation. However, a smooth and continuous metal film deposition by the electrodeposition technique requires the semiconductor to be highly conductive. In the Si membrane structure only the device area are highly doped. This resulted in a lack of good conductivity of throughout the membrane length and a good quality film could not be obtained by electrodeposition. Fig. 6.7 shows a typical Ni film grown by electrodeposition on the Si membranes.

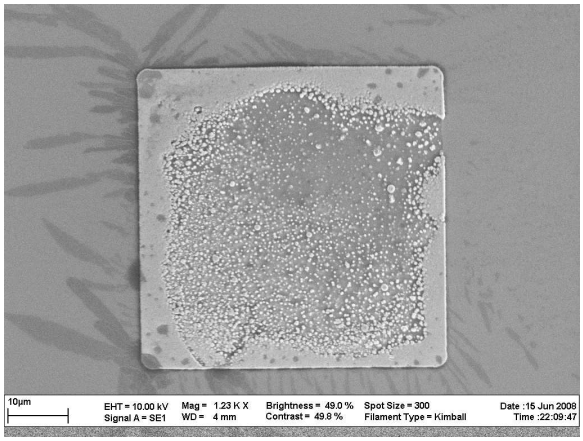

Figure 6.7: An SEM image of a Ni pad grown by electrodeposition of Ni on the Si membrane.(This part of experiment was done by Xiaoli Li)

Therefore, metallisation of 250 nm Ni and 50 nm Co on the Si membranes was rather performed by evaporation. Deposition on both sides of the sample required breaking vacuum to flip the sample over. However, prior to each deposition process a 20:1 buffered HF dip for 20 seconds was performed. A schematic diagram of the fabricated device is presented in Fig. 6.8a. An SEM image of the device is presented in Fig. 6.8b. $I - V$ characteristics measurements were performed using a Hewlett Packard 4155C semiconductor parameter analyzer. For magnetoresistance measurements, a DC sense current was passed through the current leads and the resistance was recorded automatically using a two terminal method as the in-plane magnetic field was swept. The measurements were performed at temperatures ranging from 50 to 300 K. The low temperature measurements were performed using a Bio-Rad DL 4960 cryostat temperature controller that enables a temperature variation from 1.5 K to room temperature.

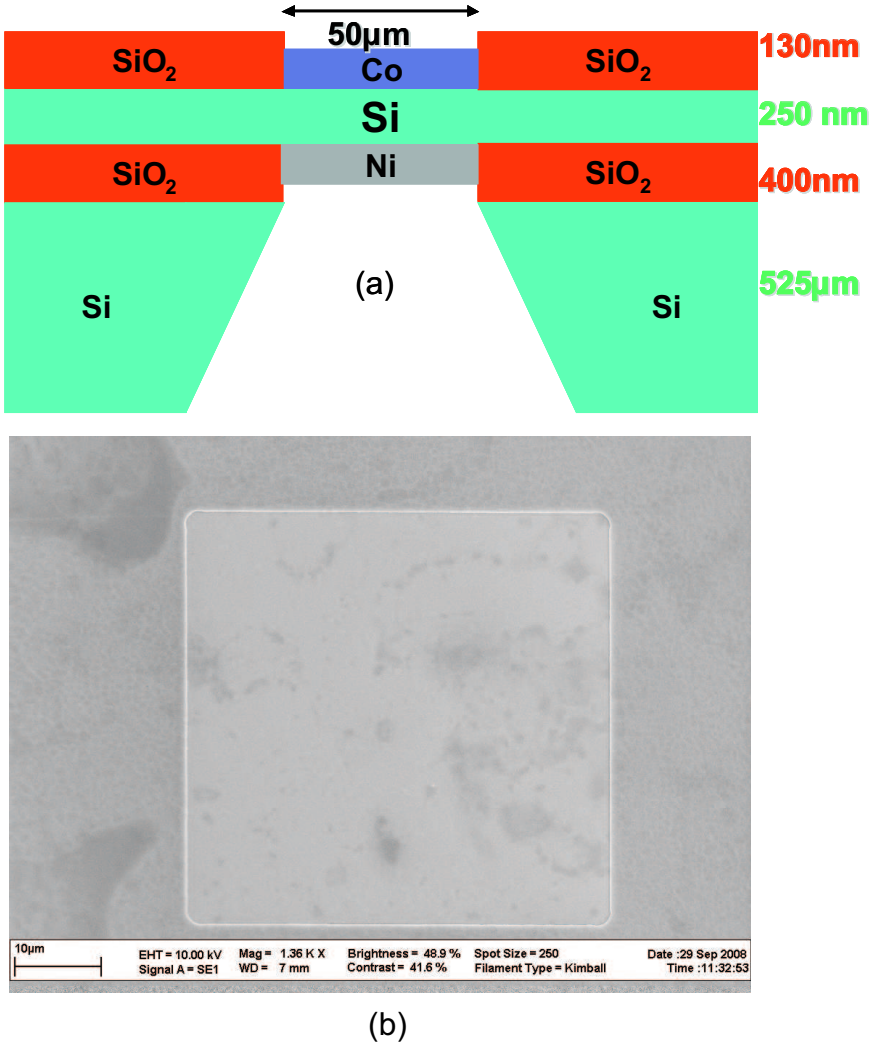

Figure 6.8: (a)A schematic representation (not to scale) of the vertical Co/Si/Ni back-to-back Schottky barrier based spin injection-extraction device. (b) A scanning electron micrograph of the fabricated device showing the top Co contact.

6.5 Results and discussions

6.5.1 Electrical characteristics

Typical $I - V$ characteristics of the Co/Si/Ni device measured at various temperature for various Si membrane doping density N_d are presented in Fig. 6.9. During measurement the anode and the cathode were connected to the Ni and the Co pad, respectively. Therefore, at positive biases, the current is dominated by the reverse bias current of the Co/Si Schottky barrier, whereas, at negative biases, it is limited

by the reverse current of the Ni/Si Schottky barrier. For the doping densities considered in the Si membranes of the devices, the current conduction mechanism is usually dominated by TFE mechanism at the temperature ranges concerned. Therefore, the increase of current with increasing bias voltage, observed in Fig. 6.9, is due to the tunneling of electrons at the respective Schottky barriers. The slight difference in the rate of current increase with increasing positive and negative biases is attributed to the different barrier heights of the Co/Si (0.65 eV [90]) and Ni/Si (0.70 eV [35]) Schottky barriers, respectively. Fig. 6.9 also reveals that the current density becomes less temperature dependent with increasing N_d, which again can be explained by a standard TFE model [35]. From the $I - V$ curves presented in Fig. 6.9, the values of currents were obtained for the corresponding spin injection bias voltage ranges of +ve 0.1-0.3 Volts (taking the Co/Si contact as the injector and the Ni/Si contact as the detector) and -ve 0.1-0.3 Volts (taking the Ni/Si contact as the injector and the Co/Si contact as the detector) at various temperatures.

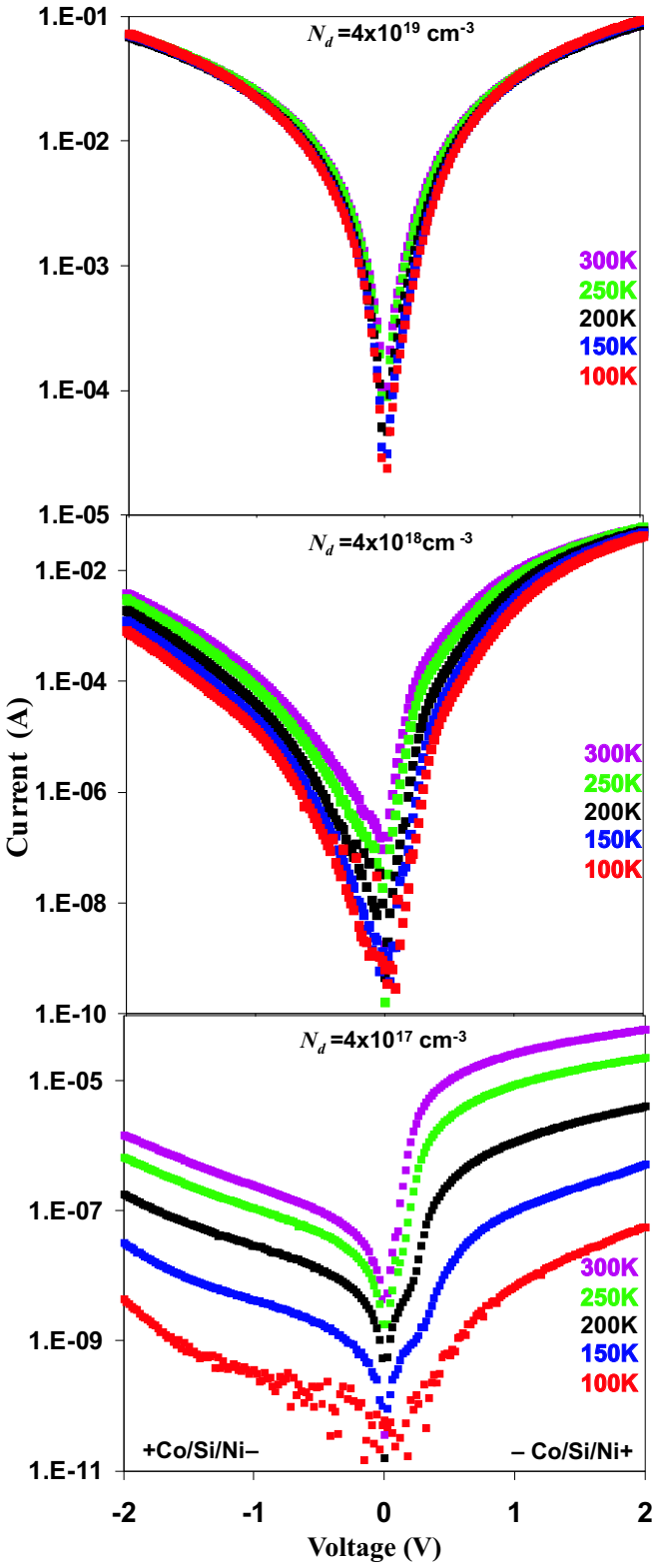

Figure 6.9: $I - V$ characteristics of the Co/Si/Ni devices as a function of temperature measured for various Si membrane doping densities N_d.

6.5.2 Magnetotransport characteristics

In order to verify a differential switching behaviour of the magnetisation in the ferromagnetic layers Vibrating Sample Magnetometer measurements were performed on Si samples containing bulk Co (50 nm) and Ni (250 nm) films. The Co film had dimensions of 1 cm × 0.9 cm, whereas, the Ni film had dimensions of 0.5 cm × 0.5 cm. During measurements, the magnetic field was applied along the long axis (in case of Co) and perpendicular to the sides (in case of Ni) In Fig. 6.10, the magnetisation versus applied field characteristics of the Co and Ni films are presented, which clearly shows the differential switching of magnetisation in the two films. The saturation magnetisation of Co and Ni films were found to be ∼150 e.m.u./g and ∼50 e.m.u./g, respectively. These values match very closely with the reported values of saturation magnetisations (161 e.m.u./g for Co and 54 e.m.u./g for Ni) in literature [91].

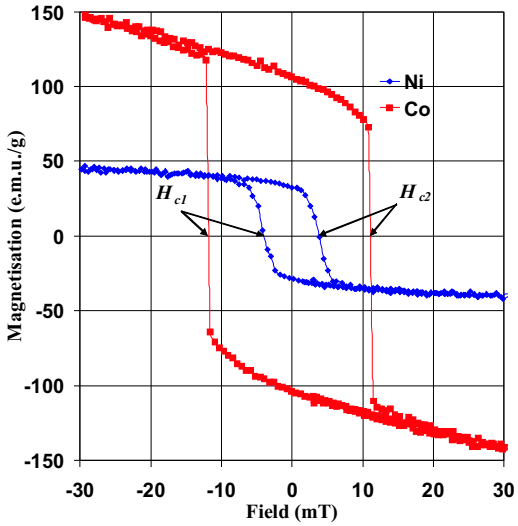

Figure 6.10: Magnetisation versus field charactersistics of a Co (50 nm) and a Ni (250 nm) film showing their differectial magnetisation switching. The Co film had dimensions of 1 cm × 0.9 cm, whereas, the Ni film had dimensions of 0.5 cm × 0.5 cm. The field was applied along the long axis (in case of Co) and perpendicular to the sides (in case of Ni). The overall coercive fields for the films were calculated taking the average of the left (H_{c1}) and right (H_{c2}) magnetisation switching fields.

The coercive fields for these ferromagnetic films are calculated by taking the average of the left (H_{c1}) and right (H_{c2}) magnetisation switching fields. The calculated coercive fields for the Co film and the Ni film are found to be 11.85 mT and 4

mT, respectively with a difference of 7.85 mT. Hence, the magnetisation in the two ferromagnetic films in the vertical Co/Si/Ni device can be considered to exhibit a differential magnetisation switching behaviour in the applied field range of ±30 mT.

Magnetoresistance measurements were performed on the fabricated Co/Si/Ni spin devices using the corresponding DC sense currents for bias voltages of ± 0.1, 0.2 and 0.3 Volts while sweeping an in-plane magnetic field in the range of -500 mT to +500 mT at a temperature range from 100 to 300 K. Typical magnetoresistance measurements at low temperatures for the Co/Si/Ni device for a Si membrane doping density of 4×10^{18} cm^{-3} and 4×10^{19} cm^{-3} are presented in Fig. 6.11 and in Fig. 6.12, respectively. No magnetoresistance signal corresponding to electrical spin injection was observed for any of the devices. An increase of resistance of 0.04% due to Lorentz deflection was, however, observed (Fig. 6.13) only for the lowly doped Si membrane (4×10^{17} cm^{-3}) at an applied magnetic field of 500 mT when a sense current of 1 μA was passed. The noise level of the obtained signal was very low (∼0.01%) confirming our measurement setup to be insensitive to the anisotripic magnetoresistance of the vertical ferromagnets.

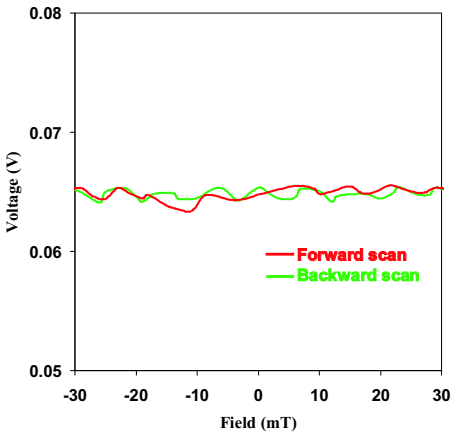

Figure 6.11: Magnetoresistance measurements at 100 K of the Co/Si/Ni spin injection extraction device. The silicon membrane doping density was 4×10^{18} cm^{-3}. The magnetic field was scanned from -30 mT to 30 mT with 1 mT step size. The applied sense current was 1 nA.

The reason behind the absense of a magnetoresistance in the vertical Co/Si/Ni device could be due to an inter-diffusion of magnetic contaminants into semiconductor by the high energy deposition technique of evaporation. This may have severely

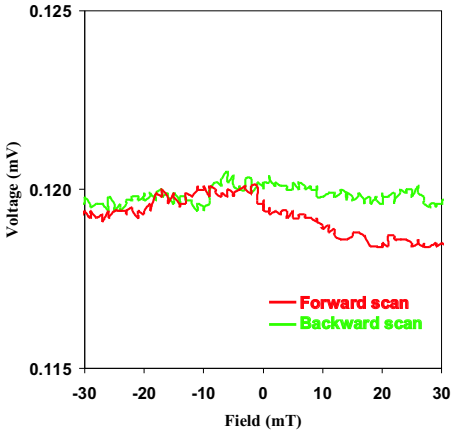

Figure 6.12: Magnetoresistance measurements at 100K of the Co/Si/Ni spin injection extraction device. The silicon membrane doping density was 4×10^{19} cm^{-3}. The magnetic field was scanned from -30 mT to 30 mT with 1 mT step size. The applied sense current was 100 nA.

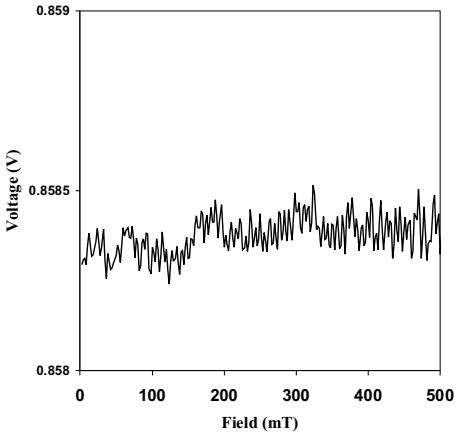

Figure 6.13: Magnetoresistance measurements at 150 K of the Co/Si/Ni spin injection extraction device showing the effect of Lorentz deflection. The silicon membrane doping density was 4×10^{17} cm^{-3}. The applied sense current was 1000 nA.

decreased the spin polarisation as mentioned by Roy *et al.* [92]. The high energy Ni deposition could have produced an interfacial silicide layer hampering spin transport across the ferromagnet/semiconductor interface. This could be avoided by a method immune to silicide formation, such as the electrochemical deposition of Ni on Si [6]. Alternatively, a thin oxide tunnel barrier at the interface would be beneficial. Another important factor for the lack of spin injection could be an improper resistance-area product of the injection electrodes as investigated experimentally by Min *et al.* [89]. The resistance-area product of a contact is defined as the applied voltage divided by the current density at a particular value of voltage. The calculated resistance-area products from the $I - V$ measurements on the devices for spin injection condition (0.2 Volts) are plotted as a function of temperature in Fig. 6.14. The minimum resistance-area products obtained in these samples, for example, when N_d=4×10^{19} cm^{-3}, are in the region of 10^{-6} Ωm^2. This is too high for a measurable magnetoresistance, according to the calculation done by Min *et al.*

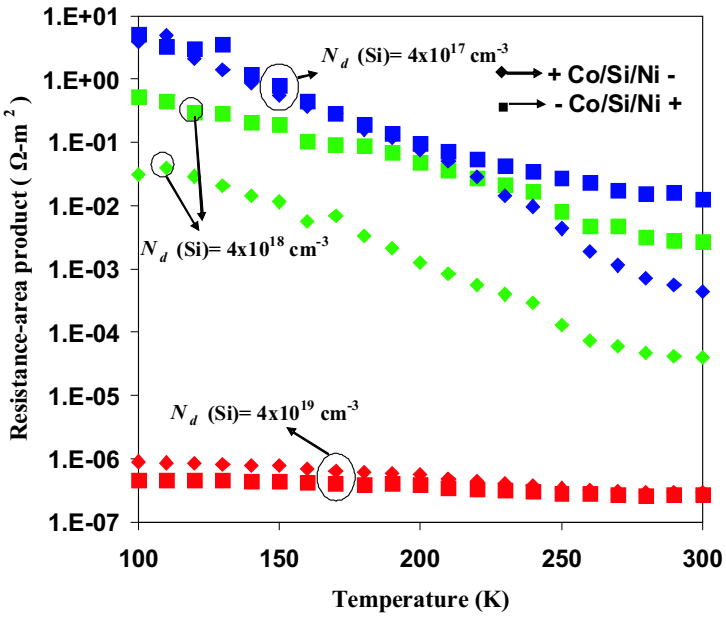

Figure 6.14: Resistance-area products measured at ± 0.2 Volts bias of the Co/Si/Ni spin injection-extraction device for various Si membrane doping densities N_d.

6.5.3 Simulation of the spin injection extraction device

As an attempt to reduce the resistance-area products of the Co/Si/Ni devices, the effect of growing a thin highly doped Ge layer at the Co/Si and Ni/Si interfaces is investigated by numerical simulation. The commercial TCAD simulator Sentaurus Device from Synopsys has been used to exhibit the experimental Schottky diode results. The devices are generated using Sentaurus Structure Editor and its Meshing engine. A very fine mesh of 1 nm square was created for the entire device.

At first the simulator is calibrated by using the Schottky barrier heights (0.70 eV for Ni/Si contact and 0.64 eV for Co/Si contact) and the various experimental doping densities N_d of the Si membranes. During this calculation various physical models, for example, effect of image force barrier lowering, bandgap narrowing and electron barrier tunneling have been used. The corresponding calculated $J - V$ curves for the various substrate doping densities are presented in Fig. 6.15 along with the experimental curves measured at 300 K. The concordance of the experimental and simulated current density curves confirms near full calibration of the simulator tool.

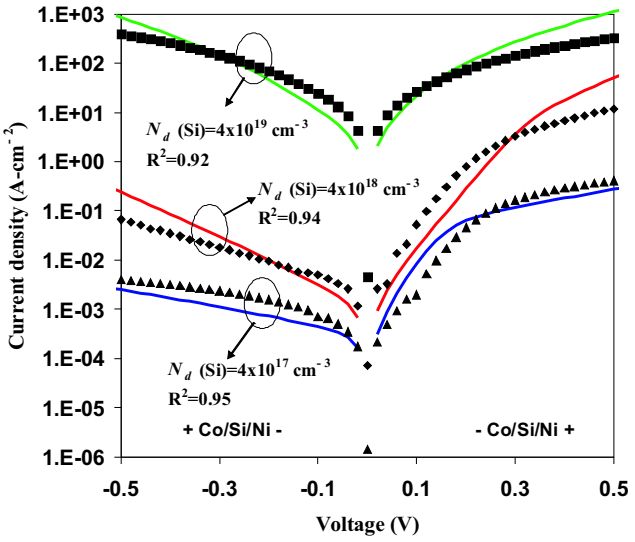

Figure 6.15: $J - V$ characteristics (symbols) of the fabricated Co/Si/Ni spin injection-extraction device for various Si membrane doping density. The solid lines refer to the $J - V$ curves modelled by Sentaurus Device simulator tool.

The effect of incorporating a 2 nm n-type δ-Ge layer of 1×10^{20} cm^{-3} doping density at both of the Schottky interfaces was simulated. The resulting resistance-area

products of the contacts for a ±0.2 Volts bias are plotted in Fig. 6.16 as a function of various Si membrane doping density N_d along with the experimental results obtained at 300 K. It is observed that the resistance-area products have been reduced to the high magnetoresistance region for all devices. Therefore, further experiment can be built on our Si-membrane-based vertical spin injection device by growing a thin, highly-doped Ge layer at the Schottky interfaces.

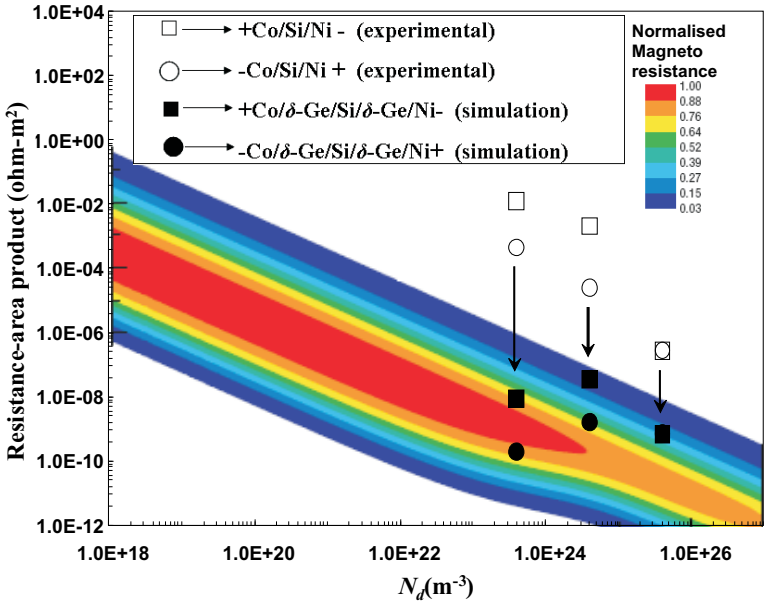

Figure 6.16: Resistance-area products of the fabricated Co/Si/Ni device and the simulated Co/δ-Ge/Si/δ-Ge/Ni device as a function of Si doping density for applied biases of ± 0.2 Volts. The calculated magnetoresistance of a Si spin transistor as a function of the contact resistance-area product and Si doping density N_d is adopted from Ref. [89], where the colour legend shows the value of normalised magnetoresistance.

6.6 Conclusions

A ferromagnetic/semiconductor Schottky barrier offers a spin dependent resistance to the spin-up and spin-down channels at the interface, which effectively eliminates the conductivity mismatch problem for spin injection. In case of Si an electrical spin detection mechanism using back-to-back Schottky barriers could be adopted for possible practical applications. Co/Si/Ni back-to-back Schottky barrier based spin injection and detection devices can be fabricated on thin Si membranes. Ni and Co

films of 250 nm and 50 nm thicknesses, respectively, show differential switching in their magnetisations, which is crucial for obtaining magnetoresistance indicative of spin injection. By using highly doped Si membranes, increased tunneling current could be attained in the Schottky junctions at low temperatures. This tunneling at a reverse biased Schottky barrier junction is the key to obtain spin injection in semiconductors. Additionally, a proper resistance-area product of the Schottky contact is very important to obtain high magnetoresistance indicative of spin injection. Based on the simulation results presented in this Chapter it can be concluded that by growing a thin highly doped Ge layer at the Schottky interfaces the resistance-area products of the contacts could be tuned to achieve high magnetoresistance. Finally, the metallisation technique used to fabricate Schottky barrier junctions could also affect the spin injection. A low energy metallisation technique, such as electrodeposition, should be used as opposed to physical vapour deposition techniques to minimise any inter-diffusion of magnetic contaminants into the semiconductor.

Chapter 7

Conclusions and outlook

The work presented in this thesis show that electrodeposited metal/Ge Schottky barriers are superior to those prepared by physical vapour deposition techniques. This is shown especially in the lower reverse bias leakage current. This improvement has revealed a number of interesting physical phenomena with potential implications for many different devices.

One strand of this thesis is directed to improve the parasitic series resistance of the source/drain in Ge based doped nMOSFETs. Formation of an ohmic contact at the n-type source/drain is hampered due to the extreme Fermi-level pinning near the valence band of Ge which is due to the presence of metal-induced gap states at a metal/Ge contact. In order to resolve this problem the Fermi-pinning characteristics on nGe was investigated. Electrodeposited Ni/Ge Schottky barriers on lowly doped Ge were characterised by $I-V$, $C-V$ and low temperature $I-V$ measurements. The barrier heights were found spatially varying which results in a non-Arrhenius behaviour of temperature dependence. This temperature dependence of Schottky barrier heights is well fitted to a model by Werner and Guttler who assumed a spatial distribution of the barrier heights expressed by a Gaussian function. A physical explanation of the spatial variation of the Schottky barrier heights could be attributed to the existence of a spatially varying thin oxide layer at the metal/Ge interface that results in a spatially varying pinning of the Fermi-level. The Fermi-level pinning hence could be overcome by using a thin oxide layer at the Ni/Ge interface. However, maintaining an adequate tunneling probability through the oxide layer is critical

to obtaining a low resistance metal/semiconductor junction in the source/drain of MOSFETs. Therefore, for Fermi-level de-pinning a non-uniform oxide layer might actually be more beneficial than a uniform layer.

In order to improve the performance of Ge-based short channel Schottky barrier MOSFETs, the source/drain formation by electrodeposition technique was investigated. In order to overcome short channel effects in Schottky barrier MOSFETs a highly doped substrate could be used. However, this imposes a challenge to the conventional method of source/drain formation using physical vapour deposition techniques since increasing the substrate doping increases the leakage currents in the the source/body and drain/body junctions. Ni/Ge Schottky barriers were fabricated by electrodeposition technique. These barriers showed high rectification with low leakage current in reverse bias even for a highly doped Ge. Ni-germanidation was performed by annealing the samples at high temperatures for a solid state reaction. X-ray diffraction investigations showed that NiGe was the only phase existing when a 70 nm Ni film was annealed at 500 °C. For this film, the lowest resistivity and sheet resistance was observed. This low resistive NiGe is crucial for source/drain formation in Schottky barrier MOSFETs. $I - V$ measurements revealed that despite the compositional change, the barrier properties were virtually unaltered due to extreme Fermi-level pinning in Ge. The reverse leakage current was orders of magnitude lower than that of similar Schottky barrierss formed by evaporation technique in literature. Numerical simulation of a Ge-based short channel Schottky barrier pMOSFET was performed for various Ge doping density. A calibration of the simulator was previously performed to exhibit the same Schottky characteristics at the source/drain of the simulated MOSFETs as in the experiment. The MOSFET simulation results reveal that a highly doped Ge substrate results in the lowest source to drain off-state leakage current. There is no additional contribution from the drain/body or source/body leakage. This is due to the extremely low leakage current in the electrodeposited Ni/Ge diode even on highly doped Ge. Therefore, electrodeposition technique could be used for source/drain formation to suppress source/drain leakage currents in a Ge based Schottky barrier MOSFET.

The experimental observation of negative differential conductance at low temperature in a Ni/Ge Schottky barrier diode is reported in another experiment. With the

aid of theoretical models and numerical simulation, it is shown that when a reverse bias is applied to a Ni/Ge Schottky barrier, electrons tunnel into the high electric field of the depletion region. This scatters the electrons into the upper valley of the Ge conduction band, which has a lower mobility. The observed negative differential conductance is hence attributed to the transferred-electron effect. The observed effect is particularly important for hot carrier injection in Gunn diodes. This experiment shows that the thermionic field emission mechanism through a Schottky barrier can be used for hot electron injection in Gunn diodes as opposed to the conventional Gunn diodes where the carrier injection is performed using the thermionic emission mechanism over a graded gap injector.

An attempt has been made to investigate electrical injection and detection of spin polarised current into Si using Schottky barrier contacts. This may lead to Si based spin transistor for practical applications. A vertical spin device consisting of Co/Si and Ni/Si back to back Schottky contacts is fabricated on a Si membrane. Low temperature $I - V$ measurements revealed the conduction being dominated by thermionic field emission, which is normally used for spin injection using Schottky contacts. However, magnetoresistance measurements performed on the device showed no evidence of spin injection. A likely explanation for the lack of spin signal is the high resistance-area product exhibited by the Schottky contacts at spin injection condition. Using numerical simulations it was shown that by growing a thin, highly-doped Ge layer at the Schottky interfaces the resistance-area products of the contacts could be tuned to achieve high magnetoresistance. Therefore, this experiment shows that an electrically well functioning back-to-back Schottky contact could be fabricated using the Si membrane for spin injection-detection in Si and further experiments can build upon this.

The outcome of the work presented in this thesis is significant because it provides an understanding of the physical and electrical properties of electrodeposited Ni/Ge interfaces and directs the future improvements of the semiconductor devices. Firstly, for an n-channel Ge based doped source/drain MOSFET, the parasitic series resistance at the source/drain could be minimised by using a thin non-uniform oxide layer between the metal and Ge interface. This would result in drive currents as a result of reducing the electron barrier height by de-pinning the Fermi-level. In-

vestigation of this finding in a Ge based nMOSFET could be performed. Secondly, electrodeposited Ni/Ge Schottky barriers could be used for source/drain formation in a Ge based Schottky barrier pMOSFET to suppress the junction leakage in the OFF state. The drive current of a Schottky barrier pMOSFET could be improved by reducing the hole barrier height at the source end. Therefore, investigations could be carried out to de-pin the Fermi-level so that a lower or even negative hole barrier height can be obtained at the source/channel junction of a Ge based Schottky barrier pMOSFET. Thirdly, the electrical characteristics of metal/GaAs or metal/InP could be investigated for possible application in a Schottky barrier injection based Gunn diode. A high Schottky barrier on a highly doped semiconductor (e.g. Ge or GaAs) would generate a large depletion field at reverse bias, which would scatter any tunneling electron to a low mobility conduction band resulting in negative differential resistance of the diode. Since electrodeposition of a metal results in a high Schottky barrier to semiconductor, this technique could be used on GaAs or InP for possible observation of negative differential resistance in the Schottky barriers. Finally, a demonstration of all electrical spin-injection and detection would be an international breakthrough in the field of electronics with major physical and engineering implications. Towards this, the Co/Si/Ni vertical structure presented in this thesis requires further investigations. The lack of observation of spin injection could be due to any inter-diffusion of ferromagnets as a result of the high energy Ni evaporation. This could be avoided by using electrodeposition of Ni and Co on Si. A further investigation on this deposition techniqe will be required to obtain a smooth and continuous ferromagnetic film on Si membrane. Moreover, the contact resistance-area product may need to be optimised by using a highly doped thin Ge layer at the interface. Alternatively, a thin tunnel barrier at the ferromagnet/semiconductor interface could also be introduced to study spin injection. Since a crystalline tunnel barrier such as MgO(100) gives large tunnel spin polarisations, application of such a barrier at the ferromagnet/semiconductor contact could be investigated.

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