LOSS COMPARISON OF TWO AND THREE-LEVEL INVERTER TOPOLOGIES

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Abstract

This paper investigates semiconductor and DC-link capacitor losses in two two-level and two three-level voltage source inverters. The components of the four inverters are selected to have appropriate voltage and current ratings. Analytical expressions for semiconductor losses are reviewed and expressions for DC link capacitor losses are derived for all topologies. Three-level inverters are found to have lower semiconductor losses, but higher DC-link capacitor losses. Overall, the three-level Neutral-Point-Clamped inverter proved to be the most efficient topology.

1 Introduction

The process of selecting the topology, components and operating parameters (voltage, current and switching frequency) of an inverter is highly affected by the anticipated inverter losses. An accurate estimate of the losses occurring in each part of an inverter can significantly contribute to achieving an enhanced inverter design. This paper examines the semiconductor and DC-link capacitor losses of four voltage source inverter topologies: the conventional two-level inverter, the two-level two-channel interleaved inverter, the three-level Neutral-Point-Clamped (NPC) inverter and the three-level Cascaded H-Bridge inverter, shown in Figure 1.

Losses in two-level inverters have been reported extensively in the literature. Researchers have also investigated semiconductor losses in three-level inverters. Estimates of switching losses have been obtained using approximations of IGBT and diode *I-V* switching characteristics [1, 4, 17, 18]. However, a more convenient approach based on calculating switching loss using the switching energy-current (E_{sw}-I) characteristics, reveals that the switching losses of an IGBT-diode pair are approximately proportional to the switching voltage and current [12]. This observation can be verified based on IGBT-Diode module data sheets [8]. Analytical expressions for switching losses in a two-level inverter can be found in [7, 12]. For the two-level inverter, all continuous PWM methods have the same switching losses, which are also independent of the load phase angle [9, 12]. Discontinuous strategies, however, can result in lower switching losses. Switching losses in a three-level NPC inverter have been investigated in [7], using a second order approximation of the IGBT and diode E_{sw}-I characteristics.

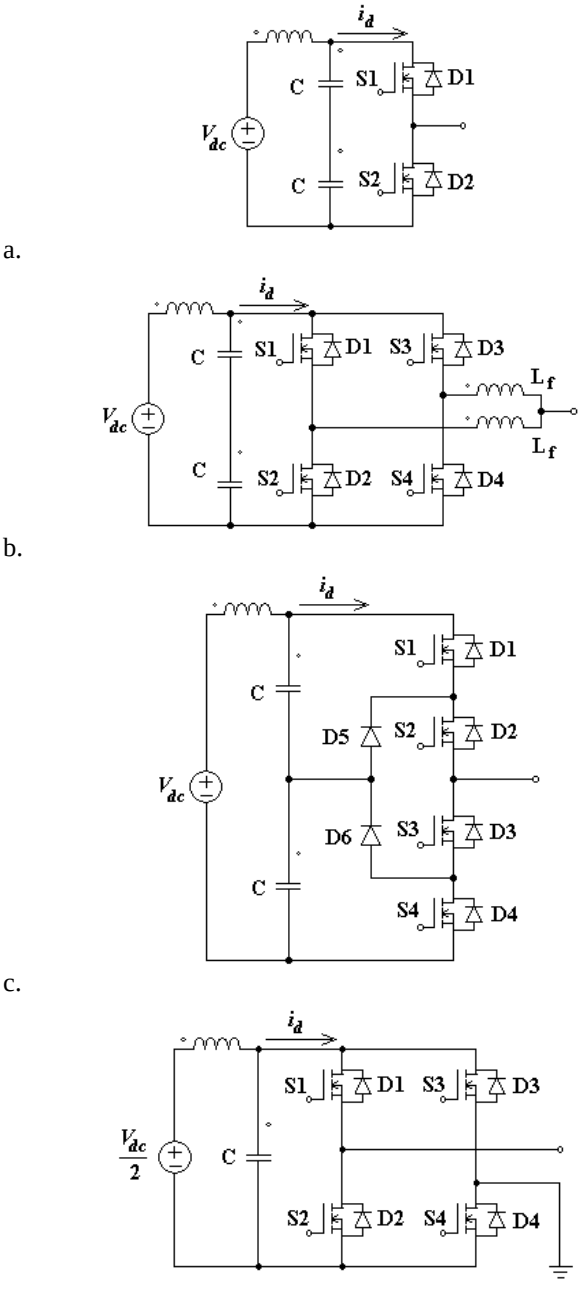

Figure 1: Circuit diagrams (one leg) of (a.) Two-level inverter, (b.) Two-channel two-level interleaved inverter, (c.) Three-level NPC inverter and (d.) Three-level Cascaded H-Bridge inverter.

Expressions for the two-level inverter conduction losses can be found in [4, 12, 14]. The calculation of conduction losses is based on the linear *I-V* characteristics of the IGBT-diode modules. Unlike switching losses, two-level inverter conduction losses are affected by the selection of the PWM strategy and the load power factor. Expressions for the NPC inverter can be found in [7] as well as in [21] for a number of modulation strategies.

DC-link capacitor loss estimation is based on the rms value of the capacitor current. The derivation of the current rms expression for the two-level inverter has been presented in [8, 13, 19]. Capacitor loss estimations also appear for the two-level two-channel interleaved and the three-level Cascaded H-Bridge inverters in [2] and [20], respectively. The DC-link of the three-level NPC inverter has only been studied in the literature with respect to its voltage and the capacitor balancing problem [5, 15, 16].

In this paper, expressions for switching and conduction losses in the four inverter topologies are reviewed. Analytical expression for DC-link capacitor losses are derived for the two-level interleaved and the three-level inverters. Unlike most studies that focus on a single inverter topology or loss type, the expressions for semiconductor and DC-link capacitor losses are used to compare the four examined topologies. Another significant contribution of the paper is that the comparison is based on a selection of inverter components from available commercial devices with appropriate voltage/current ratings and switching frequency. This selection which is different for each topology, affects the resulting losses.

2 Selection of IGBT-Diode Modules

The four inverter topologies are compared on the basis of a common power output. Assuming a DC-link voltage V_{dc} of 2kV (1kV for the Cascaded H-Bridge inverter) and a nominal load peak current I_M of 370A, the inverter power rating S_o is equal to 555kVA.

The switching voltage of the IGBT-diode modules in a three-level inverter is half of that in a two-level inverter generating a voltage waveform with the same amplitude. The voltage rating of the IGBT-diode modules used in a three-level inverter therefore needs to be half that of an equivalent two-level inverter. This difference in voltage rating has a very significant impact on switching and conduction loss parameters of the modules.

The current carried by each module is the same for all topologies except for the interleaved inverter in which each module carries half the current. The effect of the module current rating on switching loss parameters is insignificant, but conduction loss parameters are approximately doubled for the half current-rated modules.

Appropriate IGBT modules are selected for each topology. The two-level inverter uses high-voltage high-current IGBT-diode modules (A), the interleaved inverter uses high-voltage low-current modules (B), while the three-level inverters uses the low-voltage high-current module (C). Table 1 lists the switching and conduction parameters of the selected modules. Module A is the Eupec FZ800R33KL2C_B5 3.3kV – 800A IGBT-diode module, Module B is the FZ400R33KL2C_B5 3.3kV – 400A IGBT-diode module, while Module C is the FF800R17KE3 1.7kV – 800A module. Parameter values have been obtained from modules' data sheets [8].

Parameter	Module A	Module B	Module C	Unit
V_{base}	1.8	1.8	0.9	kV
$V_{0,c}$	1.6	1.6	0.9	V
R_c	2.5	5	1.87	mΩ
$V_{0,d}$	1.7	1.7	1	V
R_d	1.25	2.5	1	mΩ
a_c	5.7	5.7	0.8	mJ/A
b_c	50	50	40	mJ
a_d	0.5	0.5	0.12	mJ/A
b_d	150	150	60	mJ

Table 1: IGBT-Diode module parameters

Parameters $V_{0,c/d}$ and $R_{c/d}$ approximate the conduction *I-V* characteristics of IGBTs/diodes, respectively, according to:

$$V = V_{0,c/d} + I \cdot R_{c/d} \quad (1)$$

Parameters V_{base} , $a_{c/d}$ and $b_{c/d}$ approximate the switching energy E_{sw}-*I* characteristics according to:

$$E_{sw,c/d} = \frac{V_{sw}}{V_{base}} \left(a_{c/d} \cdot I_{sw} + b_{c/d} \right) \quad (2)$$

where V_{sw} and I_{sw} are the instantaneous switching voltage and current, respectively.

3 Estimation of Inverter Semiconductor Losses

For a given switching frequency f_s, the two-level inverter has the same switching losses for all continuous PWM methods. Switching losses are also independent of the inverter modulation index *M* and the load power factor *PF* [12] but increase linearly with switching frequency. Conduction losses are not affected by f_s but depend on the modulation strategy, *M* and *PF*. For commonly used switching frequencies, conduction losses of the two-level inverter are significantly lower than corresponding switching losses.

The two-level two-channel interleaved inverter losses are examined under the assumption that the instantaneous current carried by each of the inverter channels is approximately half of the respective phase current. Leg (channel) inductors and sufficiently high switching frequencies are used to satisfy this requirement. Each module in this topology therefore carries half the current of a two-level inverter module. On the other hand, the number of modules in the interleaved inverter is twice that of the conventional two-level inverter.

Given that the expressions for switching and conduction losses in the conventional two-level inverter are (3) and (4), the expressions for the interleaved inverter losses can be proved to be (5) and (6), respectively. All equations refer to the three-phase inverters modulated by sinusoidal waveforms and their derivation is based on [12]. Parameters a and b represent the sums of a_c, a_d and b_c, b_d, respectively, of the module selected for each inverter.

$$P_{sw,2L} = 6\frac{V_{dc}}{V_{base}}\left(\frac{a}{\pi}I_M + \frac{b}{2}\right)f_s \quad (3)$$

$$P_{con,2L} = \left[\frac{3}{4}(R_c + R_d) + \frac{2M}{\pi}(R_c - R_d)\cos\phi\right]I_M^2 + \left[\frac{3}{\pi}(V_{c0} + V_{d0}) + \frac{3M}{4}(V_{c0} - V_{d0})\cos\phi\right]I_M \quad (4)$$

$$P_{sw,2L-Int} = 6\frac{V_{dc}}{V_{base}}\left(\frac{a}{\pi}I_M + b\right)f_s \quad (5)$$

$$P_{con,2L-Int} = \left[\frac{3}{8}(R_c + R_d) + \frac{M}{\pi}(R_c - R_d)\cos\phi\right]I_M^2 + \left[\frac{3}{\pi}(V_{c0} + V_{d0}) + \frac{3M}{4}(V_{c0} - V_{d0})\cos\phi\right]I_M \quad (6)$$

The individual switching loss expressions for the three-level NPC inverter modules given in [7], were revised assuming a linear dependence of the switching losses on the instantaneous current. Their summation yields Equation (7) for the total three-phase NPC inverter switching losses. The respective equation for conduction losses is (8). These expressions are applicable to any double carrier PWM methods with sinusoidal reference waveforms, such as three-level PD and APOD/POD PWM, explained in [10].

$$P_{sw,3L} = 3\frac{V_{dc}}{V_{base}}\left(\frac{a}{\pi}I_M + \frac{b}{2}\right)f_s \quad (7)$$

$$P_{con,3L} = \left[\frac{3}{2}(R_c + R_d) + \frac{4M}{\pi}(R_c - R_d)\cos\phi\right]I_M^2 + \left[\frac{6}{\pi}(V_{c0} + V_{d0}) + \frac{3M}{2}(V_{c0} - V_{d0})\cos\phi\right]I_M \quad (8)$$

Under the assumption of an equivalent modulation strategy as described in [10], the three-level Cascaded H-Bridge inverter can be shown to have the same semiconductor losses as the NPC inverter. Equivalent strategies associate each IGBT-diode module of the NPC inverter to a module of the Cascaded inverter. The losses on IGBTs are equal for respective modules, while losses on the NPC inverter's clamping diodes are transferred to free-wheeling diodes of the Cascaded inverter. The three-phase semiconductor losses for the Cascaded H-Bridge topology can also be calculated using Equations (7) and (8).

4 DC-Link Capacitor RMS Current

In this paragraph, the method of [6], used for the derivation of the two-level inverter capacitor current rms expression, is applied to the three other inverter topologies. The method considers each inverter IGBT-diode module as a switch that, while on, carries the current of the respective phase. The sum of the currents through the upper switches of an inverter is i_d, as shown in Figure 1 for each of the four topologies. The DC component of this current is supplied by the inverter DC source, while the AC component is filtered, and hence carried by the DC-link capacitor. The rms value of the capacitor current, $I_{C,rms}$, is calculated using the average (DC) and rms values of i_d, $I_{d,,DC}$ and $I_{d,,rms}$, respectively:

$$I_{d,rms}^2 = I_{d,DC}^2 + I_{C,rms}^2 \Rightarrow I_{C,rms} = \sqrt{I_{d,rms}^2 - I_{d,DC}^2} \quad (9)$$

According to [6], the calculation of current i_d average and rms values is based on the analysis of its transitions during a single switching period. If i_d is equal to $i_{d,\text{int}1}$, $i_{d,\text{int}2}$, ... during time intervals $T_{\text{int}1}$, $T_{\text{int}2}$, ... , respectively (with $T_{\text{int}k} < T_s$), then its average and rms value during a switching period T_s are given by Equations (10) and (11):

$$i_{d,DC}(\theta) = \frac{1}{T_s}\left(\sum_k T_{\text{int}\,k} \cdot i_{d,\text{int}\,k}\right) = \sum_k \delta_{\text{int}\,k} \cdot i_{d,\text{int}\,k} \quad (10)$$

$$i_{d,rms}^2(\theta) = \frac{1}{T_s}\left(\sum_k T_{\text{int}\,k} \cdot i_{d,\text{int}\,k}^2\right) = \sum_k \delta_{\text{int}\,k} \cdot i_{d,\text{int}\,k}^2 \quad (11)$$

The interval duty cycles $\delta_{\text{int}k}$ and respective currents $i_{d,\text{int}k}$ are functions of θ, the angle of the voltage reference waveform for phase a. The average and rms values of i_d over a fundamental period are obtained using the following expressions:

$$I_{d,DC} = \frac{1}{2\pi}\int_0^{2\pi} i_{d,DC}(\theta)d\theta \quad (12)$$

$$I_{d,rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{d,rms}^2(\theta)d\theta} \quad (13)$$

The expressions for $\delta_{\text{int}k}(\theta)$ and $i_{d,\text{int}k}(\theta)$ may change during sectors of the fundamental cycle. In this case, the above expressions are written as sums of integrals for the different sectors.

For example, for the derivation of the DC-link capacitor current rms expression of the two-level two-channel interleaved inverter, the fundamental cycle is divided into six sectors, each of which covers an angle of π/3. The inverter operation in these sectors is symmetric and hence only one sector needs to be analyzed. Sector I (0 – π/3) is divided into two sub-sectors, as described in Table 2. The table illustrates the duty cycles of the switching intervals and the corresponding values of current i_d as $\delta_{\text{int}k} \rightarrow i_{\text{int}k}$. Angles θ_a, θ_b and θ_c, are equal to:

$$\theta_a = 0, \theta_b = \frac{2\pi}{3} \text{ and } \theta_c = -\frac{2\pi}{3}$$

	Sector I_1	Sector I_2
Duration (θ)	$0 - \pi/6$	$\pi/6 - \pi/3$
T_a / T_s	δ_a	δ_a
T_b / T_s	δ_b	δ_b
T_c / T_s	δ_c	δ_c
Interval 1	$2(1-\delta_c-\delta_b) \rightarrow -i_b/2$	$2(1-\delta_a-\delta_b) \rightarrow -i_b/2$
Interval 2	$2(\delta_c-\delta_a) \rightarrow (i_c-i_b)/2$	$2(\delta_a-\delta_c) \rightarrow (i_a-i_b)/2$
Interval 3	$2(\delta_a-1/2) \rightarrow -i_b$	$2(\delta_c-1/2) \rightarrow -i_b$

Table 2: Switching intervals for the two-level two-channel interleaved inverter

For two-level inverters:

$$\delta_x = \frac{1}{2}\left(1 + M\sin\left(\theta + \theta_x\right)\right) \tag{14}$$

Assuming that the inverter load has a power factor cos(φ), the three-phase currents are given by:

$$i_x = I_M \sin\left(\theta + \theta_x - \phi\right) \tag{15}$$

According to Table 2, for sector I_1:

$$\begin{aligned} i_{d,DC,I1,2L-Int}(\theta) &= 2\cdot\left(1-\delta_c-\delta_b\right)\cdot\left(\frac{-i_b}{2}\right) \\ &+ 2\cdot\left(\delta_c-\delta_a\right)\cdot\left(\frac{i_c-i_b}{2}\right) + 2\cdot\left(\delta_a-1/2\right)\cdot\left(-i_b\right) \end{aligned} \tag{16}$$

$$\begin{aligned} i^2_{d,rms,I1,2L-Int}(\theta) &= 2\cdot\left(1-\delta_c-\delta_b\right)\cdot\left(\frac{-i_b}{2}\right)^2 \\ &+ 2\cdot\left(\delta_c-\delta_a\right)\cdot\left(\frac{i_c-i_b}{2}\right)^2 + 2\cdot\left(\delta_a-1/2\right)\cdot\left(-i_b\right)^2 \end{aligned} \tag{17}$$

Similarly, expressions can be derived for sector I_2. The average (DC) and rms values of i_d are given by:

$$I_{d,DC,2L-Int} = \frac{3}{\pi}\left(\int_0^{\pi/6} i_{d,DC,I1,2L-Int}\,d\theta + \int_{\pi/6}^{\pi/3} i_{d,DC,I2,2L-Int}\,d\theta\right) \tag{18}$$

$$I_{d,rms,2L-Int} = \sqrt{\frac{3}{\pi}\left(\int_0^{\pi/6} i^2_{d,rms,I1,2L-Int}\,d\theta + \int_{\pi/6}^{\pi/3} i^2_{d,rms,I2,2L-Int}\,d\theta\right)} \tag{19}$$

which result in:

$$I_{d,DC,2L-Int} = MI_M\frac{\pi}{4}\cos(\phi) \tag{20}$$

$$I_{d,rms,2L-Int} = I_M\sqrt{\frac{3M}{\pi}\left[\frac{\sqrt{3}-1}{24} + \frac{\sqrt{3}+2}{6}\cos^2(\phi)\right]} \tag{21}$$

The capacitor current rms expression for the two-level interleaved inverter will therefore be given by:

$$I_{C,rms,2L-Int} = I_M\sqrt{\frac{3M}{\pi}\left[\frac{\sqrt{3}-1}{24} + \frac{\sqrt{3}+2}{6}\cos^2(\phi)\right] - \frac{\pi^2 M^2\cos^2(\phi)}{16}} \tag{22}$$

For the three-level NPC inverter, the three-phase voltage and current waveforms are divided into three sectors, covering an interval of $2\pi/3$, each. Sector I is divided into three sub-sectors, as described in Table 3.

	Sector I_1	Sector I_2	Sector I_3
Duration (θ)	$\pi/6 - \pi/3$	$\pi/3 - 2\pi/3$	$2\pi/3 - 5\pi/6$
T_a / T_s	δ_a	δ_a	δ_a
T_b / T_s	0	0	δ_b
T_c / T_s	δ_c	0	0
Interval 1	$\delta_c \rightarrow -i_b$	$\delta_a \rightarrow i_a$	$\delta_b \rightarrow -i_c$
Interval 2	$\delta_a-\delta_c \rightarrow i_a$		$\delta_a-\delta_b \rightarrow i_a$

Table 3: Switching intervals for the three-level NPC inverter

For three-level inverters:

$$\delta_x = M\sin\left(\theta + \theta_x\right) \tag{23}$$

According to Table 3, for sector I_1:

$$i_{d,DC,I1,NPC}(\theta) = \delta_c\cdot(-i_b) + \left(\delta_a-\delta_c\right)\cdot i_a \tag{24}$$

$$i^2_{d,rms,I1,NPC}(\theta) = \delta_c\cdot(-i_b)^2 + \left(\delta_a-\delta_c\right)\cdot i_a^2 \tag{25}$$

Similar expressions are derived for sectors I_2 and I_3. The DC and rms values of i_d for the NPC inverter are derived using equations similar to (18) and (19), which result in:

$$I_{d,DC,NPC} = \frac{3}{4}MI_M\cos\phi \tag{26}$$

$$I_{d,rms,NPC} = I_M\sqrt{\frac{\sqrt{3}M}{4\pi}\left[1+\cos^2(\phi)\right]} \tag{27}$$

Use of Equation (9) here gives the current rms expression for the upper capacitor of the three-level NPC inverter. Due to symmetry, the expression for the lower capacitor is identical:

$$I_{C,rms,NPC} = I_M\sqrt{\frac{M}{2}\left[\frac{\sqrt{3}}{2\pi} + \left(\frac{2\sqrt{3}}{\pi} - \frac{9}{8}M\right)\cos^2(\phi)\right]} \tag{28}$$

The derivation of the DC-link capacitor current rms for the three-phase Cascaded H-Bridge inverter is based on the analysis of a single H-Bridge, that of phase *a*. The current rms value of each capacitor in this topology is not affected by the switching operations of the other phases. The calculation of the capacitor rms current is based on the analysis of one out of two symmetrical sectors, covering an interval of π, each.

Duration (θ)	$0 - \pi$
T_a / T_s	δ_a
Interval 1	$\delta_a \rightarrow i_a$

Table 4: Switching intervals for phase *a* of the three-level Cascaded H-Bridge inverter

According to Table 4:

$$i_{d,DC,Casc}(\theta) = \delta_a\cdot i_a \tag{29}$$

$$i^2_{d,rms,Casc}(\theta) = \delta_a\cdot i_a^2 \tag{30}$$

The average (DC) and rms values of current i_d for the Cascaded H-Bridge inverter are calculated using Equations (12) and (13), respectively, which result in:

$$I_{d,DC,Casc} = \frac{MI_M}{2}\cos(\phi) \quad (31)$$

$$I_{d,rms,Casc} = I_M\sqrt{\frac{M\left(3+\cos(2\phi)\right)}{3\pi}} \quad (32)$$

The capacitor current rms expression for this topology can be calculated using (9), (31) and (32) to be:

$$I_{C,rms,Casc} = I_M\sqrt{\frac{M}{24\pi}\left[24-3M\pi+\left(8-3M\pi\right)\cos(2\phi)\right]} \quad (33)$$

The DC-link capacitor current of a single-phase H-Bridge has been investigated in [20], deriving an expression for the rms value of high frequency capacitor current harmonics. This expression is equivalent to (33), which also incorporates the low-frequency harmonic of the Cascaded H-Bridge inverter DC-link capacitor current. All the above derived capacitor current rms expressions were verified by inverter simulations in the SimPowerSystems toolbox of Matlab-Simulink.

5 Results

All inverters are assumed to supply a 3Ω impedance (*Z*) load with power factor equal to 0.9. Due to the increased switching losses of high-voltage IGBTs, however, two-level inverters are assumed to be switched at lower frequencies. The switching frequency f_s is set to 1kHz for two-level and 2.5kHz for three-level inverters, respectively. Figure 2 plots the semiconductor losses against the inverter Modulation Index *M*, according to Equations (3)-(8) and the values of Table 1. An inspection of the plot indicates that the switching losses of the two-level inverters are significantly higher than that of the three-level inverters. Even though the switching frequencies of the two-level inverters are lower, three-level inverters exhibit a major advantage over switching losses, as a result of their decreased switching parameter values ($a_{c/d}$ and $b_{c/d}$). The decreased number of output voltage levels and the lower switching frequencies also have a negative impact on the output harmonic performance of the two-level inverters, but this consideration is beyond the scope of this paper.

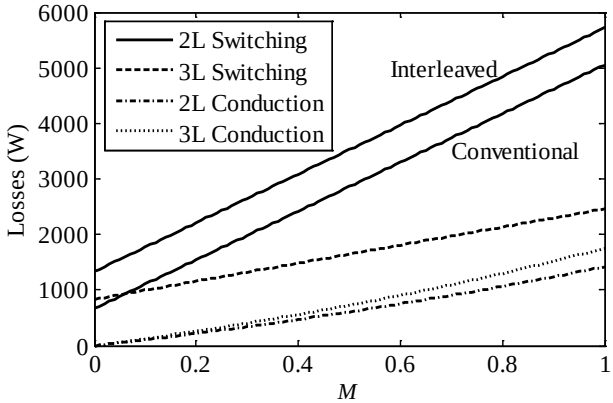

Figure 2: Semiconductor losses vs *M*

The conduction losses of the two two-level inverters are equal due to the values of conduction parameters $R_{c/d}$, which are half for the interleaved inverter modules (see Equations (4) and (6)). Conduction losses for three-level topologies are slightly higher.

The DC-link capacitors power losses are given by the following expression:

$$P_C = N \cdot R_C \cdot I_{C,rms}^2 \quad (34)$$

where *N* is the number of capacitors used in each topology and R_c represents the Equivalent Series Resistance (ESR) of each capacitor. As shown in Figure 1, *N* is equal to 2 for the two two-level and the three-level NPC inverters, and 3 for the Cascaded H-Bridge inverter. Each capacitor (or capacitor bank) is assumed to have a nominal voltage of 1kV and an ESR of 15mΩ.

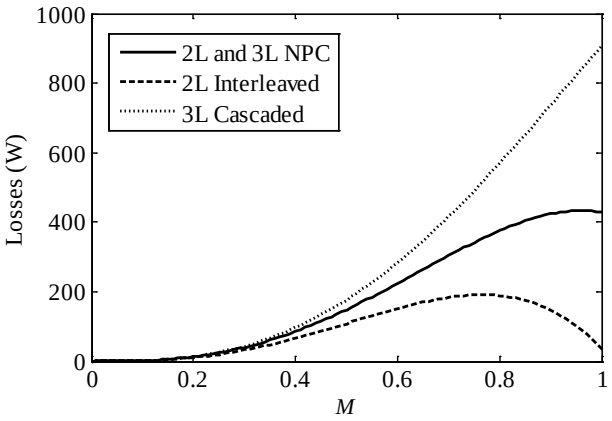

Figure 3: DC-link capacitor losses vs *M*

Figure 3 illustrates the variation of total DC-link capacitor losses with modulation index for the examined topologies. As shown in the figure, the two-level interleaved inverter has the lowest amount of DC-link capacitors losses. The capacitor losses in the conventional two-level inverter are higher and equal to the three-level NPC inverter losses. In fact, the expressions for the capacitor current rms values of these two topologies are identical. However, according to inverter simulations, their instantaneous capacitor currents and current spectra differ significantly. In contrast to the two-level inverter, the capacitor current of the three-level NPC inverter contains low-frequency harmonics. Low-frequency harmonics also appear in the capacitor current of the three-level Cascaded H-Bridge inverter. This topology has the highest amount of capacitor losses, partially due to the fact that it uses three instead of two DC-link capacitors.

A fixed value of ESR was assumed for all DC-link capacitors. In reality, the ESR of electrolytic capacitors that are commonly used for inverter DC-links, varies with the frequency of capacitor current harmonics. Its value for low frequencies, in the range of hundreds of Hz, is two to three times higher than it is for frequencies in the range of kHz.

Losses for the three-level inverters, whose capacitors carry low-frequency capacitor currents, will therefore be higher than predicted by (34). DC-link capacitor sizing for these topologies must consider this expected increment.

A final remark refers to the losses in two-level interleaved inverters. Results were presented assuming that all topologies supply the same current (with magnitude I_M and phase φ) to the load, for the given DC-link voltages. However, the leg inductors of the interleaved inverter increase the apparent load inductance (by $L_f/2$), hence decreasing the load current and increasing the power angle φ. The inductance of the leg inductors was here assumed to be small compared to the load inductance. In practice, the DC-link voltage is increased to compensate for the inductor voltage drop.

6 Conclusion

The paper examined and compared the semiconductor and DC-link capacitor losses of four inverter topologies. The semiconductor losses of the conventional and interleaved two-level inverters proved to be significantly higher than the respective losses of the NPC and Cascaded H-Bridge three-level inverters. Switching losses that dominate in the two-level inverters are increased even for low switching frequencies, due to the high-voltage IGBT-diode modules that these topologies use. The interleaved inverter has higher switching losses than the conventional two-level inverter. Semiconductor losses for the three-level topologies are lower and equal for the NPC and Cascaded H-Bridge inverters, assuming an equivalence of their modulation strategies.

In terms of DC-link capacitor losses, the interleaved inverter can achieve better results than the conventional two-level inverter. Capacitor losses in the conventional two-level and three-level NPC inverters proved to be equal. The Cascaded H-Bridge inverter, on the contrary, has significantly more capacitor losses than these two topologies. Lower DC-link capacitor losses of the two-level inverters cannot compensate for their increased semiconductor losses. Given the equality of three-level inverter semiconductor losses, the NPC inverter proved to be the most efficient between the four topologies.

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