Analysis of DC-Link Capacitor Losses in Three-Level Neutral Point Clamped and Cascaded H-Bridge Voltage Source Inverters

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***Abstract*-Loss estimation is a critical aspect of inverter design. The present work investigates the losses occurring in the DC-link capacitors of the three-phase three-level Neutral Point Clamped and Cascaded H-Bridge inverter topologies, by performing a harmonic analysis of the capacitor currents. Results are verified by simulations. Their analysis reveals the advantage of the NPC inverter.**

I. INTRODUCTION

An essential part of voltage source inverter (VSI) design is the selection of DC-link capacitors. The capacitors are a sensitive element of the inverter and a common source of inverter failures. Capacitor lifetime is highly affected by thermal stresses that occur due to internal capacitor losses. DC-link capacitor losses can be significant, hence shortening the capacitor lifetime and decreasing the inverter power output. An accurate estimate of these losses can contribute in the design processes of sizing the inverter DC-link capacitors and estimating the efficiency of the inverter.

Losses in a DC-link capacitor occur because of its Equivalent Series Resistance (ESR). The rms value of the total current flowing through a capacitor can provide a first approximation for its losses. The literature contains rms expressions for the capacitor current of the two-level [1] – [3] and the three-level Cascaded H-Bridge inverters [4]. Use of these expressions for loss estimation assumes a fixed ESR value. However, the ESR is a function of the frequency of the capacitor current [5], [6]. Since the current of a DC-link capacitor comprises several harmonics located at different frequencies, it is necessary, for accurate calculation of losses, to determine the rms values of the capacitor current harmonics and use the appropriate value of ESR for each harmonic. The losses can be then estimated as the sum of the losses caused by the different harmonics.

A harmonic analysis of DC-link capacitor current has been derived in [7] for the two-level inverter. This paper extends this analysis to the three-level Neutral Point Clamped (NPC) and Cascaded H-Bridge inverters topologies. The resulting current spectra and a capacitor ESR – frequency characteristic are used to provide estimates of the DC-link capacitor losses in the two three-level topologies as well as the two-level topology.

Losses are also estimated using the rms value of the total capacitor current and a single value for the ESR. The three topologies are compared on the basis of both of these estimates. Throughout the analysis, a ripple-free DC current is assumed to be supplied by the inverter DC sources.

Section II gives a description of capacitor ESR characteristics and relates them to expressions used for estimating capacitor lifetime. Section III presents expressions for the rms values of the DC-link current in the three topologies and uses these values to calculate the DC-link capacitor losses based on a constant value of the ESR. The method that is used for the analysis of DC-link current harmonics is summarized in Section IV, along with the results of its application to a two-level inverter. Section V contains the main part of the present work, which is concerned with the derivation of the analytical expressions for the DC-link current spectra of the three-level Neutral Point Clamped (NPC) and Cascaded H-Bridge inverters. The results are presented and validated in Section VI. The comparison between the three topologies is included in the same section. Section VII discusses the use of capacitor total current rms expressions and a fixed value of ESR for loss estimations and Section VII summarizes the final conclusions.

II. CAPACITOR ESR CHARACTERISTICS

The Equivalent Series Resistance of a DC-link capacitor varies with the frequency of the capacitor current. A typical ESR – frequency characteristic is illustrated in Fig. 1 [5].

In case that more than one current harmonics h, with rms values $I_{h,rms}$ and frequencies f_h flow through the capacitor, the losses P occurring on the capacitor's ESR can be calculated using equation (1) below, where $R_C(f_h)$ stands for the value of ESR at frequency f_h.

$$P = \sum_h R_C\left(f_h\right) \cdot I_{h,rms}^2 \tag{1}$$

Losses affect the capacitor lifetime, since they cause heat dissipation and thermal stress. A factor K_{Ripple} is used by capacitor manufacturers to quantify the effect of current ripple on capacitor lifetime.

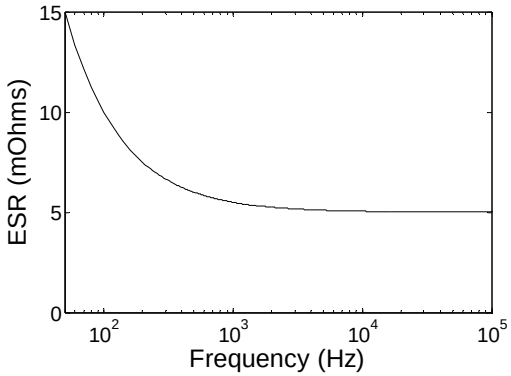

Fig. 1. ESR – frequency characteristic of a 4.7mF / 450V capacitor [5].

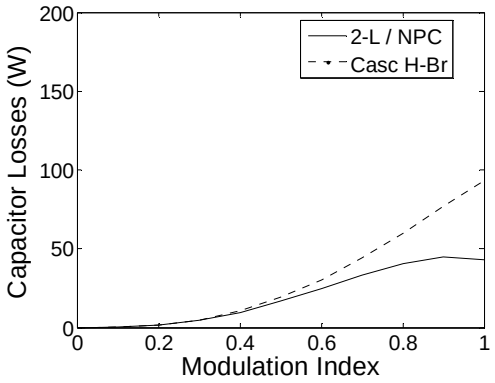

Fig. 2. Capacitor losses estimated using total current rms expressions.

K_{Ripple} is given by the following equation [6]:

$$K_{Ripple} = 2^{(\Delta T - \Delta T_0)/5},$$

$$\Delta T = \Delta T_0 \cdot \sum_h \left(\frac{I_h}{I_0 F_h} \right)^2 = \Delta T_0 \cdot \sum_h \frac{R_C(f_h)}{R_C(f_0)} \left(\frac{I_h}{I_0} \right)^2 \quad (2)$$

where ΔT_0 represents the increase in capacitor core temperature due to the rated ripple current, I_0 and f_0 represent the rated ripple current's amplitude and frequency, and I_h and f_h represent the amplitude and frequency of current harmonic h. F_h is a current multiplier given in data sheets or derived from the ESR characteristic.

III. DC-LINK CURRENT RMS VALUES

The rms value of the capacitor current can provide a first approach to estimating its losses, using the equation below:

$$P = R_C I_{rms}^2 = R_C \sum_h I_{h,rms}^2 \quad (3)$$

The use of rms values for the estimation of losses implies an assumption of constant capacitor ESR value R_C, throughout the whole frequency range. Section VII examines the conditions under which this assumption can lead to acceptable loss estimations. Equations that give the current rms values of the two-level and three-level NPC and Cascaded H-Bridge inverters are included in the Appendix. Their derivation for the case of the two-level inverter can be found in [1] – [3]. The three-level inverter equations are part of unpublished work [8]. An equivalent result for the Cascaded H-Bridge inverter is also found in [4]. It is important to note that the two-level inverter has the same rms value of capacitor current as the three-level NPC inverter. An rms-based loss estimation gives equal results for these two topologies and higher values for the Cascaded H-Bridge inverter. Fig. 2 illustrates the variation of capacitor losses with Modulation index for the three topologies. The values of the expression parameters are summarized in Table I.

TABLE I
LIST OF PARAMETERS

Quantity	Symbol	Value	Unit
DC-link voltage	V_{dc}	800	V
Fundamental frequency		50	Hz
Carrier frequency		2	kHz
Load resistance	R_L	2	Ohm
Load inductance	L_L	2	mH
Load power factor	cos(φ)	0.954	

IV. DC-LINK CURRENT HARMONICS

A more accurate approximation of DC-link capacitor losses requires a harmonic analysis of the capacitor current. The method used to analytically derive the current spectra is the well-known geometric wall model, introduced by H. S. Black in [9]. The method has been widely applied for analyzing the harmonics of the output voltage of different inverter topologies and PWM strategies [10]. The authors of [7] used this model for the analysis of the DC-link capacitor currents of a two-level inverter. The resulting spectra are combined with the ESR characteristics as shown in (1) to provide a more accurate estimation of the losses than that provided by (3).

A. Summary of Black's Geometric Wall Model

The geometric wall model provides an alternative way for representing the process of pulse generation in PWM converters. The carrier and reference waveforms are redrawn in a transformed plane, so that the intersections between the new waveforms define the same train of pulses as the original PWM method. The carrier waveform in this plane turns into a straight line (assuming natural sampling) and the reference waveform is transformed accordingly to form closed regions referred to as contour plots. The width of the generated pulses is periodic with respect to both dimensions of the new plane. The function that describes the pulse train can therefore be written as a double Fourier series. The Fourier analysis results in a spectrum that plots the function in the frequency domain.

B. *Analysis of DC-Link Capacitor Current using the Geometric Wall Model*

The geometrical wall model has been widely applied for the harmonic analysis of voltage pulse trains, as mentioned earlier. The model provides the points of waveform intersections that define the pulse widths. These points are used to chop a constant waveform, whose amplitude is equal to the pulse height, and convert it to a pulse train. When studying converter output voltages, this constant waveform is the DC-bus voltage.

In the case of DC-link capacitor current, the waveform that has to be chopped is a sinusoidal output current of the inverter (assuming in this paper a sinusoidal current at fundamental frequency). For the cases of integer carrier to fundamental frequency ratios only, the resulting (chopped) current waveform is periodic, so it can be analyzed by the geometrical wall model and expressed as a double Fourier series. However, an extension of the Fourier coefficient integrals (see (4) for example) over a large number of fundamental periods also yields identical expressions for the Fourier coefficients, while covering the cases of non integer frequency ratios [10].

The DC-link capacitor current harmonics of a two-level inverter were analyzed in [7]. The derivation was based on the current of the IGBT/Diode module V1 of phase A that is connected to the positive-end of the inverter's DC-bus. The Fourier coefficients of this current were proved to be given by (4) below, where $M(y)$ is the function that defines the voltage reference waveform and I_L represents the amplitude of the load current.

$$ {}^{mn}i_{V1} = \frac{I_L}{2\pi^2} \int_0^{2\pi} \int_{\frac{\pi}{2}(1-M(y))}^{\frac{\pi}{2}(3+M(y))} \cos(y-\phi) \cdot e^{j(mx+ny)} dxdy \quad (4) $$

The respective coefficients for the currents of the upper modules V3 and V5 of inverter phases B and C are given by (4), multiplied by $e^{+2jn\pi/3}$ and $e^{-2jn\pi/3}$, respectively. Since the capacitor current is the complex sum of these three module currents, excluding the DC component that is assumed to come from the DC source, the capacitor current Fourier coefficients can be calculated using the following equation:

$$ {}^{mn}i_C = {}^{mn}i_{V1} + {}^{mn}i_{V3} + {}^{mn}i_{V5} \quad (5) $$

V. DC-LINK CURRENT HARMONICS OF THREE-LEVEL INVERTERS

A. *Neutral Point Clamped Inverter*

As in the two-level inverter, the instantaneous current flowing through the DC-link capacitor of the NPC inverter is the complex sum of the currents through the inverter's three upper modules (V1A, V1B, V1C), shown in Fig. 3. Harmonic analysis of one of these module currents is sufficient to calculate the DC-link capacitor current harmonics.

The following solution is given for the three-level Phase-Disposition Pulse Width Modulation (PD PWM) method using two in-phase triangular carriers and a sinusoidal reference waveform. The application of the geometric wall model to the three-level PD PWM results into the wall model contour plot illustrated in Fig. 4 [10]. According to this plot, the output voltage for phase A is positive only in the closed region at the center of the graph. Hence, this is the region where module V1A carries the current of phase A. The complex Fourier coefficients of i_{V1A} will therefore come from (6).

$$ {}^{mn}i_{V1A} = \frac{I_L}{2\pi^2} \int_{-\pi/2}^{\pi/2} \int_{-\pi M\cos y}^{\pi M\cos y} \cos(y-\phi) \cdot e^{j(mx+ny)} dxdy \quad (6) $$

The results are summarized in the Appendix. The capacitor current coefficients are given by a complex sum like (5), for modules V1A, V1B and V1C.

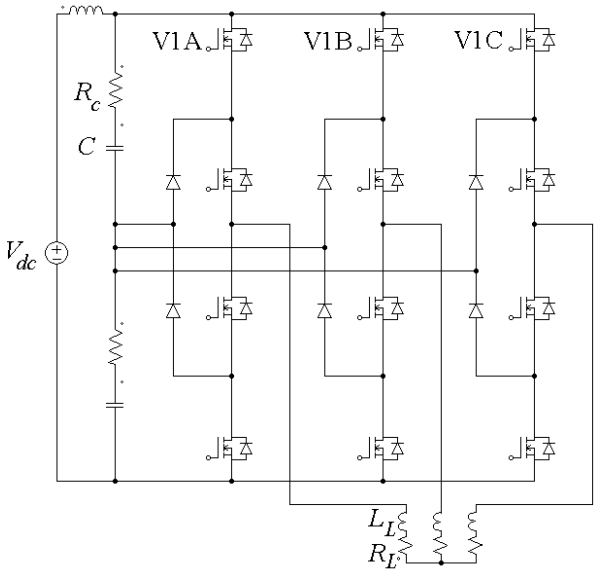

Fig. 3. Three-phase three-level Neutral Point Clamped inverter.

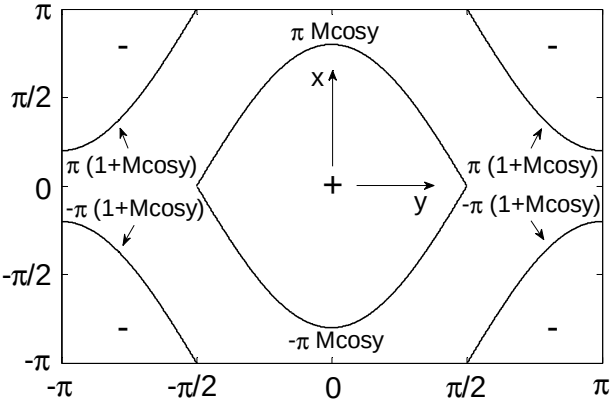

Fig. 4. Contour plot for the three-level PD PWM method [10].

B. *Cascaded H-Bridge Inverter*

Unlike the NPC inverter, the current of each capacitor in this topology is only determined by the operation of the respective H-Bridge. Hence, the derivation of a capacitor current is not given by an equation in the form of (5). The current that will be harmonically analyzed for this topology will be i_{dA}, as shown in Fig. 5. The AC component of this current flows through the DC-link capacitor of phase A.

Since the purpose of the present analysis is to perform a comparison between inverter topologies, it is important to select a switching method for the Cascaded H-Bridge inverter that is equivalent to PD PWM for the NPC inverter. A discontinuous PWM method, that yields equal switching losses and the same output voltage spectra for the two topologies, is described in pages 504 – 506 of [10]. Pulse generation is again based on the contour plot of Fig. 4. The output voltage for phase A is positive in the region at the center of the plot and negative in the regions at the edges. The current i_{dA} of the Cascaded H-Bridge inverter is therefore equal to the phase current i_A, or the opposite of it ($-i_A$) in the respective regions. Its Fourier coefficients are given by (7).

$$ {}^{mn}i_{dA} = \begin{cases} \dfrac{I_L}{\pi^2} \displaystyle\int_{-\pi/2}^{\pi/2} \int_{-\pi M\cos y}^{\pi M\cos y} \cos(y-\phi)\cdot e^{j(mx+ny)}\,dx\,dy, \\ \quad for\ n+m \rightarrow even \\ \\ 0, \quad for\ n+m \rightarrow odd \end{cases} \quad (7) $$

The Appendix contains the detailed results. Apart from the DC component, the capacitor current of phase A is harmonically described by the coefficients of i_{dA}.

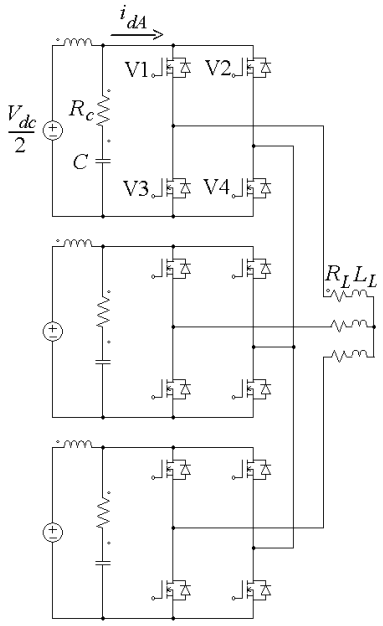

Fig. 5. Three-phase three-level Cascaded H-Bridge inverter.

VI. Validation of DC-link Current Spectra and Comparison of Inverter Losses

The two three-level inverter topologies were simulated in the SimPowerSystems Toolbox of Matlab – Simulink. This Section presents the DC-link current spectra derived using the results of the harmonic analysis and compares them with the spectra that were taken from the simulations. Fig. 6 and Fig. 7 illustrate representative results for the NPC and Cascaded H-Bridge inverters, respectively, for the operating parameters summarized in Table I and a Modulation index equal to 0.85. The analytically-derived spectra were validated by simulations for a wide range of operating parameter values (Modulation index, load power factor, fundamental and carrier frequencies).

Based on the results of the harmonic analysis, DC-link losses were estimated assuming that the capacitor ESRs follow the characteristic of Fig. 1. The NPC and the Cascaded H-Bridge inverters use two and three of these capacitors, as shown in Fig. 3 and Fig.5, respectively. The two-level inverter that is also included in the comparison uses two capacitors, connected in series.

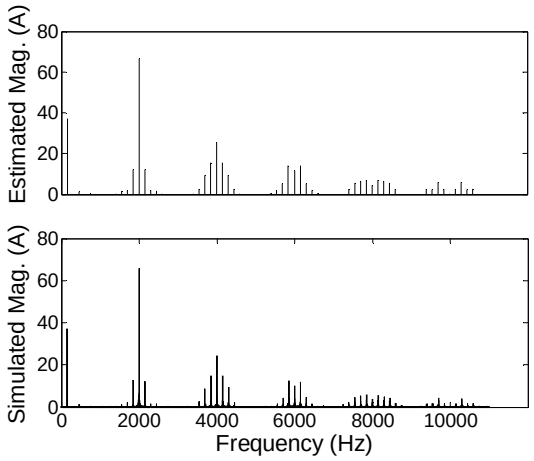

Fig. 6. Estimated and simulated spectra of the NPC inverter.

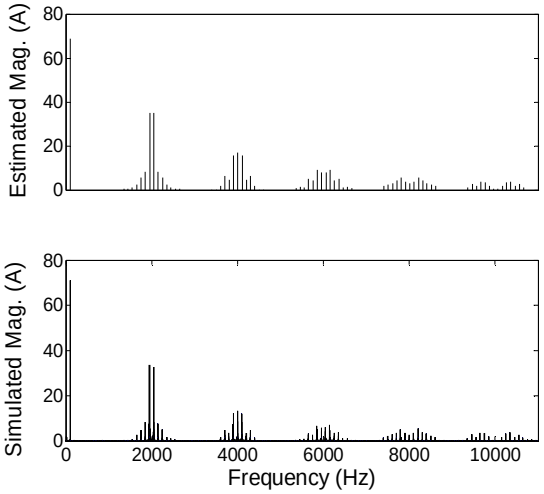

Fig. 7. Estimated and simulated spectra of the Cascaded H-Bridge inverter.

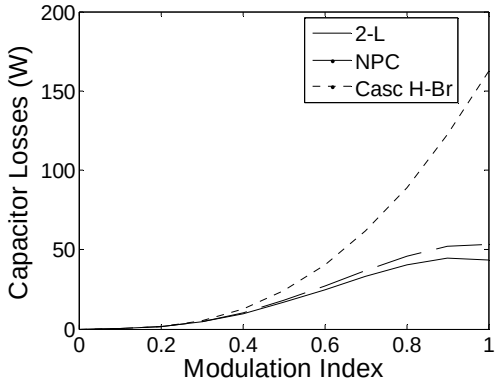

Fig. 8. Capacitor losses estimated using harmonic analysis

A plot of the estimated DC-link losses of the three topologies against the Modulation index is shown in Fig. 8. The plot indicates that the Cascaded H-Bridge inverter has the highest amount of losses. The losses in the DC-link of the NPC inverter are significantly lower, while from the same aspect, the two-level inverter is the most efficient among the studied topologies.

VII. DISCUSSION

Comparison of the two plots in Fig. 2 and Fig. 8 reveals that for the three-level topologies there is a notable deviation between the loss estimations based on the DC-link current rms expressions which assume a constant capacitor ESR, and the harmonic analysis, respectively. In contrast, the estimations are similar for the case of the two-level inverter. This difference is attributable to the shape of the electrolytic capacitor ESR characteristics.

A close examination of ESR characteristics of electrolytic capacitors indicates that their ESR decreases for harmonic frequencies between 50 Hz and 1 kHz, while it remains approximately constant for higher frequencies. Additionally, inverter switching (carrier) frequencies are commonly higher than 1 kHz. As a result, the majority of carrier and sideband harmonic groups, which appear around multiples of the switching frequency, belong in the constant-ESR frequency range. Fundamental and baseband harmonics, however, have to be associated with higher ESR values, according to (1). Loss estimation based on current rms expressions (3) fails to treat these harmonics separately, which results in an underestimation of DC-link capacitor losses for the three-level inverters. The DC-link capacitor current of the two-level inverter on the other hand does not contain any fundamental or baseband harmonics [7]. Hence, the respective rms expression and the harmonic analysis give similar results for this topology.

It is worth mentioning that in the common case of an inverter that uses electrolytic capacitors for its DC-link and switches at a moderate frequency, a complete harmonic analysis may not be necessary for the estimation of losses. The capacitor current rms expressions can be used according to (8) below to provide DC-link capacitor loss estimations. Harmonic analysis is still necessary to obtain the amplitudes and frequencies of fundamental and baseband harmonics, but does not need to extend to carrier and sideband harmonics. The subscripts *F/B* under the sums in (8) denote that they refer to the fundamental and baseband harmonics only. In the second term, R_C corresponds to the high frequency constant value of the ESR.

$$P = \sum_{F/B} R_C(f_h) \cdot I_{h,rms}^2 + R_C \cdot \left[I_{rms}^2 - \sum_{F/B} I_{h,rms}^2 \right] \qquad (8)$$

Equation (8) is not applicable to inverters that operate at low switching frequencies or use capacitors with different ESR characteristics. In these cases, certain carrier – sideband harmonic groups may belong to the low frequency ESR region and therefore the results of a complete harmonic analysis should be used according to (1).

Two-level inverters generally switch at lower frequencies compared to three-level inverters with the same power output, because of their higher voltage-rated power semiconductor modules. They are therefore more likely to have low frequency carrier and sideband harmonics. Increased ESR values for these harmonics can decrease or reverse the advantage that the two-level inverters have over the three-level topologies, and particularly the NPC.

VIII. CONCLUSION

This paper investigated the losses occurring in the DC-link capacitors of the three-level NPC and Cascaded H-Bridge inverter topologies. The three-level NPC inverter was proved to have a significant advantage over the Cascaded H-Bridge inverter in terms of its DC-link losses. The two-level inverter that was also examined performs better than both the three-level topologies, under the assumption of similar switching frequencies. In practice, a two-level inverter may need to switch at a lower frequency than the NPC due to using higher voltage devices, in which case its capacitor losses may be higher than those of the NPC inverter.

Loss estimations obtained by harmonic analysis were compared with estimates based on total DC-link capacitor current rms expressions. The comparison indicated that the latter are likely to underestimate the capacitor losses of three-level inverters because they use a fixed value for the capacitor ESR. However, fundamental and baseband harmonics can be combined with the total rms current expressions to give more accurate estimates of capacitor losses.

APPENDIX

A. Neutral Point Clamped Inverter

The expression that gives the DC-link capacitor total current rms value for the three-level NPC inverter can be shown to be identical to that of the two-level inverter [8].

$$I_{NPC,rms} = I_L \sqrt{\frac{M}{2}\left[\frac{\sqrt{3}}{2\pi} + \left(\frac{2\sqrt{3}}{\pi} - \frac{9}{8}M\right)\cos^2(\phi)\right]} \quad (9)$$

The solution of (6) provides the complex Fourier coefficients for the current of the upper DC-link capacitor of the three-level NPC inverter as follows:

Baseband harmonics, for n = 3, 9, 15, …:

$${}^{0n}i_{C,NPC} = (-1)^{\frac{n-1}{2}} \frac{6MI_L}{\pi\left(n^2-4\right)}\left(\frac{2\cos\phi}{n} + j\sin\phi\right) \quad (10)$$

Carrier harmonics, for m = 1, 2, 3, …:

$${}^{m0}i_{C,NPC} = -\frac{3I_L}{m\pi} J_1(Mm\pi)\cos\phi \quad (11)$$

Sideband harmonics, for n even and m = 1, 2, 3, …:

$${}^{mn}i_{C,NPC} = (-1)^{\frac{n}{2}} \frac{3I_L}{2m\pi}\begin{bmatrix} e^{j\phi}J_{n-1}(Mm\pi) \\ -e^{-j\phi}J_{n+1}(Mm\pi)\end{bmatrix} \quad (12)$$

Sideband harmonics, for n odd and m = 1, 2, 3, …:

$${}^{mn}i_{C,NPC} = (-1)^{\frac{n-1}{2}} \frac{6I_L}{m\pi^2} \sum_{k=1,3,5...} J_k(Mm\pi)\cdot$$

$$\left[\frac{\cos\phi + j(n+k)\sin\phi}{1-(n+k)^2} - \frac{\cos\phi + j(n-k)\sin\phi}{1-(n-k)^2}\right] \quad (13)$$

B. Cascaded H-Bridge Inverter

The DC-link capacitor current rms value for the three-level Cascaded H-Bridge topology can be shown to be given by the following expression [4], [8]:

$$I_{Casc,rms} = I_L \sqrt{\frac{M}{24\pi}\left[24 - 3M\pi + (8 - 3M\pi)\cos(2\phi)\right]} \quad (14)$$

Solution of (7) provides the complex Fourier coefficients for the current of the DC-link capacitor of phase A.

Baseband harmonic, for n = 2, only:

$${}^{02}i_{C,Casc} = \frac{MI_L}{2} e^{j\phi} \quad (15)$$

Carrier harmonics, for m even:

$${}^{m0}i_{C,Casc} = -\frac{2I_L}{m\pi} J_1(Mm\pi)\cos\phi \quad (16)$$

Sideband harmonics, for n even and m even:

$${}^{mn}i_{C,Casc} = (-1)^{1+\frac{n}{2}} \frac{I_L}{m\pi}\begin{bmatrix} e^{j\phi}J_{n-1}(Mm\pi) \\ -e^{-j\phi}J_{n+1}(Mm\pi)\end{bmatrix} \quad (17)$$

Sideband harmonics, for n odd and m odd:

$${}^{mn}i_{C,Casc} = (-1)^{\frac{n+1}{2}} \frac{4I_L}{m\pi^2} \sum_{k=1,3,5...} J_k(Mm\pi)\cdot$$

$$\left[\frac{\cos\phi + j(n+k)\sin\phi}{1-(n+k)^2} - \frac{\cos\phi + j(n-k)\sin\phi}{1-(n-k)^2}\right] \quad (18)$$

Note that the amplitude I_L of the load current is the same for all topologies and is determined by the voltage V_{dc}, the Modulation index M and the load impedance Z_L at the fundamental frequency, according to the following equation:

$$I_L = \frac{MV_{dc}}{2|Z_L|} \quad (19)$$

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