Design of a Robust Digital Current Controller for a Grid Connected Interleaved Inverter

M. A. Abusara and S. M. Sharkh
School of Engineering Sciences,University of Southampton,
Highfield,Southampton SO17 1BJ,United Kingdom.
Tel +44 2380 594641,Fax +44 2380 593053
Email: suleiman@soton.ac.uk

***ABSTRACT*-This paper is concerned with the design and practical implementation of a robust digital current controller for a three-phase voltage source grid-connected interleaved inverter. Each phase consists of 6 half-bridge channels connected in parallel. Due to the current ripple cancellation of the interleaving topology, only small output filter capacitors are required which provide high impedance to grid voltage harmonics and hence better current quality compared to traditional 2-level *LCL* topology. The current in each inductor is controlled via a single feedback loop. A feedforward loop of the grid voltage is incorporated to compensate for the grid disturbance. To control the high resonance frequency of the filter, high sampling and switching frequencies are required. Alternatively, resistors in series with the filter capacitors are used to provide damping. This method becomes practically possible due to the low magnitude of the current of the capacitors and consequently low power dissipation in the damping resistors. The paper also studies in detail the effects of computational time delay and grid impedance variation on system stability. A phase lag compensator incorporated in the inductor current loop is designed to increase system immunity to grid impedance variations. Simulation and practical results are presented to validate the design.**

I. INTRODUCTION

In recent years, distributed generators (DG) have been widely used to generate electricity. They provide an alternative or an enhancement to the traditional electric power system. Advantages of using DG include reduction of electricity transmission losses, reduction of the size of power lines, low pollution, and high efficiencies. A typical DG consists of an electrical energy source and a power electronic interface. Examples of electrical sources include fuel cells, solar cells, wind turbines, flywheel, and batteries. Most of the commercially available power electronic interface inverters are based on the two-level voltage source topology [1]-[4]. However, the need to improve efficiency and reduce size and cost of both the inverter and the output filter encouraged more research into using different inverter topologies. A 3-level inverter topology has been shown to halve the output inductor ripple current for a given switching frequency, thus reducing the size of the inductor. Additionally, the power switches in a 3-level inverter need only have half the voltage rating of the power switches in a 2-level inverter, and hence have faster switching frequencies, thus enabling further reduction in filter size [5]-[7].

In this paper we investigate an alternative topology, namely an interleaved inverter topology. The multiphase interleaved topology has been recently gaining popularity in DC/DC and AC/DC converter applications [8]-[12]. Interleaving is a form of paralleling technique where a single converter channels, e.g., half a bridge with an output inductor, is replaced by a number of smaller channels connected in parallel whose switching instants are phase shifted equally over a switching period. By introducing such a phase shift, the total capacitor ripple current is greatly reduced due to the ripple cancelation effect which in turn reduces the size of the required filter capacitor. Additionally, the inductor size is proportional to LI^2 [13] which means that replacing a single inductor by N smaller inductors of the same inductance value, each carrying (I/N) of the original current, could reduce the total size of inductors by ($1/N$). Furthermore, sharing the current among multi channels enables the use of smaller power switches which can switch at a higher frequency thus allowing a further reduction in inductor size. Also, The switching losses are spread over several components that can be cooled more effectively. Although replacing one channel by several requires more gate drives and more current sensors, the improvement in terms of size reduction may justify the extra complexity.

In addition to the benefits mentioned above for the interleaving topology for DC/DC applications, using this topology in grid-connected inverters will help overcome some of the problems inherent in the two-level and multi-level inverters. The need for a large filter capacitor to filter out the switching frequency ripple in these traditional topologies provides a low system output impedance and hence an easy path for harmonic currents caused by grid voltage harmonics. In the interleaved topology, much small filter capacitors are required thanks to the ripple cancellation feature. This also eliminates the need for a second output filter inductor (i.e. using an *LCL* filter instead of an *LC* filter) that is normally used in 2-level and multi-level grid connected inverters to block the switching ripple in cases where the grid impedance is too low. Furthermore, the resonance frequency of the interleaved system will be high due to the much smaller output filter capacitors and inductors. This gives more headroom for increasing the controller gain at lower harmonic frequencies in order to suppress the low harmonic currents caused by grid voltage harmonic distortion.

This paper focuses on the design of the control system of a 6-channel 3-phase grid connected interleaved inverter. The inverter system is first described in sections II. Section III derives a model of the system, section IV discusses the design of the control system, and section V presents simulation and practical results.

II. System Description and Controller Structure

A schematic diagram for the inverter is shown in Fig. 1 and the system parameters are listed in Table 1. The half bridge leg of the inverter is made of N=6 channels in parallel. The optimal selection of the number of channels, switching devices and filter parameters, and the design of the filter components are outside the scope of this paper, but will be the subject of future publications. In general, the choice of the number channels is constrained by practical considerations of the maximum possible switching frequency of the IGBTs with the appropriate voltage rating, overall efficiency of the inverter and availability of suitable filter components. The output of each channel is connected to a common point of coupling to the grid through the inductance L, carrying a share I_{Lx} (x=1..6) of the total current I_L such that

$$I_L = NI_{Lx} \tag{1}$$

The common points of the three-phases are connected to star-connected capacitors C in series with resistors R. The voltage sources V_u and the inductances L_u (with subscripts a, b and c for the three phases) represent the grid equivalent circuit, and I_{Out} is the grid current.

The three phases of the inverters are controlled independently. Fig. 2 shows the block diagram of the PWM inverter and filter and the control system of one of the phases. The model assumes balanced three-phase currents and hence the voltage of the star point of the filter capacitors is at the same potential as the grid neutral point. The current in each inductor is controlled using a single feedback loop with a digital controller $K(z)$. A feedforward loop of the grid voltage at the point of common coupling V_G is also included to cancel the grid voltage disturbance, as discussed in [5]. A second feedback loop of the capacitor current to provide active damping as discussed in [5] was not implemented as the sampling frequency f_s (35kHz) is only 1.47 to 3.2 times the natural damped frequency f_d, depending on the value of the grid inductance as shown in Table 2, which is too low to provide effective damping. In order to control the system resonance frequency, the sampling rate needs to be at least 8 to 10 times faster than the natural damped frequency f_d [14]. Instead, a resistor in series with the filter capacitor is used to provide passive damping. Fortunately, due to the ripple cancellation feature of the interleaving topology, the capacitor current is quite small and hence the power dissipation in R is also small and the losses are acceptable.

The time delay T_d caused by the controlling processor computational time is modeled as $e^{-T_d s}$. The Analogue to digital converters are modeled as Zero Order Hold (ZOH) blocks preceded by samplers. The total inductor current I_L equals the sum of the capacitor current and the output current I_{Out}, and hence the demanded I_L^* should ideally include a correction to allow for the capacitor fundamental frequency 50 Hz current. But since this current is very small in practice, it may be neglected and the demanded I_L^* can be set to the value of the required output current.

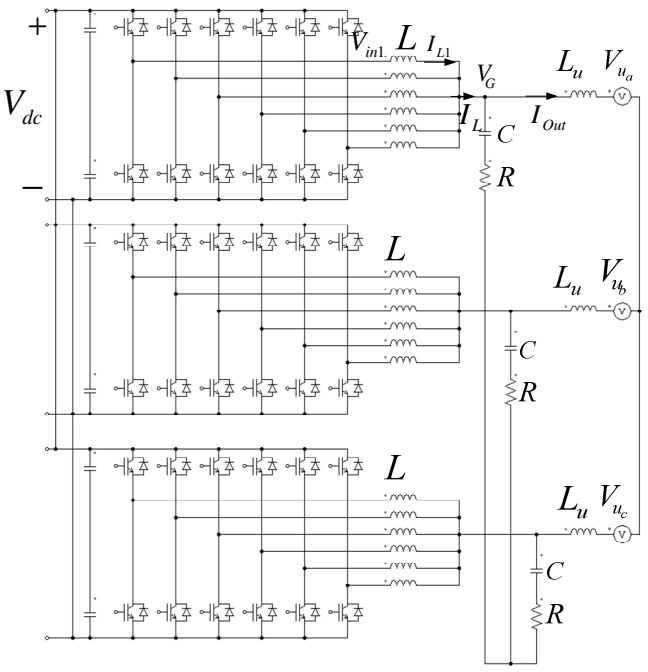

Fig. 1. Three-phase interleaved grid-connect interleaved inverter.

TABLE 1
SYSTEM PARAMETERS VALUES

Description	Symbol	Value
Number of interleaved channels	N	6
Passive damping resistor	R	0.5Ω
Channel inductor	L	150µH
Grid inductance	L_u	1 to 500 µH
Filter capacitor	C	10.8µF
Switching frequency	f_{sw}	35kHz
Sampling frequency	f_s	35kHz
Time delay	T_d	14.28µs
Output current	I_{Out}	50 Arms
Grid voltage	V_u	
Grid voltage at the point of common coupling	V_G	230 Vrms
Grid Frequency	F	50Hz
Inverter dc voltage	V_{dc}	750 Vdc

TABLE 2.
NATURAL DAMPED FREQUENCY VERSUS L_u.

L_u (µH)	**Natural damped frequency f_d (kHz)**
5	23.7
20	14.5
100	10.8

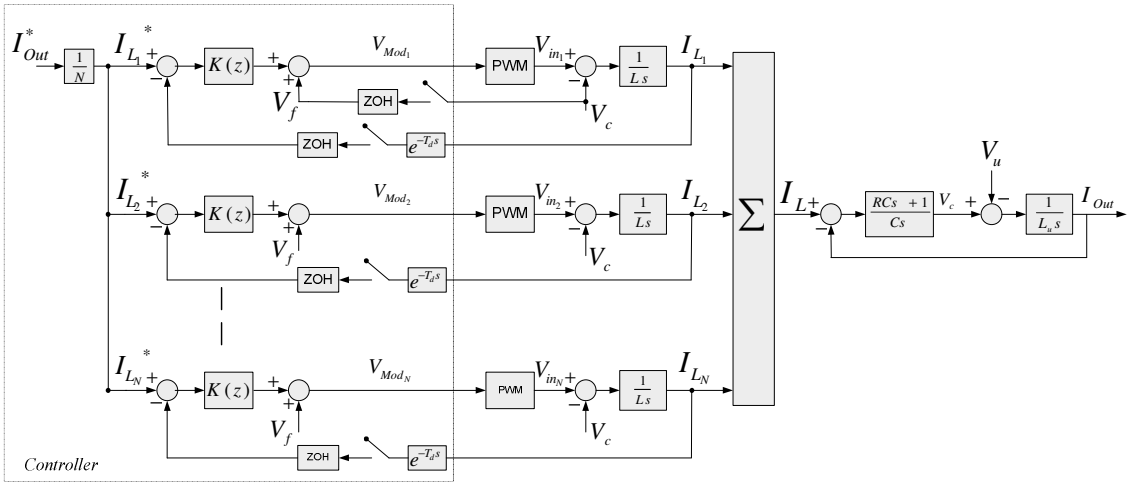

Fig. 2. Block diagram of one phase and its controller.

III. SYSTEM ANALYSIS

In this section, the effects of the passive damping resistor R, the computational time delay T_d, and the variation in grid impedance L_u on system stability are studied. The system ability to reject grid harmonics is also analyzed. For the purpose of the discussion in this section, which meant to provide an insight into the problem, the controller $K(z)$ is assumed to be a simple proportional gain with a value of 10. In the next section, the design of a more sophisticated controller $K(z)$ is discussed.

From Fig. 2, the transfer function $A(s)$ of I_{Lx} to V_{in_x} is given by

$$A(s) = \frac{L_u C s^2 + RCs + 1}{LL_u C s^3 + RC(L + NL_u)s^2 + (L + NL_u)s} \tag{2}$$

The continuous time delay open loop transfer function including the computational time delay block will therefore be given by

$$G(s) = e^{-T_d s} A(s) \tag{3}$$

In the discrete domain, $G(z)$, can be obtained by performing the Z-transform of $G(s)$ taking into account the zero order hold effect,

$$G(z) = Z\left[\frac{1 - e^{-T_s s}}{s} e^{-T_d s} A(s)\right] \tag{4}$$

$G(z)$ was computed using Matlab with the time delay $e^{-T_d s}$ approximated using Pade approximation.

A. *Effect of Passive Damping and Grid Impedance*

Without computational time delay (T_d = 0) and with R set to zero, the root locus of $K(z)G(z)$ is shown in Fig. 3, with L_u as a parameter varying from 1μH to 500μH. The closed loop poles are located at the border of the unit circle which means the system will be critically stable. In Fig. 4, the root locus of $K(z)G(z)$ is plotted when R is set to 0.5Ω. It is clear that the closed loop poles have been pushed well inside the unit circle making the system more stable. However, the system seems to suffer from a lack of immunity to grid impedance variations as it becomes unstable when L_u > 20μH.

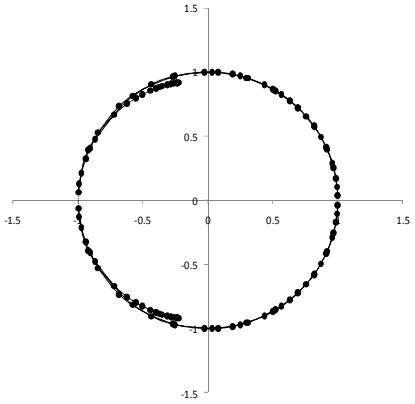

Fig. 3. Root locus of $K(z)G(z)$ with L_u changing from 0 to 500uH, T_d = 0, $K(z)$ =10, R = 0 Ω.

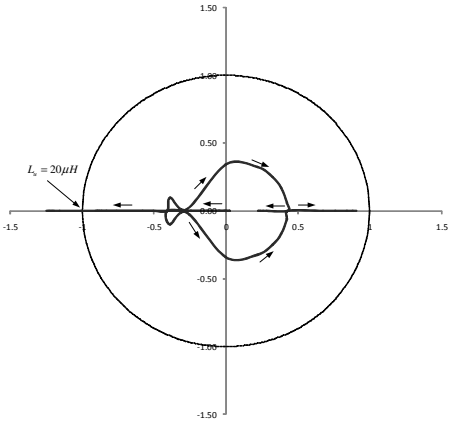

Fig. 4. Root locus of $K(z)G(z)$ with L_u changing from 0 to 500μH, T_d = 0, $K(z)$ =10, R = 0.5Ω.

B. Effect of the Computational Time Delay

Fig. 5 illustrates the sampling strategy for the proposed controller. In this system, the inductor currents are sampled at the same rate as the switching frequency. Each inductor current is sampled when the PWM carrier reaches its trough. The processor then starts performing the controller calculations and updates the modulating voltage V_{Mod} when the PWM carrier reaches its peak. In this case the time delay equals half of the sampling period,

$$T_d = 0.5T_s \tag{5}$$

Fig. 6 shows the root locus of $K(z)G(z)$ as a function of L_u when R is set to 0.5Ω but with T_d set to $0.5T_s$. The system becomes unstable only when L_u > 300μH. This is may be a surprising result as time delay normally reduces systems stability. To understand this phenomenon, the bode diagrams of $K(z)G(z)$ with and without time delay are plotted in Fig. 7. Although the time delay has decreased the phase margin (PM) from 72° to 32°, it also caused a magnitude attenuation which resulted in an increase in the gain margin (GM) from -1.5 to 3.5 and hence stabilized the system. Note that time delay in the continuous time domain does not alter the magnitude bode diagram because $\left|e^{-T_d s}\right| = 1$. However, in discrete time domain, time delay may alter the magnitude of the bode diagram.

C. Grid Harmonics Rejection

To completely compensate for the grid disturbance, the feedforward loop should ideally take the form of $B(s)V_u$ as discussed in [5] where

$$B(s) = \frac{RCs+1}{L_u Cs^2 + RCs + 1} \tag{6}$$

However, V_u cannot be measured directly and L_u varies according to the grid. Fortunately, the small value of C, makes a direct feedforward of grid voltage V_G at the point of common coupling, which is approximately equal to V_u, good enough to reject the grid harmonics disturbance.

With the feedforward loop and neglecting the sampling effect and time delay, I_L can be shown to be given by (assuming $I_L^* = 0$ in Fig. 2)

$$I_L = \frac{A(s)\left(1-B(s)\right)}{1+K(s)A(s)} NV_u \tag{7}$$

Note that $K(z)$ is expressed by its equivalent 's' function. If the feedforward loop of the grid voltage is not employed, (7) becomes

$$I_L = \frac{-A(s)B(s)}{1+K(s)A(s)} NV_u \tag{8}$$

Fig. 8 shows the bode diagram of I_L/V_u with and without the feedfrward loop for different values of L_u. The effectiveness of the feedforward loop in attenuating the grid voltage and its low frequency base harmonics is clear from the diagram.

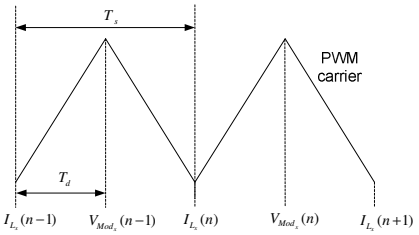

Fig. 5. Sampling Strategy.

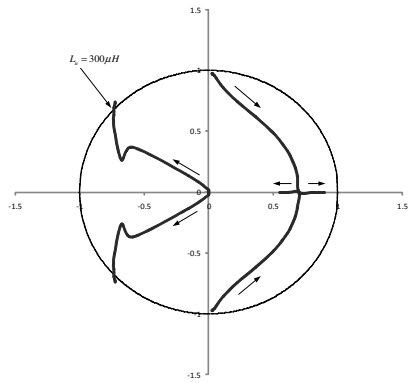

Fig. 6. Root locus of $K(z)G(z)$ with L_u changing from 0 to 500μH, $T_d = 0.5T_s$, $K(z)$ =10, R = 0.5Ω.

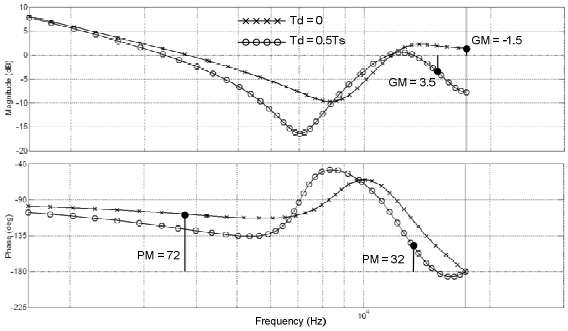

Fig. 7. Bode diagram of $K(z)G(z)$ with and without time delay, L_u = 40μH.

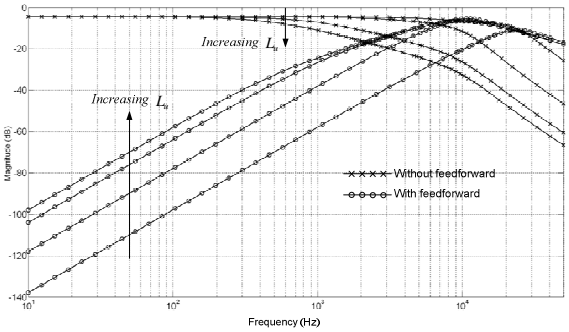

Fig. 8. Bode diagram of I_L/V_u with and without feedforward, L_u =5, 50, 250, and 500μH, $K(s)$ = 10.

IV. CONTROLLER DESIGN

The controller $K(z)$ needs to be designed to fulfill certain tasks. Firstly, it should provide good tracking of the reference signal. Secondly, it should provide good rejection of grid voltage harmonics. Thirdly, the controller stability has to be immune to variations in grid impedance. Good tracking and good grid harmonics rejection require a high gain value of $K(z)$ at the fundamental and the low frequency harmonics. However, high values of $K(z)$ mean less stability. The magnitude of $K(z)$ has already been chosen to be 10 to give a good low frequency gain. However, the system will become unstable when L_u > 300μH as was shown in Fig. 6. Fig. 9 shows the bode diagram of $K(z)G(z)$ with L_u having the values of 5, 50, 250, and 500μH. At high values of L_u, the gain margin becomes negative and hence the system becomes unstable. If $K(z)$ is modified to be a phase lag as illustrated in Fig. 10 then it provides more attenuation at the higher frequencies to improve the gain margin and at the same time increases the gain at the lower frequencies to improve reference signal tracking and grid harmonics rejection. The proposed phase lag controller is given by

$$K(z) = 10\frac{0.5z - 0.35}{z - 0.97} \tag{9}$$

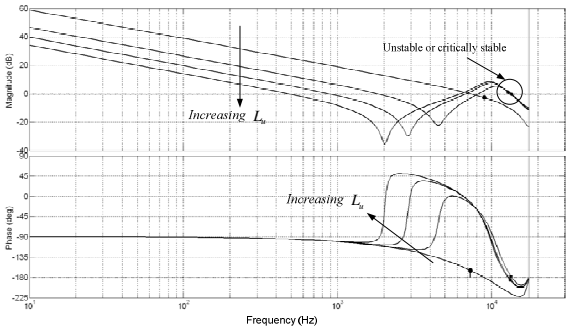

Fig. 9. Bode diagram of $K(z)G(z)$, $K(z)$=10, L_u = 5, 50, 250, and 500 μH.

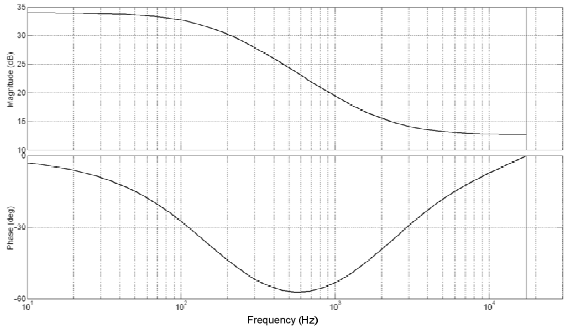

Fig. 10. Bode diagram of a phase lag K(z), $K(z) = 10\frac{0.5z - 0.35}{z - 0.97}$

Fig. 11 shows the bode diagrams of $K(z)G(z)$ with $K(z)$ as given in (9) for different values of L_u. It can be noticed that the system always has a positive gain margin. Also the low frequency gain is now higher, which will improve reference signal tracking and grid harmonics rejection. The root locus of $K(z)G(z)$ with L_u varying from 0 to 1mH is shown in Fig. 12. The system remains always stable and the immunity of the system to grid impedance variation is clear.

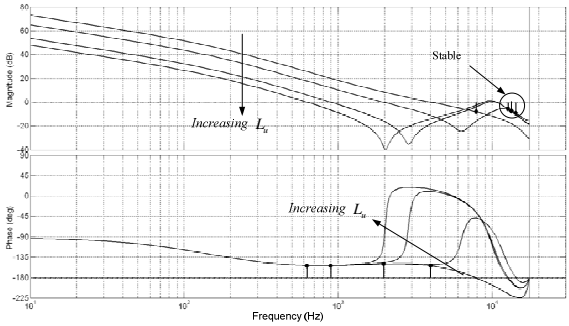

Fig. 11. Bode diagram of $K(z)G(z)$, $K(z) = 10\frac{0.5z - 0.35}{z - 0.97}$, L_u = 5, 50, 250, and 500 μH.

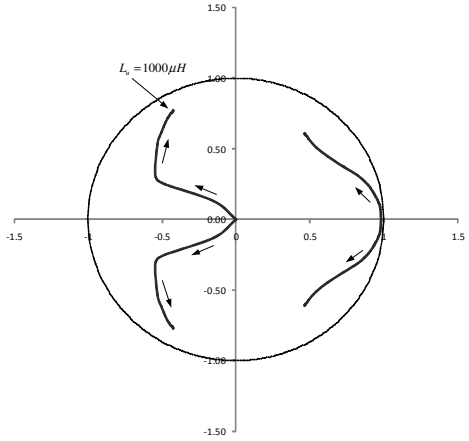

Fig. 12. Root locus of $K(z)G(z)$ with L_u changing from 0 to 1mH, $T_d = 0.5T_s$, R=0.5 Ω, and $K(z) = 10\frac{0.5z - 0.35}{z - 0.97}$.

V. SIMULATION AND PRACTICAL RESULTS

A detailed Matlab/Simulink model was used to aid the design and predict the performance of the system. The simulated grid voltage included low frequency harmonics similar to those measured at the test site. The total voltage THD was 2%. Fig. 13 shows the output current for a 50Amps rms demand. The current THD was only 2.1%. Fig. 14 shows the filter capacitor current to have a low magnitude at both the fundamental and switching frequencies.

A three-phase grid-connected interleaved inverter was designed and built. The proposed controller was implemented using the Texas Instrument TMS320F2808 32-bit Digital Signal Processor (DSP). One DSP per phase was used and the low speed communications between the controllers such as start/stop and total current commands were implemented using the Controller Area Network (CAN) protocol. Synchronization with the grid was implemented by having each phase controller measure the corresponding grid phase voltage to detect the zero crossing. Fig. 15 shows the grid voltage and the inverter output current. The grid voltage THD

was measured to be 1.8% and the output current THD was measured to be 2.3%. Fig. 16 shows the step response of the output current when the demand changes from zero to full value. The inverter has also been tested with various output inductors up to 1 mH to represent the grid impedance and robust stability has been confirmed.

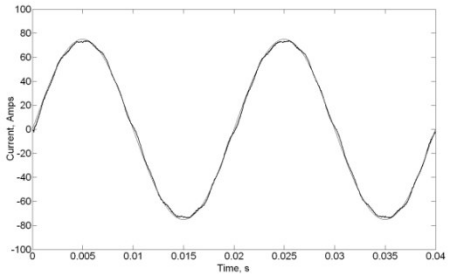

Fig. 13. Simulated output current

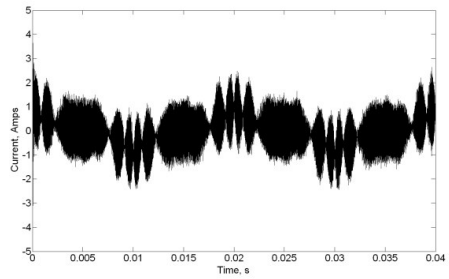

Fig. 14 Simulated capacitor current.

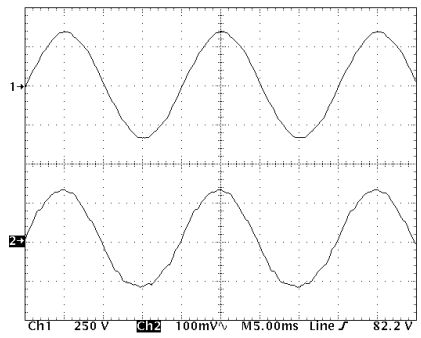

Fig. 15. Practical results, Ch1 grid voltage, Ch2 Output current 1Amps/2mv.

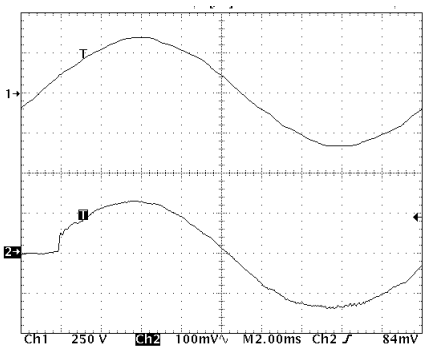

Fig. 17. Step response in current demand Ch1 grid voltage, Ch2 Output current 1Amps/2mv

VI. CONCLUSION

The design and practical implementation of a robust digital current controller for a three-phase voltage source grid-connected interleaved inverter has been presented. The interleaved topology offers the advantages of reduced filter size, and higher grid disturbance rejection compared to other inverter topologies. But the high resonance frequency of the filter required passive damping resistors in series with the filter capacitors, which was found to be acceptable due to the low capacitor currents. The grid impedance variations were found to reduce system stability. But using a phase lag compensator incorporated in the inductor current loop was found to be sufficient to increase the system's immunity to grid impedance variations. The design has been validated by simulation and practical results.

VII. REFERENCES

[1] S.M. Sharkh, M. Abu-Sara, and Z.F Hussien, "Current control of utility-connected DC- AC three-phase voltage-source inverters using repetitive feedback," *European Power Electronic Conference EPE*, Graz, 2001.

[2] E. Twining, and D.G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL filter," IEEE 33rd Annual Power Electronics Specialists Conference, 2002, 13, pp. 1189-1194.

[3] M. Prodanovic, T.C. Green, "Control and filter design of three-phase inverters for high power quality grid connection", IEEE *Transactions on Power Electronics*, 2003, 18, (1), pp. 373-380.

[4] G. Shen, D. Xu, L. Cao, and X. Zhu, "An Improved Control Strategy for Grid-Connected Voltage Source Inverters With an LCL Filter," *IEEE Transactions on Power Electronics*, vol. 23, NO. 4, 2008, pp. 1899-1906.

[5] S. M. Sharkh and M. Abu-Sara, "Digital current control of utility connected two-level and three-level PWM voltage source inverters," *European Power Electronic Journal*, vol. 14 No. 4, 2004, pp. 13-18.

[6] O. Bouhali, B. Francois, C. Saudemont, and E.M. Berkouk, "Practical power control design of a NPC multilevel inverter for grid connection of a renewable energy plant based on a FESS and a Wind generator," *IEEE Annual Conference on Industrial Electronics, IECON 2006*, pp. 4291-4296.

[7] S.V. Araujo, A. Engler, B. Sahan, and F. Antunes, "LCL Filter design for grid-connected NPC inverters in offshore wind turbines," *International Conference on Power Electronics*, Korea, October 2007.

[8] B.N. Singh, G. Joos, G, and P. Jain, " A new topology of 3-phase PWM AC/DC interleaved converter for telecommunication supply systems," *Industry Applications Conference*, vol. 4, pp. 2290-2296, 2000.

[9] M. Gerber, J. A. Ferreira, I. W. Hofsajer, and N. Seliger, " High Density Packaging of the Passive Components in an Automotive DC/DC Converter," *IEEE Transactions on Power Electronics*, vol. 20, 2005, pp. 268-2755.

[10] B. Destraz, Y. Louvrier, and A. Rufer, "High Efficient Interleaved Multi-channel DC/DC Converter Dedicated to Mobile Applications," *Industry Applications Conference* 2006, pp. 2518-2523.

[11] M. Pavlovsky, Y. Tsuruta, and A. Kawamura, "Pursuing high power-density and high efficiency in DC-DC converters for automotive application," *Power Electronics Specialists Conference PESC,* pp. 4142-4148, 2008.

[12] I. Cervantes, A. Mendoza-Torres, A.R. Garcia-Cuevas, and F.J. Perez-Pinal, " Switched control of interleaved converters," *Vehicle Power and Propulsion Conference VPPC*, pp. 1156-1161, 2009.

[13] N. Mohan, T. M. Undeland, W. P. Robbins, *Power Electronics, Converters, Applications, and Design.* John Wiley & Sons, 2003.

[14] K. Ogata, *Discrete-Time Control Systems.* Prentice Hall, 1995.